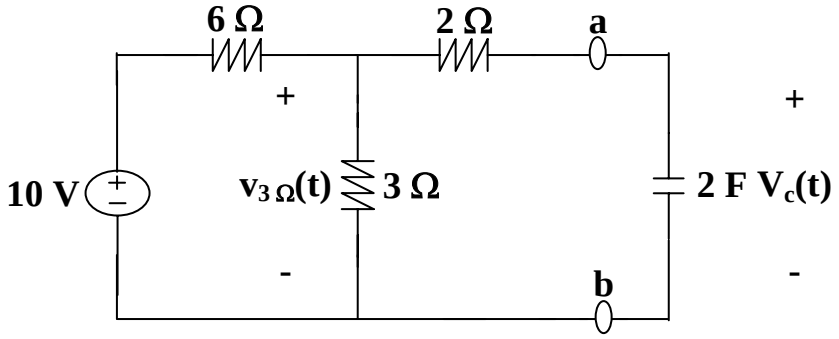
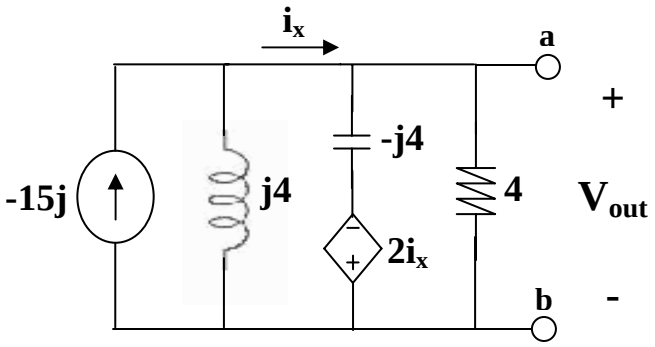
EE 209 Midterm #2

Problem 1: (25 pts)



a) Find Thevenin Equivalent of the resistive circuit on the left side of a-b terminals.
b) Using the result of part a), write a differential equation in terms of $V_c(t)$ characterizing the given circuit.
c) Given that $V_c(t)$ at t=0 is 2 V, i.e. $V_c(0)=2$ V; *find and plot* $V_c(t)$ for $t \geq 0$.
d) Given that $V_c(0)=2$ V; *find and plot* $V_{3\Omega}(t)$ for $t \geq 0$ using the result of part c).

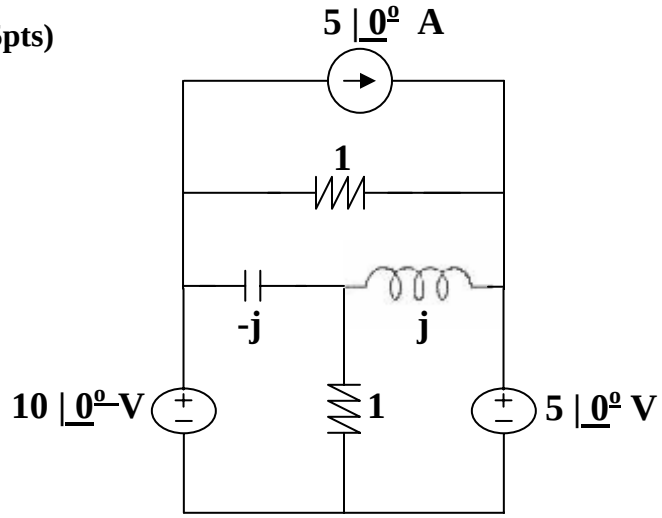
Problem 2: (25 pts)



The phasor equivalent of an AC circuit is given above.

a) Draw the circuit diagram for the time domain equivalent of the circuit if $\omega = 2$ rad/sec.
b) Find the phasor voltage of V_{out}.
c) Find the steady state value of $V_{out}(t)$ (take $\omega = 2$).
d) Find the equivalent impedance seen from a-b terminals.

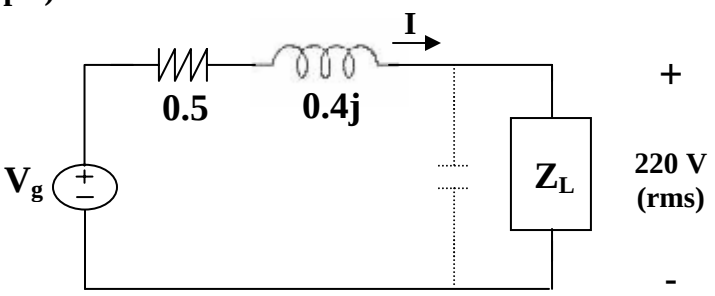
Problem 3: (25pts)



(Voltage and current values are in RMS)

a) Find the complex power of each one of the 7 components in the circuit.
b) Determine the real power of each source. State whether the source is supplying or absorbing power.
c) Determine the power factor of each source. State whether it is lagging or leading.

Problem 4: (25 pts)



The load shown by Z_L absorbs 60 kW at 0.8 pf lagging.

For the circuit shown above, a shunt capacitor is being planned to be installed in parallel with the load. (Assume that the load voltage stays at 220 V (rms) after the capacitor installation)

a) Find the magnitude of current I, the power loss on 0.5 Ω resistor and the magnitude of voltage V_g , when there is no shunt capacitor in the system.
b) Assume that the connected capacitor improves the power factor of the combined load (the capacitor and Z_L) to 0.95 lagging. Redo part a) when the capacitor is in-line.