Xyloni Development Kit User Guide

XYLONI-DK-UG-v1.2
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www.efinixinc.com

Contents

Introduction

Thank you for choosing the Xyloni Development Kit (part number: XYLONI), which allows you to explore the features of the T8 FPGA.

Figure 1: Xyloni Development Kit

Warning: The board can be damaged without proper anti-static handling.

What's in the Box?

The Xyloni Development Kit includes:

- Xyloni Development Board preloaded with a demonstration design
- 1 USB-A to Micro-USB cable
- 3 unsoldered pin headers

Register Your Kit

When you purchase an Efinix development kit, you also receive a license for the Efinity® software plus one year of software upgrades and patches. The Efinity® software is available for download from the Support Center on the Efinix web site.

To get access to our Support Center to download your software, register your development kit at https://www.efinixinc.com/register.

Download the Efinity® Software

To develop your own designs for the T8 device on the board, you must install the Efinity® software. You can obtain the software from the Efinix® Support Center under Efinity Software (www.efinixinc.com/support/).

The Efinity® software includes tools to program the device on the board. Refer to the **Efinity® Software User Guide** for information about how to program the device.

Learn more: The Efinity® Software User Guide is also installed with the software (see **Help** > **Documentation**).

Efinity® Software Requirement

Efinity® version 2020.1 with patch 2020.1.140.7.2 or later installed.

Installing the Linux USB Driver

The following instructions explain how to install a USB driver for Linux operating systems.

1. Disconnect your board from your computer.
2. In a terminal, use these commands:

```
> sudo <installation directory>/bin/install_usb_driver.sh
> sudo udevadm control --reload-rules
```

Note: If your board was connected to your computer before you executed these commands, you need to disconnect and re-connect it.

Install USB Drivers (Windows)

The Xyloni Development Board development board has a FTDI FT4232H chip to communicate with the USB port. This chip has separate channels that the board uses for the SPI, JTAG, and UART interfaces. You need to install a driver for each interface, and then each interface appears as a unique FTDI device.

Note: If you install a composite driver, all of the interfaces appear as a composite device and you cannot use them separately (which means you cannot use all of the features of the board).

On Windows, you use software from Zadig to install drivers (zadig.akeo.ie). In the Zadig software, the interface names end with *(Interface N)*, where *N* is the channel number.

Driver Options

The Zadig software includes a variety of drivers. When programming Efinix FPGAs, use one of these drivers:

- **libusb-win32** (*version*)—This driver is more stable for unplug/plug events. This driver does not work when debugging with OpenOCD.
- **libusbK** (*version*)—Use this driver if you plan to use OpenOCD to debug any Efinix RISC-V SoC.

Warning: Do **not** choose the WinUSB driver.

Install Drivers

1. Connect the board to your computer with the appropriate cable and power it up.
2. Download the Zadig software from zadig.akeo.ie. (You do not need to install it; simply run the downloaded executable.)
3. Run the Zadig software.

Note: To ensure that the USB driver is persistent across user sessions, run the Zadig software as administrator.

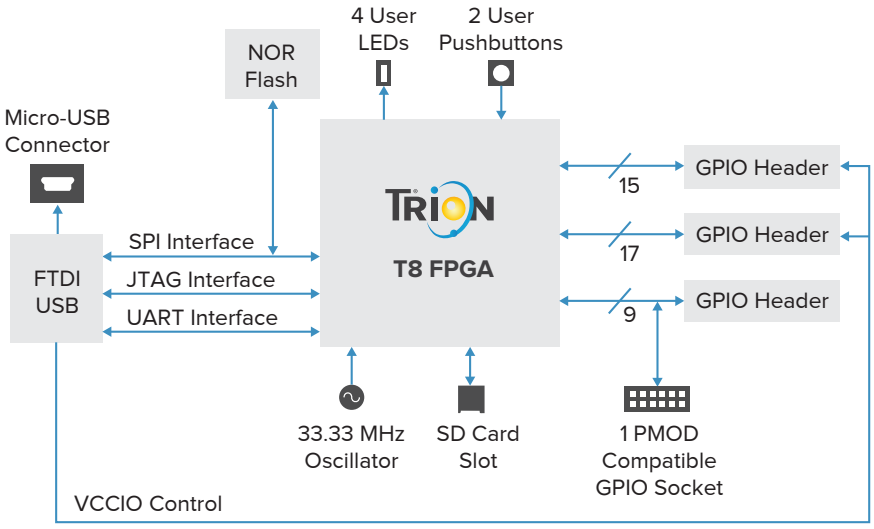
4. Choose **Options > List All Devices**.
5. Repeat the following steps for each interface. The interface names end with *(Interface N)*, where *N* is the channel number.
   - Select **libusb-win32** or **libusbK** in the **Driver** drop-down list. (Do **not** choose WinUSB.)
   - Click **Replace Driver**.
6. Close the Zadig software.

Important: For the Xyloni Development Board, install drivers for interfaces 0, 1, and 3 only. You do not need to install a driver for interface 2 because when you connect the Xyloni board to your computer, Windows automatically installs a driver for it.

Board Functional Description

The Xyloni Development Board contains a variety of components to help you build designs for the Trion® T8 device.

Figure 2: Xyloni Development Board Block Diagram



Features

- Efinix® T8F81C2 device in an 81-ball FineLine BGA package
- 128 Mbit SPI NOR flash memory
- FTDI FT4232H chipset with USB controller
- Dedicated UART interface through USB
- Micro-USB type B receptacle
- 41-pin high-speed connectors (including PMOD) for user I/O with unattached pin headers
- 12-pin PMOD-compatible GPIO socket
- Micro-SD card slot
- User LEDs and switches:
  - 4 LEDs on T8F81C2 bank 1B and 2B
  - 2 pushbutton switches (connected to bank 2A I/O pins)
- 33.33 MHz oscillator for T8F81C2 PLL input
- Power:
  - Power source: USB
  - User selectable voltages from 1.8 V, 2.5 V, and 3.3 V for bank 2A and 2B through USB
- Power good and T8F81C2 configuration done LEDs

Overview

The board features the Efinix® T8 programmable device in a 81-ball FBGA package, which is fabricated using Efinix® Quantum™ technology. The Quantum™-accelerated programmable logic and routing fabric is wrapped with an I/O interface in a small footprint package. T8 devices also include embedded memory blocks and multiplier blocks (or DSP blocks). You create designs for the T8 device in the Efinity® software, and then download the resulting configuration bitstream to the board using the USB connection.

Learn more: For more information on T8 FPGAs, refer to the T8 Data Sheet.

Figure 3: Xyloni Development Board Components (Top)

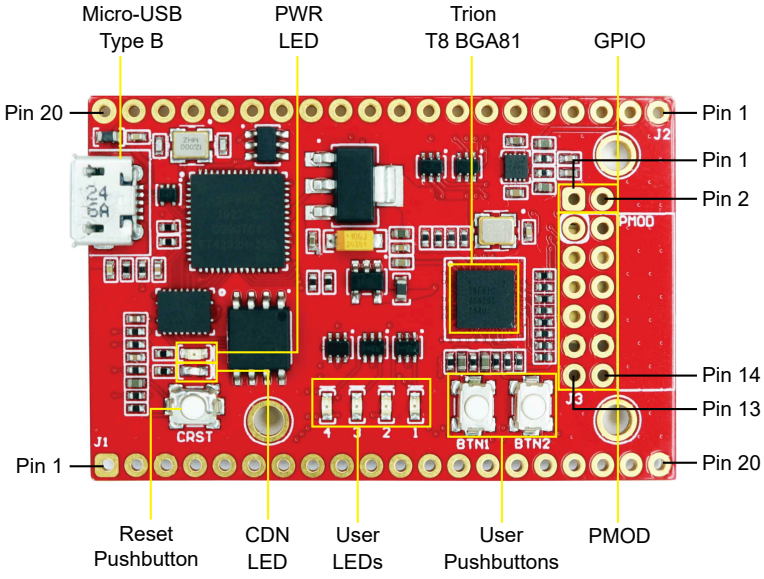
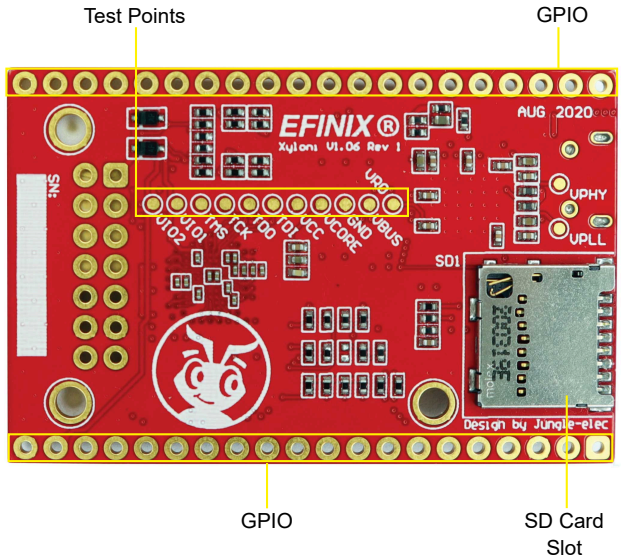


Figure 4: Xyloni Development Board Components (Bottom)



The FTDI FT4232H module has four channels to support the following interfaces:

- FTDI interface 0 = SPI
- FTDI interface 1 = JTAG
- FTDI interface 2 = UART
- FTDI interface 3 = VCCIO setting

It receives the T8 configuration bitstream from a USB host and writes to the on-board SPI NOR flash memory. After a reset in SPI passive mode, the FTDI controller can also write the configuration bitstream directly to the FPGA. Additionally, it supports direct JTAG programming mode in which it writes the configuration bitstream directly to the FPGA through the JTAG interface.

Learn more: Refer to **AN 006 Configuring Trion FPGAs** for more information.

The SPI NOR flash memory stores the configuration bitstream it receives from the FTDI FT4232H module. The T8 device accesses this configuration bitstream when it is in active configuration mode (default).

The board regulates down the 5 V DC input using on-board switching regulators to provide the necessary voltages for the T8 device, PMOD module, SPI flash memory, and on-board oscillator.

Learn more: Refer to the **Xyloni Development Board Schematics and BOM** for more information about the components used in the Xyloni Development Board.

Power On

To turn on the development board, connect the micro-USB connector to a computer. Upon power-up, the on-board regulators generates the required 3.3 V, 2.5 V, 1.8 V and 1.2 V voltages. The the red LED PWR illuminates when all the voltages are up and stable.

Selecting VCCIO

The Xyloni Development Board supports user selectable VCCIO from 1.8 V, 2.5 V, and 3.3 V for bank 2A and 2B through the USB interface. By default, the VCCIO for both banks are 3.3 V.

To change the Xyloni Development Board VCCIO:

1. Connect the Xyloni Development Board to the computer using the USB cable.
2. Run `xyloni_set_vccio.py <X>V <Y>V` command at the command line interface, where *X* is the new VCCIO for bank 2A and *Y* is the new VCCIO for bank 2B.

The following example shows the command to change the VCCIO for bank 2A to 2.5 V, and bank 2B to 1.8 V.

```
xyloni_set_vccio.py 2.5V 1.8V
```

Note: The VCCIO control uses the channel 3 of the USB interface. Make sure the channel driver is installed properly. Refer to the **Install USB Drivers (Windows)** on page 5 for more information about installing the USB driver.

Reset

The T8F81C2 device is typically brought out of reset with the CRESET signal. Upon power up, the T8F81C2 device is held in reset until CRESET toggles high-low-high.

CRESET has a pull-up resistor. When you press CRST pushbutton, the board drives CRESET low; when you release CRST pushbutton, the board drives CRESET high. Thus, a single press of CRST provides the required high-low-high transition.

After toggling CRESET, the T8F81C2 device goes into configuration mode and reads the device configuration bitstream from the flash memory. When configuration completes successfully, the device drives the CDONE signal high. CDONE is connected to a yellow LED (LED CDN), which turns on when the T8F81C2 device enters user mode.

Clock Sources

The Xyloni Development Board includes one 33.33 MHz oscillator. You can clock the T8F81C2 device using this oscillator, which drives the T8F81C2 PLL IN pin.

Configuration

The Xyloni Development Kit supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode.

In SPI active and passive mode, you can choose which image to load from the SPI flash by pulling the CBSEL0 and CBSEL1 pins high or low.

Table 1: Configuration Image Pins

CBSEL0	CBSEL1	Notes
High	Low	Load configuration image 0.
Low	High	Load configuration image 1.

Learn more: For more details on configuration, refer to AN 006 Configuring Trion FPGAs.

Headers

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

Table 2: Xyloni Development Board Headers

Reference Designator	Description
J1	20-pin connector for GPIO
J2	20-pin connector for GPIO
J3	12-pin PMOD socket and 2-pin connector for GPIO
USB1	Micro-USB type-B receptacle
SD1	SD card slot
Test Points	Test points

Headers J1 and J2

J1 an J2 are pins that you can use to control the GPIO. J1 connects to GPIO pins in bank 2B, and J2 connects to GPIO pins in bank 2A. J1 is connected to VCCIO1 and VCC, and J2 is connected to VCCIO2.

Note: The pin headers for J1 and J2 are not soldered to the Xyloni Development Board. You can choose to attach the header to the top or the bottom of the board. Attaching from the top makes the use of jumper cables easier while attaching from the bottom is commonly when connecting the headers to a breadboard.

Table 3: J1 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	VBUS	2	VCC
3	GND	4	GPIOR_20
5	GPIOR_21	6	GPIOR_22
7	GPIOR_23	8	GPIOR_24
9	GPIOR_25	10	GPIOR_26
11	GPIOR_27	12	GPIOR_28
13	GPIOR_30	14	GPIOR_31
15	GPIOR_32	16	GPIOR_34
17	GPIOR_35	18	GPIOR_36
19	VCCIO2	20	GND

Table 4: J2 Pin Assignments

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	VCCIO1
3	GPIOR_19	4	GPIOR_18
5	GPIOR_17	6	GPIOR_16
7	GPIOR_15	8	GPIOR_14
9	GPIOR_13	10	GPIOR_12
11	GPIOR_11	12	GPIOR_10
13	GPIOR_08	14	GPIOR_07
15	GPIOR_06	16	GPIOR_05
17	GPIOR_03	18	GPIOR_01
19	GPIOR_00	20	VBUS

Headers J3 (PMOD)

J3 is a 14-pin connector which consists of a 12-pin peripheral module (PMODs) and a 2-pin GPIO. You can use the PMOD to connect to a standard off-the-shelf modules such as ADC, DAC, audio, WiFi, Bluetooth, etc.

Table 5: J3 Pin Assignments

Pin Number	Signal Name	T8F81C2 Pin Name	Pin Number	Signal Name	T8F81C2 Pin Name
1	-	VBUS	2	-	GPIOL_7
3	PMOD_A_IO0	GPIOL_12	4	PMOD_A_IO1	GPIOL_13
5	PMOD_A_IO2	GPIOL_14	6	PMOD_A_IO3	GPIOL_15
7	PMOD_A_IO4	GPIOL_16	8	PMOD_A_IO5	GPIOL_17
9	PMOD_A_IO6	GPIOL_19	10	PMOD_A_IO7	GPIOL_18
11	GND	-	12	GND	-
13	VCC	-	14	VCC	-

USB1

USB1, a micro-USB type B socket, is the interface between the board and your computer for power and communication. Connect the micro-USB cable for configuring T8F81C2 FPGA and NOR flash.

SD1

The Xyloni Development Board includes an SD card slot, SD1. SD1 connects to GPIO pins in bank 1A. The SD card interface runs on serial peripheral interface (SPI) speed.

Table 6: SD1

Pin Name	Signal Name	T8F81C2 Pin Name
CD1	SD DET	-
CD2	VCC	-
G1	GND	-
G2	GND	-
G3	GND	-
G4	GND	-
T1	No Connect	-
T2	SD_CS	GPIOL_00
T3	SD_DI	GPIOL_03_CDI4
T4	VCC	-
T5	SD_SCLK	GPIOL_09_CDI2
T6	GND	-
T7	SD_DO	GPIOL_05_CDI5
T8	No Connect	-

Test Points

The Xyloni Development Board includes 13 test point pins. You can use the test points to monitor the state of the circuitry or to inject test signals.

Table 7: Test Point Pin Assignments

Test Point Name	Test Point Reference
TP1	VBUS
TP2	VCC
TP3	VCORE
TP4	VCC_IO1
TP5	VCC_IO2
TP6	GND
TP7	VRO
TP8	VPHY
TP9	VPLL
TP10	TDI
TP11	TDO
TP12	TMS
TP13	TCK

User Outputs

The board has 4 yellow user LEDs that are connected to I/O pins in T8F81C2 banks 2A, 1B, and 2B. By default, the T8F81C2 I/O connected to these LEDs are set as active high. To turn a given LED on, pull the corresponding I/O signal high.

Note: When adding these GPIO in the Efinity® Interface Designer, configure them as output pins.

Table 8: User Outputs

Reference Designator	T8F81C2 Pin Name	Active
LED1	GPIOL_21_NSTATUS	High
LED2	GPIOR_37_TESTN	High
LED3	GPIOR_16	High
LED4	GPIOR_17	High

User Inputs

The board has 2 pushbutton switches that you can use as inputs to the T8F81C2 device. The T8F81C2 bank 2A I/O signals connected to these switches have a pull-up resistor. When you press the switch, the signal drives low, indicating user input.

Table 9: User Pushbuttons

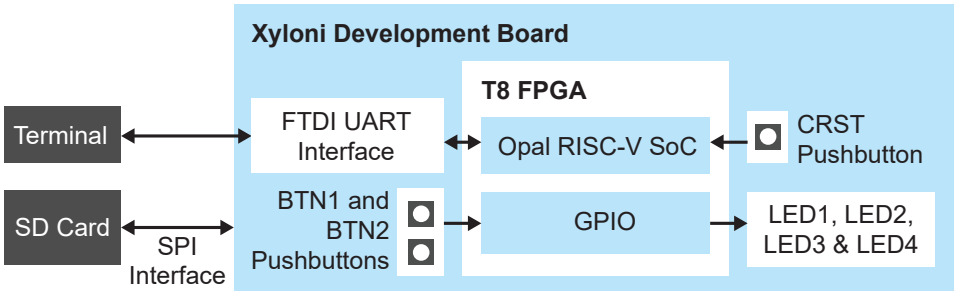
Reference Designator	T8F81C2 Pin Name	Active
BTN1	GPIOR_02	Low
BTN2	GPIOR_15	Low

Running the Example Design

Efinix® preloads the Xyloni Development Board with an example design and firmware. The design includes two functions, the invert LED operation and the read SD card information operation. The read SD card information operation requires a terminal program in a computer and an SD card inserted into the SD card slot to display the SD card information.

The example design implements an open-source variation of the Efinix®'s Opal RISC-V SoC. The Opal RISC-V is a cacheless, small footprint SoC that is ideal for applications that require embedded compute capability such as system monitoring or remote configuration and control. For more information, refer to the **Opal (Xyloni) RISC-V SoC Hardware and Software User Guide**.

Figure 5: Xyloni Development Board Example Design Block Diagram



Invert LED

Follow these steps to run the invert LED operation:

1. Connect the USB cable to the board and to your computer. LED PWR turns on, indicating that the board is receiving power correctly. When configuration completes, the configuration done (LED CDN) turns on. The LEDs turn on sequentially from LED1 to LED4.

   Note: If LED PWR does not turn on, the board is not receiving power correctly.

2. Press pushbutton BTN2 to invert the LEDs. The LEDs turn off sequentially from LED1 to LED4.

Read SD Card Information

Follow these steps to run the read SD card information operation:

1. Connect the USB cable to the board and to your computer. LED PWR turns on, indicating that the board is receiving power correctly. When configuration completes, the LED CDN turns on. The LEDs turn on sequentially from LED1 to LED4.

   Note: If LED PWR does not turn on, the board is not receiving power correctly.

2. Insert the SD card into the SC card slot.
3. Open a terminal software on the computer. You can use any Windows or Linux terminal applications such as, PuTTY, Tera Term, Minicom, and others.
4. Select the available USB COM port. Depending on the operating system settings, the terminal may show four COM ports instead of one. In that case, select the COM[2] port in the terminal software. Example:
   - In Windows, if the terminal shows COM30 COM31 COM32 COM33, select COM32.
   - In Linux, if the terminal shows ttyUSB0 ttyUSB1 ttyUSB2 ttyUSB3, select USB2.
5. Set the serial port baud rate to 115200 bits per second.
6. Press pushbutton BTN1. The terminal displays the following test menu:

```
==========Xyloni Test Menu==========
---Press BTN2 On Board - INVERT LED BLINK
---Press Keyboard 'Enter' Key  - READ SD CARD INFO
```

   Note: If the terminal does not display the Xyloni test menu correctly, verify that the port's baud rate is set correctly.

7. Press the Enter key, and the terminal displays the SD card information. For example:

```
=========SD Card Info=========

Manufacturer ID    : 3
Type               : Hard disk file system
TRAN_SPEED         : 10Mbit/s
SD CARD Size       : 15218 MByte
```

8. If there is no SD card in the SD card slot, the terminal displays:

```
Response Fail!! NO SD Card Detect
```

Creating Your Own Design

The Xyloni Development Board allows you to create and explore designs for the T8 device. Efinix® provides example code and designs to help you get started. Refer to the Xyloni GitHub page (https://github.com/github-efx/xyloni) for more examples targeting the board.

Note: For more information, email support@efinixinc.com.

Appendix 1: Shared Resources

Some of the resources available on the Xyloni Development Board are connected to more than one I/Os. You need to ensure there are no overlapping assignments when using these resources. The following table lists the resources shared by more than one I/Os. You can refer to this table to help you plan the resources available in the Xyloni Development Board

Note: Resources that are not listed are only available from one I/O (see Headers).

Table 10: Xyloni Development Board Shared Resources

<header name>.<pin name/number>

Resource	Connection 1	Connection 2
GPIOR_16	J2.6	LED.LED3
GPIOR_17	J2.5	LED.LED4
GPIOR_15	J2.7	Pushbutton.BTN2

Revision History

Table 11: Revision History

Date	Version	Description
April 2022	1.2	Corrected J1 and SD1 header pin names. Added Appendix 1: Shared resources. Corrected What's in the Box topic, updated hyperlinks, improved USB driver installation steps and editorial changes. (DOC-775)
December 2020	1.1	Added pin number labels to Xyloni Development Board Components (Top) figure. (DOC-356)
November 2020	1.0	Initial release.