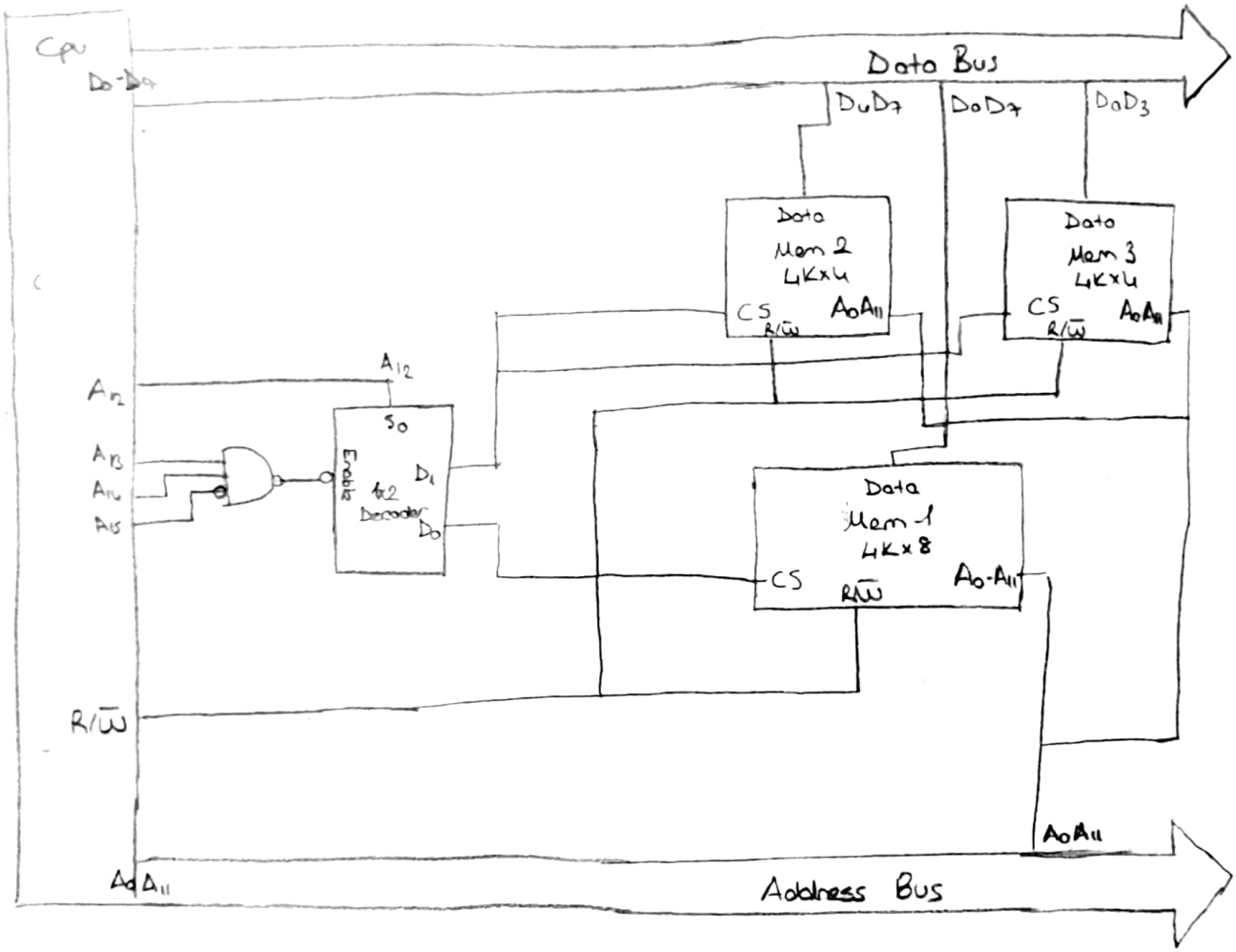
Çağla Midikli
150200011

		Enable D_0	12 bits
Module 1	$6000	0110	0000 0000 0000
	$6FFF	0110	1111 1111 1111

		Enable D_1	
Module 2	$7000	0111	0000 0000 0000
	$7FFF	0111	1111 1111 1111



First of all, since I have one 8 bit and two 4bit memory chips and Data Bus should be 8 bit. I connect the two 4-bit memory chips in paralel to create an 8 bit memory space. When I calculate the memory address ranges. I noticed that the first twelve bits of the address specify the location. While the 13th bit depends on the selected chips. Therefore A_{12} is used as input to a 1x2 Decoder to choose between the two chip group. The address range A_0A_{11} is connected to address bus. The range $A_{13}A_{15}$ remains unchanged so is appropriately connected to the decoder's enable input. I have connected the R/$\overline{W}$ signal from the CPU to each memory chips seperately. When the first chip active, output data is D_0D_4. When the second and third chips are active. The data from the second chips in the D_4D_7 range and data from the third chips is in the D_0D_3 range Thus completing 8 bit data bus.