General 2-PORT SRAM
32 WORDS X 16 BITS, MUX 1
SMIC 55nm LL Logic Process

Version 1.1.0

OVERVIEW

The General 2-PORT SRAM is designed for SMIC's 55nm CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.08V to 1.32V and a temperature range of -40^{o} C to 125^{o}C.

Chip enable (CENA,CENB), address (AA[0:i],AB[0:i]) and data in (DB[0:n]) signals are latched on the rising-edge of the clock. When CENA is low, the memory is in read-mode. Data is read from the memory location specified on the address bus AA[0:i] and appears on the data output bus QA[n:0].When CENB is low, the memory is in write-mode. The word on the data port DB[0:n] will be written into the location specified by the address AB[0:i] and the data will appear on the output port QA[n:0].When CENA is high, port A enters the standby mode. Data outputs remained stable.When CENB is high, port B enters the standby mode. Data stored in the memory is retained, but the new data writes is not allowed.

CONFIGURATION:

PARAMETER	VALUE
Mux	1
Words	32
Bits	16
Width	100.74um
Height	58.915um
Area	5935.097um^{2}

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
AA[4:0]	Input	A Port Address Inputs
AB[4:0]	Input	B Port Address Inputs
DB[15:0]	Input	B Port Data Inputs
CENA	Input	A Port Enable
CENB	Input	B Port Enable
CLKA	Input	A Port Clock Input
CLKB	Input	B Port Clock Input
QA[15:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	FF CORNER 1.32V, -40°C		FF CORNER 1.32V, 0°C		FF CORNER 1.32V, 125°C		SS CORNER 1.08V, -40°C		SS CORNER 1.08V, 125°C		TT CORNER 1.2V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	0.289		0.309		0.356		0.882		1.013		0.528	
Ta	Access Time[1]	0.263		0.280		0.324			0.802		0.921		0.480
Tah	Address Hold	0.094		0.093		0.092		0.195		0.111		0.096	
Tas	Address Setup	0.366		0.404		0.418		0.651		0.637		0.421	
Tch	Cen Hold	0.042		0.039		0.033		0.032		0.000		0.019	
Tcs	Cen Setup	0.311		0.315		0.326		0.800		0.683		0.398	
Tdh	Data Hold	0.211		0.211		0.211		0.411		0.321		0.242	
Tds	Data Setup	0.297		0.321		0.376		0.781		0.781		0.331	
Tckh	Clock High	0.020		0.020		0.020		0.040		0.040		0.020	
Tckl	Clock Low	0.099		0.099		0.110		0.231		0.264		0.143	
Tckr	Clock Rise Skew	0.500		0.500		0.500		1.000		1.000		0.600	
Tcc	Clock Collision	0.263		0.280		0.324		0.802		0.921		0.480	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

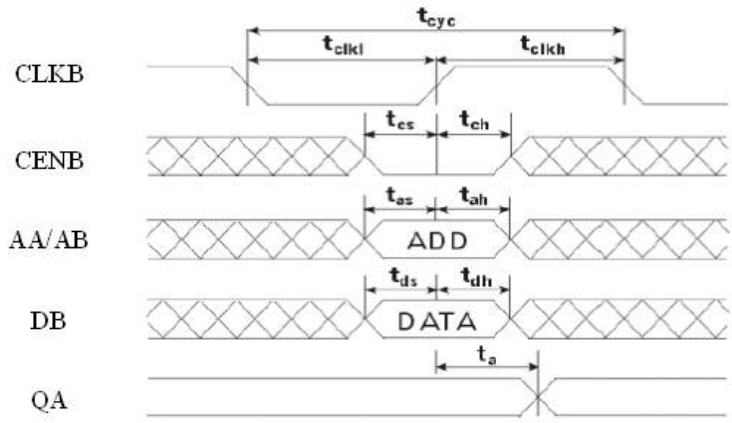
POWER:(UNITS=uA/Mhz)

PARAMETER	FF CORNER 1.32V, -40°C	FF CORNER 1.32V, 0°C	FF CORNER 1.32V, 125°C	SS CORNER 1.08V, -40°C	SS CORNER 1.08V, 125°C	TT CORNER 1.2V, 25°C
AC Current[2]	4.361	4.375	4.812	3.328	3.458	3.839
Read AC Current	3.931	3.891	4.380	2.943	3.085	3.395
Write AC Current	4.792	4.859	5.244	3.712	3.830	4.283
Standby Power (mW)	0.000485	0.002379	0.108599	0.000018	0.001582	0.000362
Deselect Power (mW)	0.052516	0.052834	0.040381	0.030140	0.031541	0.039681

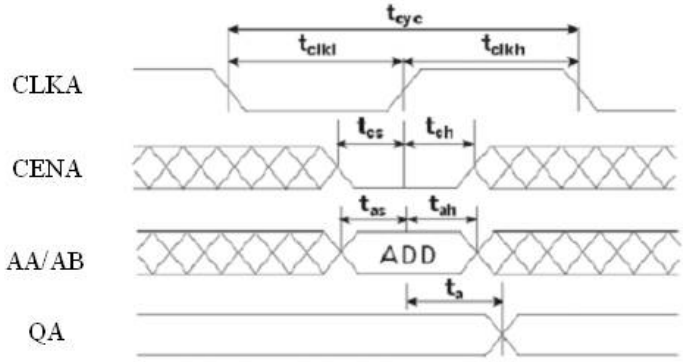
Power simulation conditions:

2. CEN is low, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz
3. CEN is high, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:



READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	null	

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