CMPE 122/222 Homework 3 - Winter 2019

Due: February 12, 12:30pm (one hour before class)
125 Points

Fixes:

- 3/8/19: Added setup.tcl requirement.

Please start early. This homework has several parts! Please ask all questions in Piazza for others to see.

First, read through this entire assignment. Second, you should read through the HW3 tutorial that teaches you how to use IRSIM for digital simulation, netgen for LVS and xcircuit for schematic entry. You should also review the portion of the Magic tutorials on hierarchical design.

The final part of this homework is to design the spice netlist and layout for an 8-bit ripple carry adder, show its logic correctness (using logic derivations and digital simulation), and measure its area (μm^2).

The inputs to the adder should be A7..A0, B7..B0, CIN. The outputs should be SUM7..SUM0 and COUT. Note these are capitalized and the 0 bits are the least significant. You should only use one label for the inputs and outputs in the layout (i.e., do not connect nets by label). It is acceptable to use more than one label for vdd and gnd rails (but not internal to the cell) since these will be connected later at the chip level.

The layout area is the bounding box of your design – in other words, the smallest rectangle that can enclose all the shapes in your layout.

Your ADDER should instantiate full-adder (FA) cells hierarchically and route them together to make a ripple carry adder. Your FA cell may use other sub-cells if you wish, or it can be flat. However, be sure to include all the sub-cells if you use additional ones. It is highly recommended to look ahead in the book to find more efficient FA circuits – this will save you time and area.

Your LVS scripts should be able to be run with the following commands:

```
netgen -noconsole source FA.tcl
netgen -noconsole source ADDER.tcl
```

It should exit at the end.

Your IRSIM scripts should be able to be run with the following commands:

```
irsim scmos30.prm FA.sim -FA.cmd
irsim scmos30.prm ADDER.sim -ADDER.cmd
```

It should quit at the end.

You should create a directory called "hw3" in your git repository. Please pay careful attention to the case, extension and spelling in all file names, inputs, and outputs. In this directory, please commit and push the following files:

- A copy of **scmos30.prm** for IRSIM simulations.
- A full adder layout **FA.mag** (and any other cell layouts if you used more hierarchy).
- A full adder spice file **FA.spc** created by hand or in xcircuit. This should include all subcircuits if you used any.
- A full adder IRSIM sim netlist **FA.sim** (created by xcircuit or Magic).
- An IRSIM command file **FA.cmd** to verify your full adder (FA.sim)
- Your hierarchical adder layout file **ADDER.mag**.
- Your spice file for the adder **ADDER.spc** created by hand or in xcircuit. This should include all subcircuits such as the FA.
- Your LVS setup script for the full adder **FA.tcl**.
- You must include a (possibly modified!) **setup.tcl**.
- Your extracted spice file **ADDER.spice** (from Magic) using ext2spice.
- An adder IRSIM sim netlist **ADDER.sim** (created by xcircuit or Magic).
- An IRSIM command file **ADDER.cmd** to verify your full adder spice file (ADDER.sim)
- Your LVS setup script for the adder **ADDER.tcl**.
- (Optional) Your adder schematic files **ADDER.ps** (this should include all other cell schematics).
- A very brief report in text format (**hw3.txt**) summarizing your area result in μm^2 and the logic explanation of your FA/ADDER. Write equations like this: !a + !(b & c)
- Submit your final commit ID: `http://bit.ly/2F7XIvK`

The grading rubric will be:

- FA DRC: 15
- FA LVS: 15
- FA IRSIM: 15
- Adder DRC: 20
- Adder LVS: 20
- Adder IRSIM: 20
- Layout quality (minimum area, correct cell height, hierarchical design, standard cell style, no connect by label): 15
- Report: 5