HW4: VLSI Design (CMPE 222)

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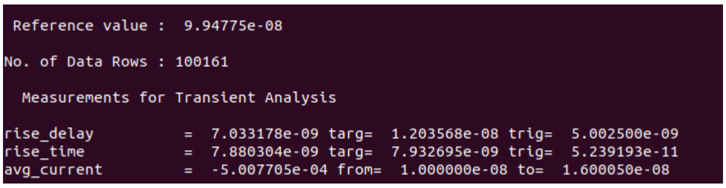
Due Tuesday February 26th 12:30PM

1. What is the worst-case delay in ps of your ADDER using ngspice WITHOUT extracted parasitics? You should set the inputs appropriately to 1 or 0 and toggle the CIN to cause the COUT to change.

As the figure bellow shows, the delay is: $7.03317 \times 10^{-9} = 703\,ps$



```
 Reference value :  9.94775e-08
No. of Data Rows : 100161
  Measurements for Transient Analysis
rise_delay          =  7.033178e-09 targ=  1.203568e-08 trig=  5.002500e-09
rise_time           =  7.880304e-09 targ=  7.932695e-09 trig=  5.239193e-11
avg_current         =  -5.007705e-04 from=  1.000000e-08 to=  1.600050e-08
```

Figure 1: Results for the ADDER.spc simulation at 3.3V 20°C.

The following picture displays the plot of CIN and COUT of the ADDER.spc simulation:

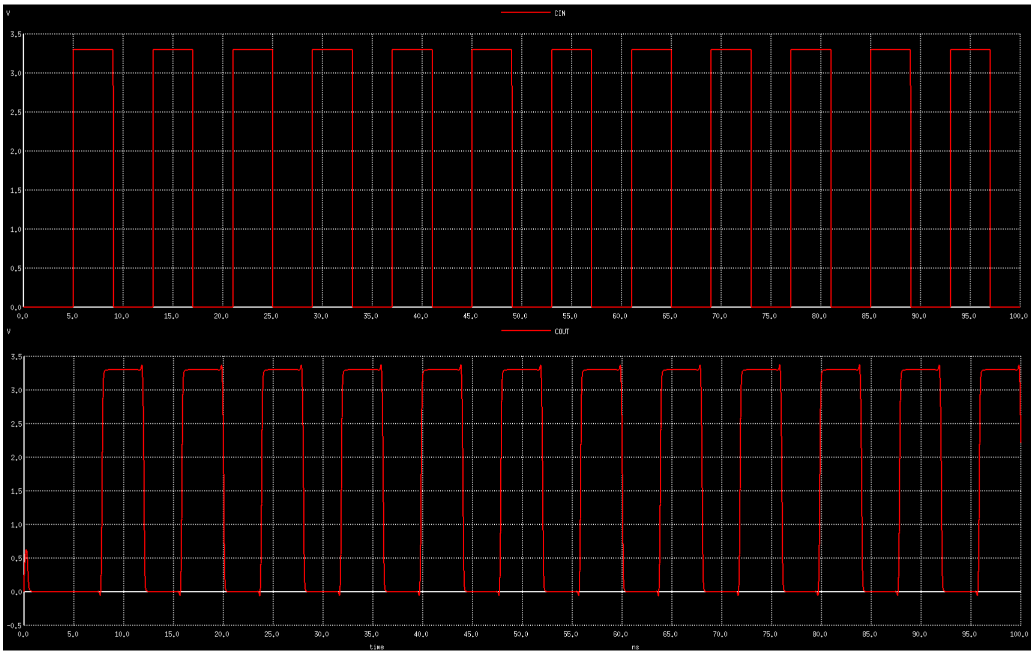


Figure 2: CIN and COUT plot.

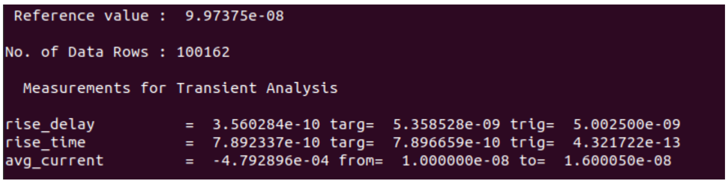
2. What is the power in nW of this worst-case input pattern WITHOUT parasitics?

As the fig.1 shows, the total current from 10n to 16n is: 5.007705×10^{-4}, therefore the power can be obtained as:

$$(3.3\text{V})(5.007705 \times 10^{-4}\text{A}) = 0.001652543\text{W} = 1652543\text{nW}$$

3. What is the worst-case delay in ps of your ADDER using ngspice WITH extracted parasitics using the same input pattern?

As the figure bellow shows, the delay is: $3.560284 \times 10^{-9} = 356\,ps$



```
 Reference value :  9.97375e-08

No. of Data Rows : 100162

  Measurements for Transient Analysis

rise_delay          =  3.560284e-10 targ=  5.358528e-09 trig=  5.002500e-09
rise_time           =  7.892337e-10 targ=  7.896659e-10 trig=  4.321722e-13
avg_current         =  -4.792896e-04 from=  1.000000e-08 to=  1.600050e-08
```

Figure 3: Results for the ADDER.spice simulation at 3.3V 20°C.

The following picture displays the plot of CIN and COUT of the ADDER.spc simulation:

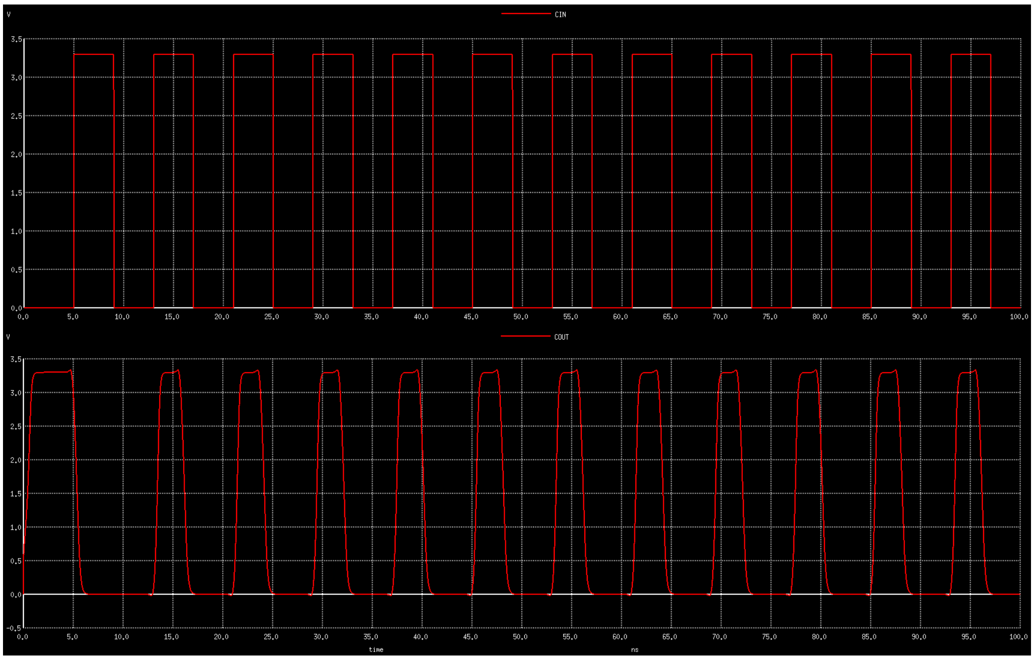


Figure 4: CIN and COUT plot.

4. What is the power in nW of the same input pattern WITH parasitics?

As the fig.3 shows, the total current from 10n to 16n is: 4.792896×10^{-4}, therefore the power can be obtained as:

$$(3.3\text{V})(4.792896 \times 10^{-4}\text{A}) = 0.001581656\text{W} = 1581656\text{nW}$$

5. Using logical effort, how many stages of minimum-size inverters are needed to create a 200MHz oscillator?

The frequency of the ring oscillator is given by:

$$f = \frac{1}{2dn} \tag{1}$$

Now, solving for n:

$$n = \frac{1}{2df} \tag{2}$$

Considering that the logical effort for an inverter is equal to 1 and $\tau = 40 \cdot 10^{-12}$ we then have:

$$n = \frac{1}{2 \cdot (200 \cdot 10^{6}) \cdot (40 \cdot \ 10^{-12})} \approx 62.5 \tag{3}$$

6. Design this ring oscillator in spice and Magic using hierarchical design techniques (e.g. provide an inverter subcircuit and an oscillator subcircuit in one file). The output at the top-level should be named OSC. You may only change the number of stages. You should assume minimum transistor lengths and balance the P and N sizes appropriately.

I tried different configurations for the oscillator, then by trial and error I found that for the ideal ring oscillator 39 stages give an almost exact 200Mhz. The magic desing is shown bellow:

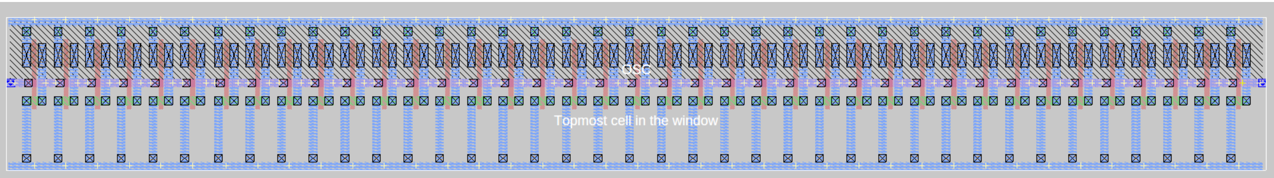


Figure 5: Magic design.

7. What is the oscillator frequency without parasitics?

The results of the simulation are shown bellow. we can notice that the oscillator needs about 30ns to stabilize.

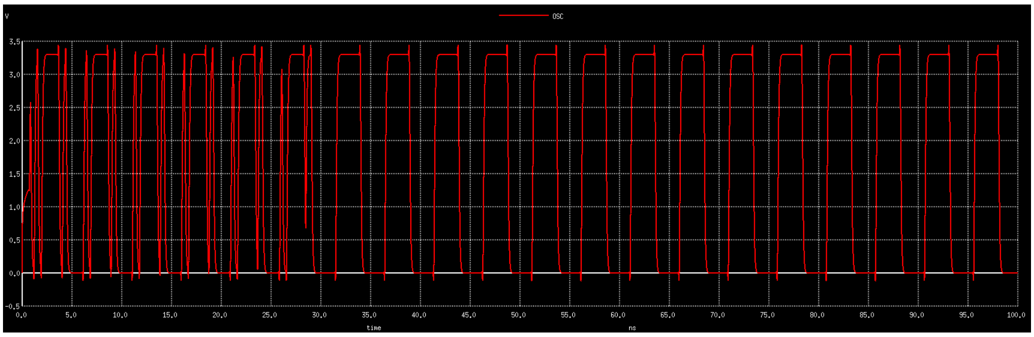


Figure 6: Simulation results for the ideal oscillator at 3.3V and 20°C.

We can see from the picture bellow that the frequency is approximately: 200**Mhz**.

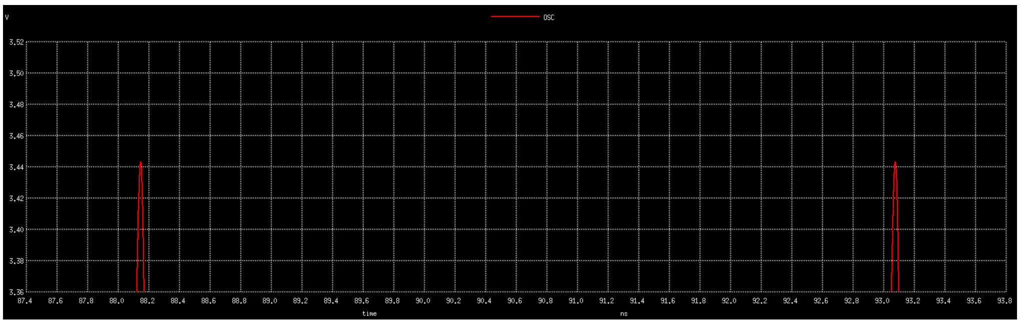


Figure 7: Frequency ideal oscillator at 3.3V and 20°C.

8. What is the oscillator frequency with parasitics?

The results of the simulation are shown bellow. we can notice that the oscillator needs about 2ns to stabilize.

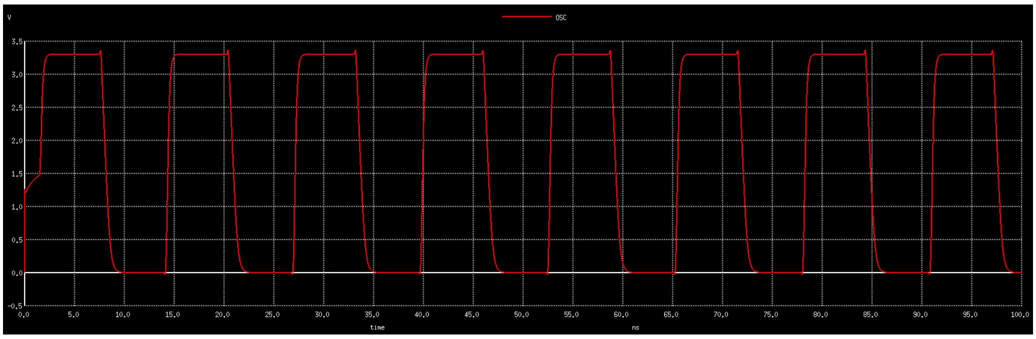


Figure 8: Simulation results for the extracted oscillator at 3.3V and 20°C.

We can see from the picture bellow that the frequency is approximately: 78.4313725**Mhz**.

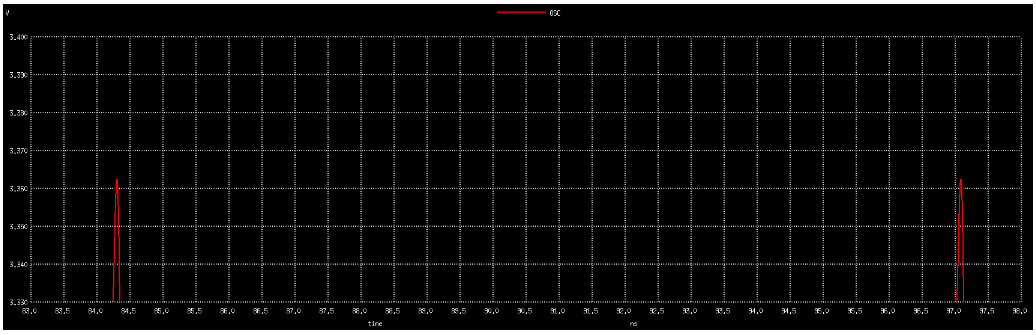


Figure 9: Frequency extracted oscillator at 3.3V and 20°C.

9. How does the ring oscillator frequency vary over the supply voltage range 1V to 5V ? You may do this manually or using ngspice scripting. Use at least 4 points.

The following pictures show the results fro the simulations at the different voltages:

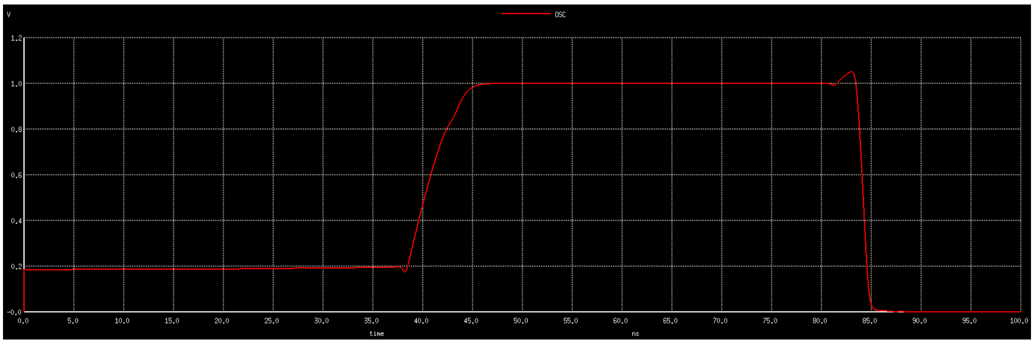


Figure 10: Frequency > 10Mhz at 1V and 20°C.

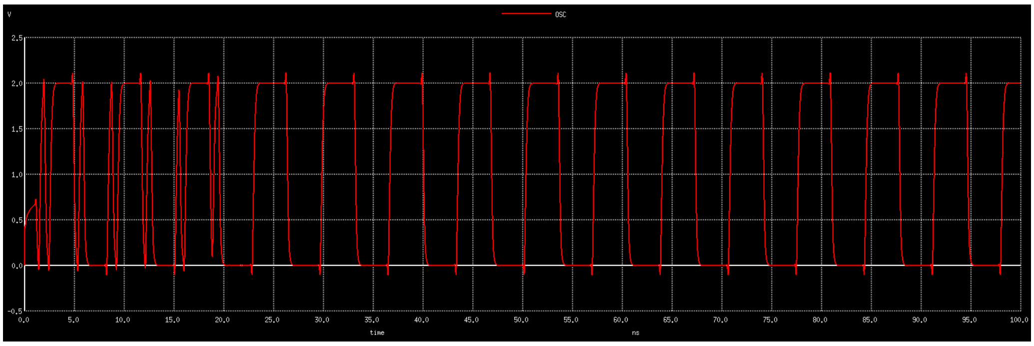


Figure 11: Frequency $\approx$ 148.15Mhz at 2V and 20°C.

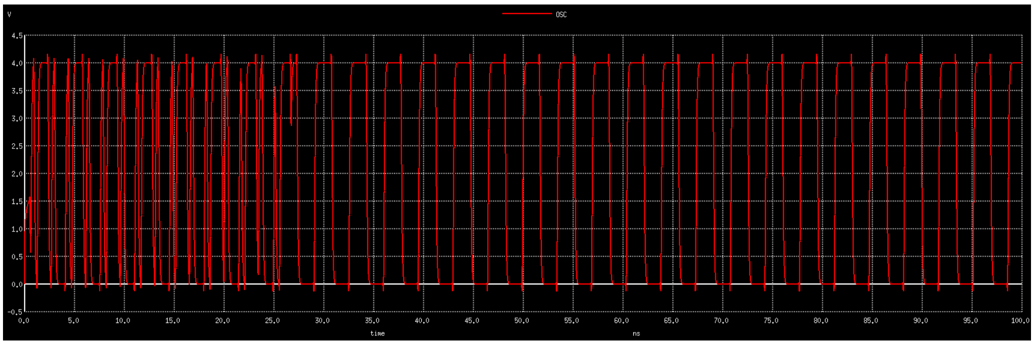


Figure 12: Frequency $\approx$ 285.71Mhz at 4V and 20°C.

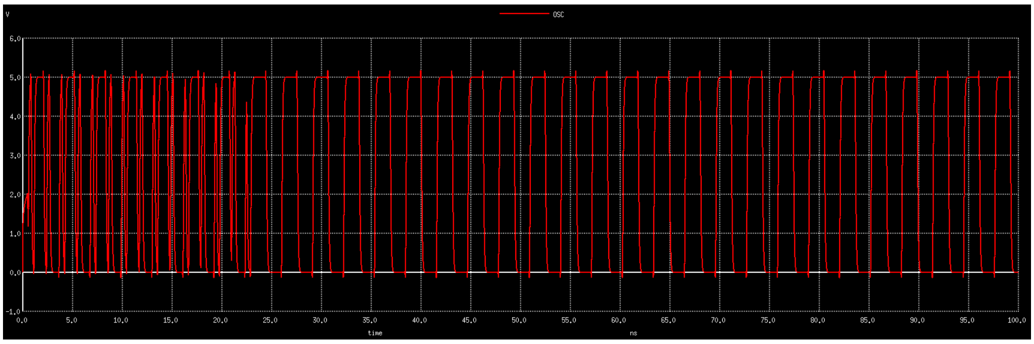


Figure 13: Frequency $\approx$ 322.58Mhz at 5V and 20°C.

10. How does the ring oscillator frequency vary with temperature from 0C to 100C? You may do this manually or using ngspice scripting. Use at least 4 points.

The following pictures show the results fro the simulations at the different temperatures:

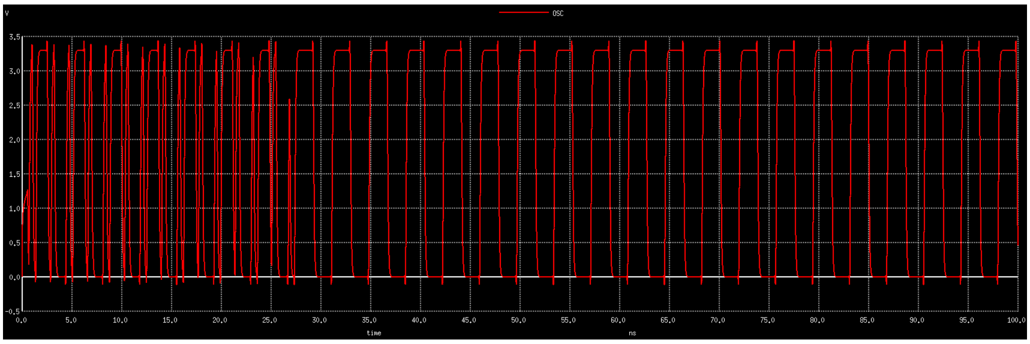


Figure 14: Frequency ≈ 270.27Mhz at 3.3V and 0°C.

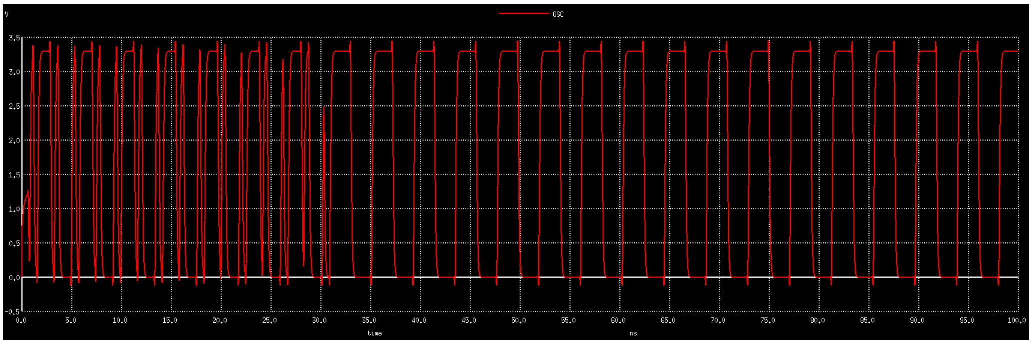


Figure 15: Frequency ≈ 238.09Mhz at 3.3V and 40°C.

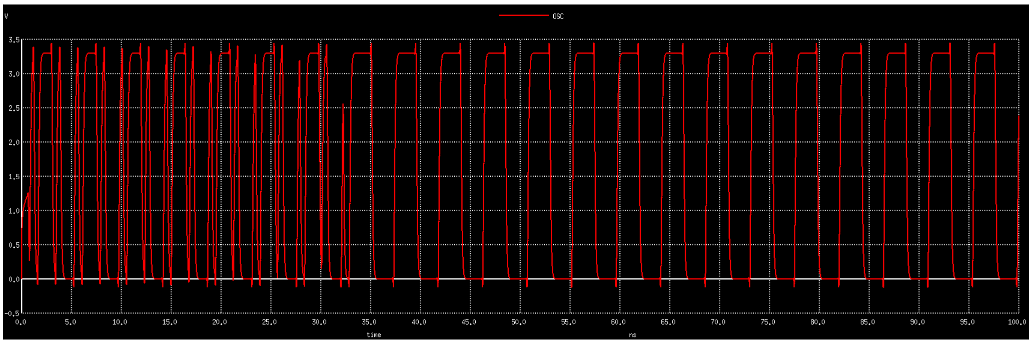


Figure 16: Frequency ≈ 222.22Mhz at 3.3V and 60°C.

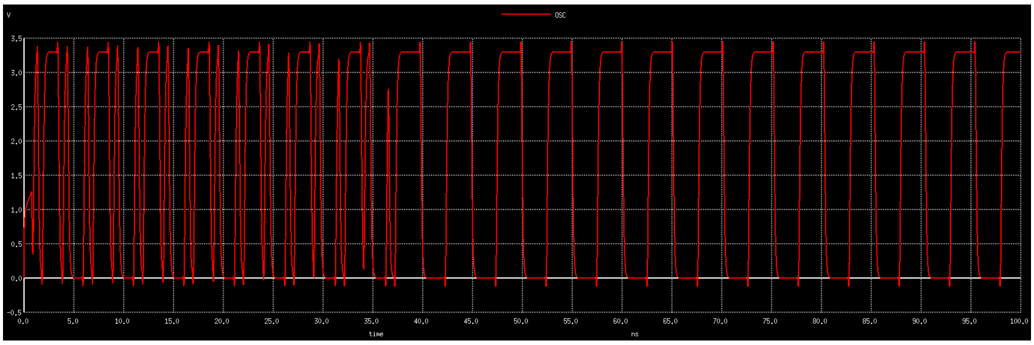


Figure 17: Frequency $\approx$ 190.47Mhz at 3.3V and 100°C.