Block Diagram:





Describe Operation:

Parameter:

1. Testbench have to receive awready and wready signal from fir.v before transfer the data(awaddr, wdata) and valid(awvalid, wvalid) signal, in the data transfer process from testbench to tap RAM we gotta make sure the tap_WE and tap_EN are high.

2. By setting tap_WE=0 and tap_EN=1, we access data from both shiftRam and tapRAM to computation.

3. When RIF process all the dataset, ap_done is generated via setting address to 0x01.
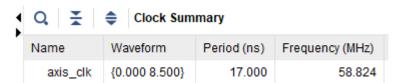
Resource Usage:

1.Two Brams for tapRam and dataRam,

2.Register including :three counters, state and register in MAC accumulation.

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+--------------------------+------+-------+------------+-----------+-------+
|         Site Type        | Used | Fixed | Prohibited | Available | Util% |
+--------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*              |  263 |   0   |      0     |   53200   |  0.49 |
|   LUT as Logic           |  263 |   0   |      0     |   53200   |  0.49 |
|   LUT as Memory          |    0 |   0   |      0     |   17400   |  0.00 |
| Slice Registers          |  155 |   0   |      0     |  106400   |  0.15 |
|   Register as Flip Flop  |  123 |   0   |      0     |  106400   |  0.12 |
|   Register as Latch      |   32 |   0   |      0     |  106400   |  0.03 |
| F7 Muxes                 |    0 |   0   |      0     |   26600   |  0.00 |
| F8 Muxes                 |    0 |   0   |      0     |   13300   |  0.00 |
+--------------------------+------+-------+------------+-----------+-------+

2. Memory
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+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |  0   |   0   |     0      |    140    |  0.00 |
|   RAMB36/FIFO* |  0   |   0   |     0      |    140    |  0.00 |
|   RAMB18       |  0   |   0   |     0      |    280    |  0.00 |
+----------------+------+-------+------------+-----------+-------+
```

Timing Report:

◀ Q  ⤦  ⇕  **Clock Summary**

| Name | Waveform | Period (ns) | Frequency (MHz) |
|------|----------|-------------|-----------------|
| axis_clk | {0.000 8.500} | 17.000 | 58.824 |

| **Setup** | | **Hold** | | **Pulse Width** | |
|-----------|---|----------|---|-----------------|---|
| Worst Negative Slack (WNS): | 1.274 ns | Worst Hold Slack (WHS): | 0.140 ns | Worst Pulse Width Slack (WPWS): | 8.000 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 528 | Total Number of Endpoints: | 528 | Total Number of Endpoints: | 124 |

All user specified timing constraints are met.

Simulation Waveform: