

Computer Architecture

Assignment 5 - Memory Hierarchy

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Answer 1

Assuming that:

$$\begin{array}{ll}
 \text{T avg seek} & 4ms \\
 \text{T avg rotation} & \frac{\text{T max rotation}}{2} = \frac{(60/15000) \times 1000}{2} = 2ms \\
 \text{T avg transfer} & \frac{60}{15000} \times \frac{1}{1000} \times 1000 = 0.004ms \\
 \text{T locate} & \text{T avg seek} + \text{T avg rotation} = 6ms
 \end{array}$$

Note,

$$m = \frac{2}{512} = 4000$$

Thus, the answers are:

A

$$T = T \text{ locate} + m * T \text{ avg transfer} = 22ms$$

B

$$T = m * (T \text{ locate} + T \text{ avg transfer}) = 24016ms = 24.016s$$

Answer 2

The Answer is the following table:

cache	m	C	B	E	S	t	s	b
1	32	1024	4	4	64	24	6	2
2	32	1024	4	256	1	30	0	2
3	32	1024	8	1	128	22	7	3
4	32	1024	8	128	1	29	0	3
5	32	1024	32	1	32	22	5	5
6	32	1024	32	4	8	24	3	5

Answer 3

The Answers are:

A given:

$$\begin{array}{ll} t & 0x45 = 0b01000101 \\ s & 0b001 \\ b & xx : x \in \{0, 1\} \end{array}$$

The address may be:

$$01000101 \ 001 \ xx$$

which would be formatted as:

$$0 \ 1000 \ 1010 \ 01xx$$

where the address range is between $0x08A4 - 0x08A7$. Furthermore:

$$t = 0x38$$

with an address range between $0x0704 - 0x0707$

B the range is:

$$0x1238 - 0x123B$$