Introduction to Digital Systems Design

ECEN 248 Spring 2020

Instructor:	Dr. Pierce Cantrell
Office:	Wisenbaker (WEB) Room 333D
Office Phone:	(979) 845–3719
Office Hours:	Monday 3:00–4:00 pm, Tuesday 9:00–10:00 am, Wednesday 3:00–4:00 pm, and Thursday 9:00–10:00 am; or make an appointment by calling 845-3719; or send e-mail to `p-cantrell@tamu.edu`
Class Meets:	Sections 200, 501–505, MWF from 10:20–11:10 am in ZACH Room 341
Course:	Introduction to Digital Systems Design, (3-3), Credit 4: Combinational and sequential digital systems design techniques; Design of practical digital systems.
Textbook:	Frank Vahid, *Digital Design with RTL Design, VHDL, and Verilog, 2nd Edition.* John Wiley & Sons, 2011. The textbook is required. Exams are open book and notes, but **no** electronics. You will have to print textbook sections for the exam if you have an electronic version of the textbook.
TA's:	TBA
Web Site:	Class notes, online homework, handouts, old exams, and the grade book will be found in the university's learning management system, eCampus. Go to `http://ecampus.tamu.edu` and login with your NetID/password. The class notes are either developed by the course instructor or derived from the original copyrighted notes of the textbook author.
Prerequisites:	MATH 152 with a grade of C or better; PHYS 207 or PHYS 208 with a grade of C or better or concurrent enrollment.

Grading: **Regular Sections**

Homework	10%
Laboratory	25%
Two Exams	20% each
Final Exam	25%

Grading: **Honors Section**

Homework	10%
Laboratory	25%
Honors Project	6%
Two Exams	18% each
Final Exam	23%

Grading scale: A (90-100), B (80-89), C (70-79), D (60-69), F(<60)

Learning Outcomes

Digital Systems are ubiquitous and significantly impact the way we live. A student who successfully fulfills the course requirements will have demonstrated the ability to convert desired system functionality into a digital design. Specific learning outcomes include the following: (1) ability to analyze and design combinational logic circuits, (2) ability to analyze and design sequential logic circuits, (3) ability to design high-level digital systems using Register-Transfer Level (RTL) design, and (4) utilize the Verilog hardware description language, logic simulation, and Field Programmable Gate Array (FPGA) technology to implement combinational, sequential, and RTL-based digital systems. A detailed daily syllabus with class-by-class topics and reading list is included at the end of this syllabus.

Exams and Final Exam

The two exams and the final exam will be open book and open notes. While the final exam will be cumulative, 70% of the final will be on material subsequent to the second exam (i.e., 3/23/2020 through 4/27/2020). **No electronic devices are allowed in Exam I. The only electronic device allowed during Exam II and the Final Exam is a calculator**. Please put your cell phone, smartphone, smartwatch, laptop, etc. in your backpack during the exam. The two exams will be in-class and are shown on the daily syllabus. The Final Exam is at the scheduled time for final exams.

Attendance and Makeup Policy

Attendance to class is optional. Please do your best to be present for the exams and the final exam. If you miss an exam or the final and have a *university excused absence*, you will need to schedule a makeup exam. If you do not have an excused absence, you will receive a zero unless there are extenuating circumstances. Please see me before the scheduled time for the exam if possible. I will expect written confirmation of a visit to a health care professional, affirming the date and time of the visit, for an injury or illness that requires you to be absent from an exam or the final. Please review the Student Rule on attendance `http://student-rules.tamu.edu/rule07`.

Homework

Homework will be assigned weekly, and it will all be online in eCampus. With the exception of the weeks of the first and second exams, I will accept late homework for up to one class period after the original due date (e.g., for homework due on Wednesday, you can submit late homework through Friday at 11:59 pm), but there will be a 10 point penalty (i.e., one letter grade). Homework due on Wednesday, February 12 and March 25 will *not* be accepted late due to Exam I and Exam II. I will post the homework solutions for these two assignments on Thursday, February 13 and March 26.

Academic Integrity

"An Aggie does not lie, cheat, or steal or tolerate those who do." Students are expected to be aware of the Aggie Honor Code and the Honor Council rules and procedures
(see `http://aggiehonor.tamu.edu`).

It is acceptable to discuss homework problems with your classmates, but the work you submit in eCampus should be your own and not a team effort.

ADA Statement

Texas A&M University is committed to providing equitable access to learning opportunities for all students. If you experience barriers to your education due to a disability or think you may have a disability, please contact Disability Resources in the Student Services Building or at (979) 845-1637 or visit `http://disability.tamu.edu`. Disabilities may include, but are not limited to attentional, learning, mental health, sensory, physical, or chronic health conditions. All students are encouraged to discuss their disability related needs with Disability Resources and their instructors as soon as possible.

Texas A&M University
Department of Electrical and Computer Engineering

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DATE	READ VAHID	TOPICS
M 1-13	1.1, 1.2	Intro to Digital Design; Digital vs Analog; Binary Numbers
W 1-15	1.2, 1.3	Binary Numbers (cont); Implementing Digital Systems
F 1-17	2.1–2.4	Combinational Logic; Switches; CMOS Transistors; Boolean Logic Gates
M 1-20		MLK Jr. Holiday - NO CLASS
W 1-22	2.4, 2.5, App A	Boolean Logic Gates (cont); Boolean Algebra
F 1-24	2.6, 2.7	Representing Boolean Functions; Combinational Logic Design Process
M 1-27	2.7, 2.8, 2.9	Comb. Logic Design Process (cont); More Gates; Decoders and Muxes
W 1-29	2.10, 6.1–6.2	Propagation Delay; Minimization
F 1-31	6.2	Minimization (cont)
M 2-3	4.1, 4.3, 6.4	Data Path; Adders; Incrementer; Faster Adders
W 2-5	6.4, 4.4–4.5	Carry-Lookahead Adder; Comparator; Multiplier
F 2-7	4.6	Subtractors and Signed Numbers
M 2-10	4.6, 4.7	Signed Numbers (cont); Arithmetic Logic Unit (ALU)
W 2-12	4.8, 7.1, 7.4	Combinational Shifter; 7400 SSI Logic; PLD's
F 2-14	**Exam I**	1/13–2/10 (Lecture 2/10 through slide 11) (CH 1, CH 2, App A, 6.2, 4.1, 4.3–4.6, 6.4)
M 2-17	3.1, 3.2	Flip-Flops
W 2-19	3.2, 4.2, 9.2	Flip-Flops (cont); Registers; Intro to Hardware Description Languages
F 2-21	9.2, Notes	Verilog – Combinational
M 2-24	9.3, Notes	Verilog – Simulation and Sequential
W 2-26	9.4, Notes	Verilog – Blocking/Nonblocking Guidelines; Datapath
F 2-28	3.3	Finite State Machines (FSM)
M 3-2	3.4	Controller Design
W 3-4	3.5, 6.3	Metastability; Flip-Flop Set-Reset; Glitches; Sequential Logic Opt
F 3-6	Notes, 6.3. 3.8	Max clock rate; State Encoding; Mealy and Moore FSM's; Pacemaker
M 3-9		Spring Break – NO CLASS
W 3-11		Spring Break – NO CLASS
F 3-13		Spring Break – NO CLASS
M 3-16	4.2, Notes	Shift Registers; Serial Transmission; Ethernet
W 3-18	4.2, 4.9	Multifunction Registers; Counters and Timers
F 3-20	4.10, 6.4, 5.1	Register Files; Smaller Multiplier; Register Transfer Language (RTL)

DATE	READ VAHID	TOPICS
M 3-23	5.2, 5.3	RTL Design; High-Level State Machines; RTL Design Process
W 3-25	5.3, 5.4	RTL Design Process (cont); More RTL
F 3-27	**Exam II**	2/10–3/20 (Lecture 2/10 slides 12-21; Lecture 3/20 through slide 12) (4.7, 4.8, 7.1, 7.4, CH 3, 6.3, 4.2, 4.9, 4.10, 6.4, Verilog)
M 3-30	5.4, 5.5, 5.6	More RTL (cont); RTL Max Clock Freq; RTL Behavioral Design
W 4-1	5.7	RAM; ROM
F 4-3	5.7, 5.8, 5.9	Flash; 3D-XPoint; FIFO's; Multiple Processors
M 4-6	5.10, 5.13, 6.5	Hierarchical Design; Cell Phone; RTL Design Optimization and Tradeoffs
W 4-8	6.5, 7.1, 7.2	RTL Design Opt (cont); Intro Manufactured IC Types
F 4-10		Reading Day – NO CLASS
M 4-13	7.2, 7.3	Intro Manufactured IC Types (cont); FPGA
W 4-15	7.3, 7.5	FPGA (cont); IC Tradeoffs
F 4-17	8.1, 8.2, 8.3	Programmable Processors – Basics and Three-Instruction Processor
M 4-20	8.4	Six-Instruction Programmable Processor
W 4-22	Notes	Error Detection in Digital Design
F 4-24	Notes	Error Correction in Digital Design; Design for Maintainability
M 4-27	Notes	Intro to Encryption and Authentication
T 4-28		Review for Final Exam (Redefined Day – Attend Friday classes)
M 5-4	**Final Exam**	8:00 am – 10:00 am