COMPUTER ENGINEERING & SYSTEMS GROUP

Follow Us!

Loading

Home

ECEN 350: Computer Architecture and Design - Spring 2019

Spring 2019

Credits: 4

Instructor Information:

Name: Dr. Paul V. Gratz
Email address: pgratz@gratz1.com
Office location: WERC 333M
Office hours:
TBD
Otherwise by apt. (send email 24 hours ahead of time)

TA Information:

TBD

Meeting Times and Locations:

All Lectures will be held in ZACH 241
All Recitations will be held in ZACH 241
Labs will be held in ZACH 333
Lecture, Lab and Recitation times vary dependent upon section number as shown in howdy.

Course Description:

Computer architecture and design; use of register transfer languages and simulation tools to describe and simulate computer operation; central processing unit organization, microprogramming, input/output and memory system architectures. Cross-listed with CSCE 350.

Prerequisite:

ECEN 248 – Introduction to Digital Systems Design.

Course Outcome:

The goal of this course is to provide the student with a working knowledge of different methods for logic representation, manipulation, and optimization, for both combinational and sequential logic. At the end of the course the student should be able to view the design of digital systems from a new perspective and have an understanding of several fundamental concepts that can be applied to a wide variety of digital design problems.

Textbook and/or Resource Material:

Required:
David Patterson and John Hennessy, “Computer Organization and Design: The hardware/software interface”, ARM EDITION, 2017.
(**note: no other edition is usable for this class as older textbooks use the MIPS ISA not the ARM ISA**)
Supplemental texts:
“Starter’s Guide to Verilog 2001” by M. Ciletti, Prentice Hall; illustrated edition (September 29, 2003);
“A Verilog HDL Primer” by J. Bhasker, Star Galaxy Publishing; 3rd edition (January 2005);

“Verilog HDL” by S. Palnitkar, Prentice Hall, 2 edition (March 2003).

Grading Policies:

Breakdown:

Exams (2 Exams)	50%
Labs	35%
Quizzes	15%

Grading Scale:

- Electrical & Computer Engineering Department Webpage
- Texas A&M University Access Policy
- Texas A&M University Webpage

Return to top of page

A: 90-100%
B: 80-89%
C: 70-79%
D: 60-69%
F: 0-59%

(note: in the event that the average overall grade of all students lies below a 79% there will be a curve on the overall grade. I will not curve the individual exams and assignments.)

Computer Engineering & Systems Group
Department of Electrical & Computer Engineering
Texas A&M University
333E WERC, College Station, Texas, 77843-3259
Phone (979) 458-5005, Fax (979) 845-2630

Individual Course Objectives:

At the end of this course, students should:

- Understand the organization of a computer system including the CPU datapath, CPU control, and memory systems
- Understand the impact of semiconductor technology on computer design and architecture.
- Understand the basics and principles of instruction set design.
- Be familiar with programming using an assembly level language.
- Understand the impact of instruction sets on hardware design.
- Be familiar with designing datapaths for a processor.
- Understand the implications of branch instructions on program flow and hardware design.
- Understand the performance implications of various factors such as clock speed, average clock cycles per instruction and number of instructions.
- Understand the role of compilers and high-level languages in programming.
- Be familiar with designing control circuitry for a basic processor.
- Understand the differences in single-cycle/multicycle design of processors.
- Be familiar with processor pipelining.
- Understand the implications of pipelining on memory design, instruction set design, compiling, performance etc.
- Understand the implications of branch instructions on pipelining.
- Understand basics of memory technology, registers, SRAM, DRAM.
- Understand the performance issue of various memory technologies.
- Be familiar with the notion of locality.
- Understand the memory architectures including cache architectures.
- Be familiar with various cache architectures: direct-mapped, set-associative, wide/narrow block size etc.
- Understand the concepts of virtual memory.
- Be familiar with the need for address translation.
- Understand the impact of address translation on cache/memory accesses.
- Be familiar with hardware designs of various cache architectures.
- Understand the basics of Input/Output.
- Understand the principles of instruction-level parallelism (ILP) and processor microarchitectures which exploit it.
- Understand the principles of thread-level parallelisms and processor microarchitecture which exploit it.
- Understand register-transfer level (RTL) system concepts and description methods, including a hardware description language (VERILOG)

Exams:

There will be two exams. The second exam will be cumulative, but with an emphasis on the material covered since the first exam. **All tests are open-book, open notes.**

Tentative Test schedule:
Exam 1 – in class, 3/7/19 (tentative)
Exam 2 – in class, 4/25/19

Course Topics/Schedule:

Hours: Topic
3 hours: Overview of Computer Architecture
3 hours: Instruction Set Architectures (ISA), Representing instructions on the computer, Arithmetical and logical instructions, Memory access instructions
3 hours: Instruction Set Architectures (ISA), Control flow instructions, Function calls instructions, Input-output instructions SPIM- instruction set simulator
3 hours: Computer Arithmetic, Signed and unsigned numbers, Addition and subtraction, Multiplication, Division, Floating point operations
3 hours: Translating and starting a program, Compilers, compiler optimization, Object code generation, assemblers, linking, Run-time execution environment
3 hours: Performance evaluation, CPU performance and its factors, performance metrics, performance factors, comparing performance, SPEC benchmarks
4 hours: Hardware Description Languages, Verilog hardware description language, Design-Simulation Process, Structural Designs in Verilog Behavioral HDL Description of Systems
3 hours: Datapath and Control, and ALU design
3 hours: Single-cycle implementation
3 hours: Microprogramming, catchup
3 hours: Pipelining, Pipelined datapath
4 hours: Pipelined control, Pipeline hazards: structural, control, data hazard detection and resolution, exception handling
4 hours: Memory Hierarchy, Overview of SRAM and DRAM design, Basic of caches, Framework for memory hierarchy, Measuring memory performance

Lectures:

All lectures will be recorded live during the lecture class period. The recordings will be broken up into individual, subject-oriented, videos and uploaded to the eCampus website for on-line viewing and review. A limited number of “online-only” lectures on special topics will also be made available.

Assignments/Quizes:

Rather than traditional homework, this course will rely upon a series of on-line quiz assessments. The goal of these quizzes will be to test your knowledge of the lecture material and pinpoint which lectures you should go back and review on-line. There will be one quiz for each lecture, this quiz must be completed prior to the next lecture. Students may retake the quiz as many times as desired between its release and the next lecture, however no late quizzes will be accepted.
The TAMU eCampus system will be used for all quiz and Lab submissions.
The two lowest quiz grades will be dropped.

Recitations:

Recitations will cover material from lectures and laboratories. Recitations will be conducted by a TA, and the professor will coordinate with the TA about the material to be covered in recitation for any given week. In recitation, answers to the last three quizzes will be discussed in detail. Other topics related to the weeks’s material will also be discussed.

Other Pertinent Course Information:

Excused absences:

Rules concerning excused absences may be found at http://student-rules.tamu.edu/rule07. In particular, except for absences due to religious obligations, the student must notify his or her instructor in writing (acknowledged e-mail message is acceptable) prior to the date of absence if such notification is feasible. In cases where advance notification is not feasible (e.g., accident, or emergency) the student must provide notification by the end of the second working day after the absence. This notification should include an explanation of

why notice could not be sent prior to the class. If the absence is excused, the instructor must either provide the student with an opportunity to make up any quiz, exam or other graded activities or provide a satisfactory alternative to be completed within 30 calendar days from the last day of the absence.

Days of religious observance:

By state law, if a student misses class due to an obligation of his or her religion, the absence is excused.

Americans with Disabilities Act (ADA):

The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact Disability Services, in Cain Hall, Room B118, or call 845-1637. For additional information visit http://disability.tamu.edu

Academic Integrity:

“An Aggie does not lie, cheat, or steal, or tolerate those who do.”
Upon accepting admission to Texas A&M University, a student immediately assumes a commitment to uphold the Honor Code, to accept responsibility for learning and to follow the philosophy and rules of the Honor System. Students will be required to state their commitment on examinations, research papers, and other academic work. Ignorance of the rules does not exclude any member of the Texas A&M University community from the requirements or the processes of the Honor System. For additional information please visit: http://aggiehonor.tamu.edu/
On all course work, assignments, and examinations at Texas A&M University, the following Honor Pledge shall be preprinted and signed by the student:
“On my honor, as an Aggie, I have neither given nor received unauthorized aid on this academic work.”
Remember that plagiarism will not be tolerated and will be dealt with under the Aggie Honor System Office guidelines.

Suggestions:

Suggestions for improvement are welcome at any time. Any concern about the course should be brought to the instructor’s attention.