Published in IET Circuits, Devices & Systems
Received on 23rd November 2010
Revised on 12th May 2011
doi: 10.1049/iet-cds.2010.0399

ISSN 1751-858X

Twelve-bit 20-GHz reduced size pipeline accumulator in 0.25 μm SiGe:C technology for direct digital synthesiser applications

B.S. Jensen[1] *M.M. Khafaji*[2] *T.K. Johansen*[1] *V. Krozer*[3] *J.C. Scheytt*[2]

[1]*Department of Electrical Engineering, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark*
[2]*IHP Microelectronics GmbH, 15236 Frankfurt (Oder), Germany*
[3]*Terahertz Photonics, Johann Wolfgang Goethe University, 60438 Frankfurt (Main), Germany*
E-mail: bsj@elektro.dtu.dk

Abstract: This article presents a 20 GHz, 12-bit pipeline accumulator with a reduced number of registers, suitable for direct digital synthesiser (DDS) applications. The accumulator is implemented in the IHP SG25H1 (0.25 μm) SiGe:C technology featuring heterojunction bipolar transistors (HBTs) with F_t/F_{max} of 180/220 GHz. The accumulator architecture omits the pre-skewing registers of the pipeline, thereby lowering both power consumption and circuit complexity. Some limitations to this design are discussed and the necessary equations for determining the phase jump encountered each time the control word (synthesised frequency) is changed are presented. For many applications employing signal processing after detection, this phase shift can then be corrected for. Compared to a full pipeline architecture (omitting the input circuitry for the most significant bit, as is customary for such designs), the implemented 12-bit accumulator reduces the number of registers by 55% and the power by approximately 32%, while obtaining the highest clock frequency for SiGe:C accumulators intended for DDS applications.

1 Introduction

Direct digital synthesisers (DDS) are becoming increasingly attractive alternatives to analogue-based phase-locked-loop (PLL) synthesiser counterparts, because of their agility and broadband performance. Compared to PLL techniques, the DDS offer higher-frequency output range (ideally from DC to half the clock frequency, F_{clk}), higher frequency switching speed and greater stability. However, they also have a high number of spurious output components because of the periodic nature of the digital implementation, [1]. Recently, DDS designs running at clock frequencies of up to 32 GHz have been reported in the literature, for example [2–5]. Although requiring large amounts of power and high production costs, these designs have been manufactured in Indium Phosphide (InP) Double-Heterojunction Bipolar Transistor (DHBT) technologies where the cut-off frequency is high because of the high carrier mobility. Recent advances in SiGe:C technologies have yielded heterojunction bipolar transistor (HBT) devices with f_T/f_{max} in the vicinity of 300 GHz [6], while still maintaining low power consumption. Using such technologies for DDS applications yields high levels of integration and the possibility to include Complementary metal-oxide-semiconductor (CMOS) circuits on the same chip. Therefore lately very fast SiGe:C technologies have been utilised to lower the power consumption and die area of DDS ICs, for example [7–10]. However, until now, some of the fastest SiGe:C DDS ICs have been limited to clock frequencies of about 15 GHz.

A simplified block diagram of a standard DDS design utilising a phase increment counter (accumulator) and a look-up table (LUT) containing the sine wave samples, is shown in Fig. 1. Although the counting speed of the accumulator is set by the clock frequency, the so-called frequency control word (FCW) at the input sets the count increment of the accumulator and thereby the synthesised output frequency, according to

$$F_{out} = \mathrm{FCW} \cdot \Delta F, \quad \Delta F = \frac{F_{clk}}{2^j} \tag{1}$$

where ΔF is the frequency resolution of the DDS and j is the number of bits in the phase accumulator. Note from Fig. 1 that only the k most significant bits (MSB) are used for the LUT indexing. This truncation of the accumulator output word is used to reduce LUT size and will result in some higher spurious components, as described in Section 3.1. At higher clock frequencies, to maintain the DDS resolution, that is, small frequency steps, the number of accumulator bits, j, should be increased. This in turn, will increase the overall power consumption and complexity of the DDS.

Many publications have sought to reduce the power consumption of the DDS; however, most of these publications address gate-level designs and/or special techniques to lower the size of the LUT, which traditionally

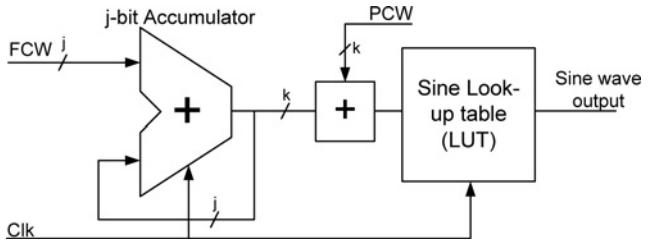

Fig. 1 *Simplified block diagram of a standard DDS architecture*

A j-bit accumulator counts the phase, while the k most significant output bits are used for indexing the sine LUT. FCW controls frequency and PCW modulates phase

has been implemented as a memory block containing the sine-wave samples and connected at the output to a linear digital-to-analogue converter (DAC). Two architectures, [8, 11], reduce the power consumption of the LUT considerably. In [8] and also later in [5], the memory block and the linear DAC were replaced with a sine-weighted DAC. However, a weighted DAC design is often more complicated and will often consume more power than a linear one, so in [11] yet another architecture was considered (Fig. 2). Here the MSB of the accumulator inverts all the bits to produce a digital triangle waveform instead of the normal ramp waveform. The LUT is then implemented with a linear DAC and a bipolar differential pair as the triangle-to-sine wave converter, [12].

In [13], it was sought to lower the accumulator power consumption by implementing a pipelined split-accumulator architecture and a special pre-skewing scheme for the pipeline registers.

This work considers the feasibility of completely removing all pre-skewing registers in the pipeline accumulator. This implementation has been suggested before, [14], however, without considering in detail the consequences and the exact relationship between the switching of the FCW and the associated phase jump. Here a mathematical treatment is given together with a discussion of the benefits and drawbacks of this implementation and a reduced size 20 GHz 12-bit accumulator suitable for use in the DDS architecture of Fig. 2 is presented.

In the next section the reduced-size accumulator is introduced and the equations for determining phase jumps associated with a change of synthesised frequency are presented. Furthermore, the circuit reduction and associated lowering of the power consumption is presented. Sections 3 and 4 then discuss the design of the implemented accumulator IC and the measurements carried out, respectively. Finally, Section 5 gives the conclusion.

2 Pipeline accumulator without pre-skew registers

For high-speed operation the accumulator is implemented as a pipeline accumulator in which registers are used to pre- and post-skew the input- and output data, respectively. An example of a 5-bit pipeline accumulator is given in Fig. 3. It can be seen that once the accumulator has been operated for K_{flush} clock cycles corresponding to the number of pipeline stages (e.g. six clock periods for the 5-bit example), the output becomes valid (O_{ACC} increments with a steady rate) and the pre-skewing registers are not changed before the FCW is updated again. The post-skewing registers are important for aligning the output data to the LUT. If a phase jump, $\Delta\Phi_{\text{err}}$, can be allowed each time FCW changes, the pre-skewing registers can be omitted to save power and reduce circuit complexity. The synthesised frequency, after changing FCW, will be the same as in the traditional DDS, once the accumulator has settled. Traditionally, this approach has been avoided, because some applications do not tolerate a non-continuous phase, thereby losing the ability for the DDS design to be an all-purpose building block. However, as will be discussed next, for many applications this phase jump is in fact not a problem.

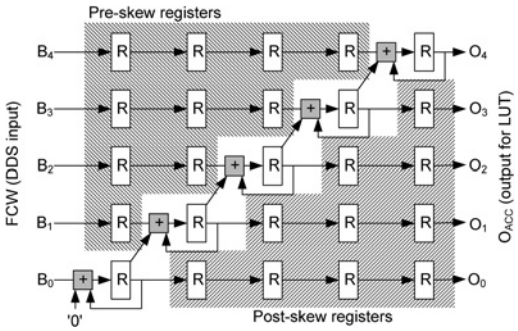

Fig. 3 *Example of 5-bit standard pipeline accumulator for use in DDS*

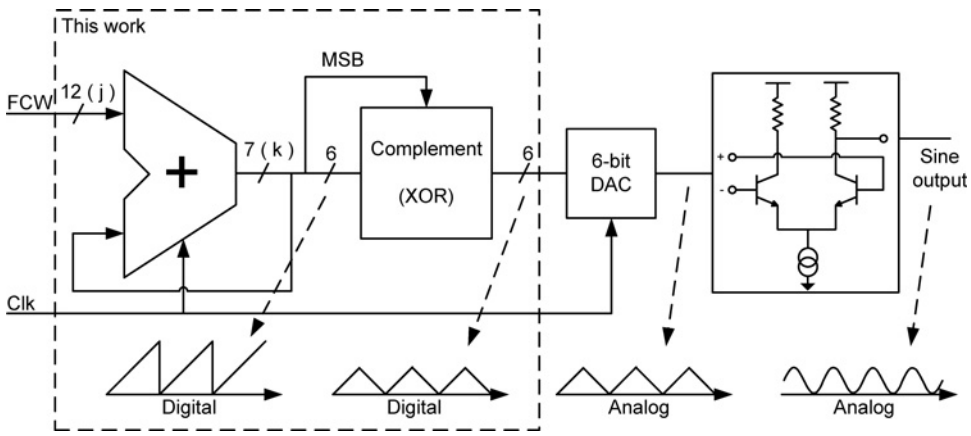

Fig. 2 *DDS architecture that reduces power consumption by implementing the LUT as a linear DAC connected at the output to a differential bipolar pair for triangle-to-sine conversion, as described in [11]*

Chip implemented in this work includes the 12-bit accumulator and the complement circuit (XOR) for digital ramp-to-triangle conversion

doi: 10.1049/iet-cds.2010.0399

The use of DDS-type local oscillators (LO) in transceiver systems enables fast switching (multiplexing) between different frequency bands and reduction in complexity, as the DDS allows both the frequency and the phase to be directly modulated. Most receiver types receiving either amplitude-, phase- or frequency-modulated (AM, PM and FM, respectively) signals, employ a constant LO frequency and thus can use the DDS as LO. For transmitters employing amplitude modulation schemes, such as single- or double-sideband AM, quadrature amplitude, amplitude shift keying etc. where frequency and phase of the LO are constant during up- and down conversion, the use of the reduced-size DDS as LO is also allowed. The standard implementation of phase modulation in DDS designs is indicated in Fig. 1. Here a phase control word (PCW) is added to the accumulator output. As a result, once the frequency is stable after a change in FCW, the DDS can directly be used for standard phase modulation types such as simple PM, phase shift keying (PSK), quadrature PSK, continuous phase modulation etc. If the DDS is to be used for frequency modulation in transmitters, only frequency shift keying (FSK) will operate correctly, as this is the only frequency modulation scheme that does not require a continuous phase, as does simple FM and continuous phase FSK. The only exception to this is in transmitters used for radar applications. If the value of a phase jump created by switching the DDS frequency can be determined, then radar applications monitoring phase and/or frequency can use the DDS for frequency chirps and then correct for the jumps in the signal processing part of the receiver.

2.1 Phase jump determination

Imagine that the pre-skewing registers in Fig. 3 for the 5-bit accumulator are omitted. Each time the FCW is changed, the input bits to the five adders are not aligned. In fact, all bits except for the least significant bit (LSB), B_0, will reach the adders too soon, creating a jump in the accumulator output value, O_{ACC}. Based on the frequency setting before and after the switching, FCW_1 and FCW_2, respectively, the jump of the accumulator output, ΔO_{ACC}, can be determined as follows

$$\Delta O_{\mathrm{ACC}} = \sum_{n=0}^{j-1} n(B_{n,2} - B_{n,1})2^n \tag{2}$$

where $B_{n,x}$ represents bit n in FCW_x. The equation states that each bit, corresponding to a specific value (i.e. $2^3 = 8$ for B_3) will add to the counter jump, ΔO_{ACC}, according to the missing delay in front of the adders. For example, depending on whether B_3 changes upwards (0 to 1) or downwards (1 to 0), and because this bit is missing three delays, the accumulator will count three times 2^3 (i.e. in total 24) too much, or too little, respectively. It is important to note that (2) does not say anything about the value during the switching, that is, before the pipeline has been flushed (K_{flush} clock cycles have passed). It only determines the steady-state counting error. Now, as the phase resolution of the DDS is determined by $\Delta\Phi = 2\pi/2^j$ it is possible to find the phase jump, $\Delta\Phi_{\mathrm{err}}$, as follows

$$\Delta\Phi_{\mathrm{err}} = \Delta O_{\mathrm{ACC}}\Delta\Phi = \frac{\Delta O_{\mathrm{ACC}}}{2^{j-1}}\pi \tag{3}$$

Note that (3) sometimes predicts phase jump values outside the range $[-2\pi, 2\pi]$. As these values do not have physical influence on the output after LUT and digital-to-analogue conversion, such phase jumps should be wrapped to be within the range $[-2\pi, 2\pi]$. Fig. 4 shows an Agilent Ptolemy simulated discrete-time waveform example of a 12-bit DDS using 7 bits for LUT indexing. The initial phase difference between the waveform of the reduced-size design and the traditional design is due to the initial skew created during start-up of the circuits. At sample 2500, FCW is changed from 32 to 300, which is seen to result in not only higher frequency but also a phase jump ($\Phi_1 < \Phi_2$) simulated to be $\Delta\Phi_{\mathrm{err}} = \Phi_2 - \Phi_1 = 3.24$ rad. Using (3) we obtain $\Delta\Phi_{\mathrm{err}} = 3.19$ rad. The difference between the simulation and the calculation is owing to the finite precision caused by the truncation of the five LSBs.

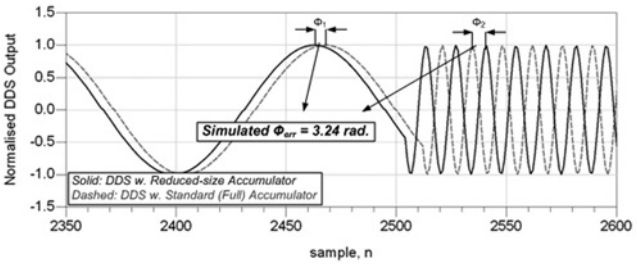

Fig. 4 *Simulated output waveform of a 12-bit DDS using the seven MSBs from the accumulator for LUT indexing*

Number of samples across 2π radians is different for the two cases of FCW values

2.2 Circuit reduction

As is also indicated in Fig. 1, many high-speed high-resolution DDS designs truncate some accumulator LSBs to reduce the LUT size. Furthermore, as a DDS can only synthesise up to the Nyquist frequency (half the clock frequency), the pre-skewing registers for the MSB are omitted. The input for this bit is then internally biased to a logic low value. When compared with a full pipeline design employing these standard circuit reductions, the 12-bit accumulator presented here reduces the number of registers from 105 to 50. Furthermore, this reduction also lowers the requirement to the clock tree and thus clock buffers; so in total the power reduction is approximately 32%.

3 Accumulator design

The accumulator is implemented in the IHP SG25H1 (0.25 μm) SiGe:C technology, [15], using a traditional pipeline design with 1-bit adders for maximum speed, as shown in Fig. 5. Note that the MSB output of the accumulator core controls the Exclusive-Or (XOR)-gates at the remaining outputs to create the complement function indicated in Fig. 2 and thus to create triangle waveforms. In the following, some of the most important design choices will be discussed.

3.1 Frequency- and phase resolution for DDS application

The design of the accumulator is driven by a desire to have a frequency synthesiser able to synthesise up to some 10 GHz signals with a frequency resolution, ΔF, better than 6 MHz. Using $j = 12$ in (1) we obtain $\Delta F = 4.9$ MHz.

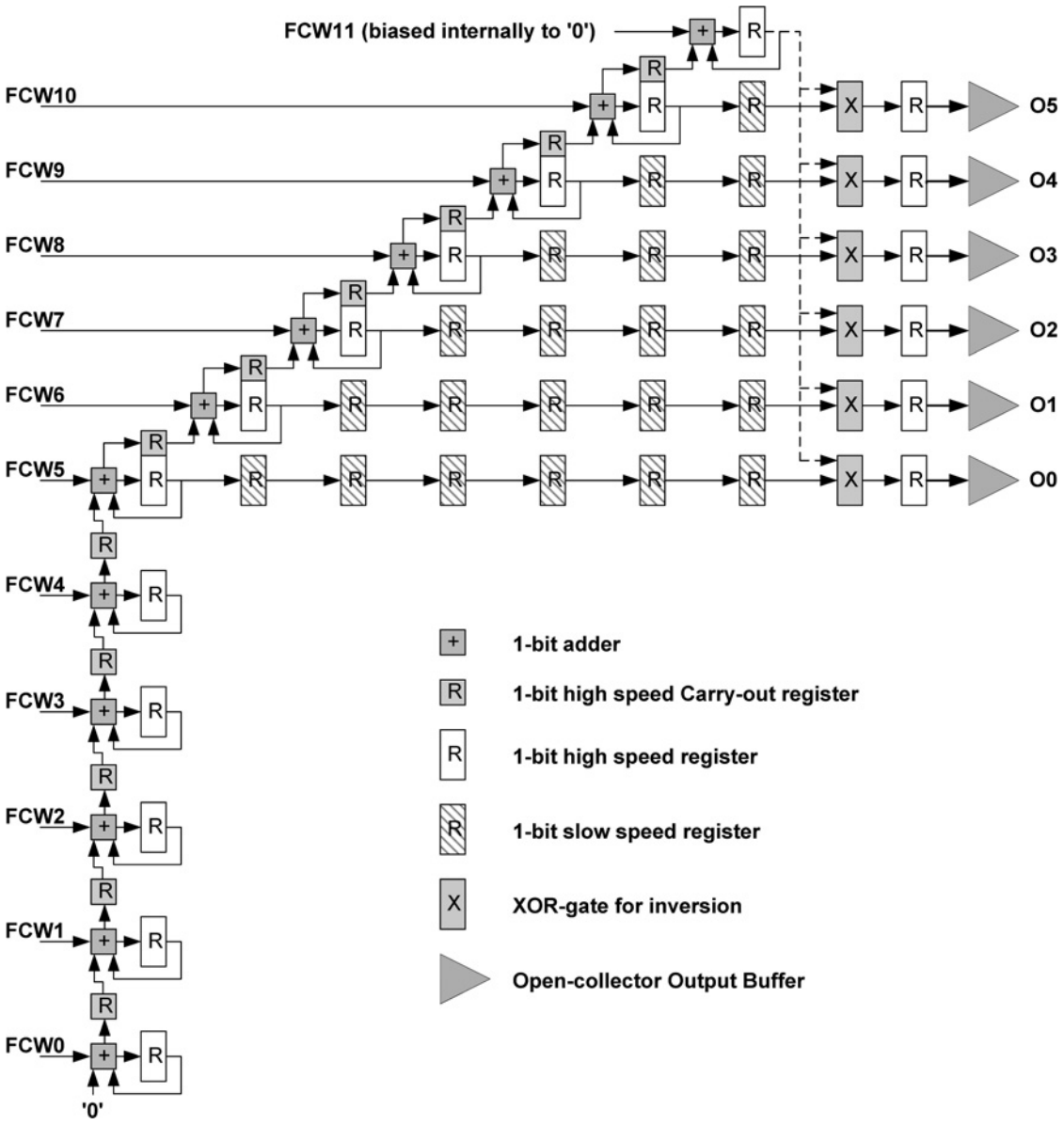

Fig. 5 *Block diagram of the reduced pipeline accumulator*

All registers are clocked at the same time, as discussed in Section 3.3 on the clock tree

One of the drawbacks of a DDS, compared to a PLL, is that many spurious frequencies are created because of the periodic nature of a counting accumulator. The spurious free dynamic range (SFDR) of a DDS using k bits for sine-wave look-up (see Fig. 2) can be estimated by [16]

$$\text{SFDR} \simeq 6.02k - 3.992 \text{ (dB)} \tag{4}$$

So for a DDS implemented with the accumulator presented here with $k = 7$ we should expect SFDR $\simeq$ 38.15 dB. Note that (4) do not take into account the effect of DAC non-linearity and the finite number of amplitude bits, which contribute to the creation of spurious frequencies, as well.

3.2 SiGe differential emitter-coupled logic (DECL) gates

In order to reach the desired clock speed of 20 GHz, the accumulator is implemented with DECL. As DECL is of the non-saturation-type logic with a more or less constant current in each cell (i.e. small difference between dynamic and idle current) the power consumption is high compared to other types of logic.

The DECL sum-output and carry-output gates used for the 1-bit adders are shown in Fig. 6. The sum-output circuit is implemented with two cascaded XOR-gates whereas the carry-output circuit is implemented as a majority gate [17] in which the total current in the cell is divided among three parallel differential bipolar pairs acting as the inputs. All gates in the pipeline core, that is, XOR-gates and latches for the registers, Figs. 6*b* and *d*, operate with a single-ended internal signal swing of 200 mV. The only exception is the majority gate in Fig. 6*c*, which uses a 400 mV signal swing. The reason for this is that whenever two of the inputs have the same logic value, and the third is not equal to those, the signal swing will be reduced to one-third of the maximum swing encountered when all inputs are the same – what will here be referred to as the nominal swing. For a 200 mV nominal swing this would mean that the reduced swing would be only 67 mV which is not desirable as it approaches the thermal voltage. Instead, for a swing of 400 mV the reduced swing is 133 mV.

doi: 10.1049/iet-cds.2010.0399

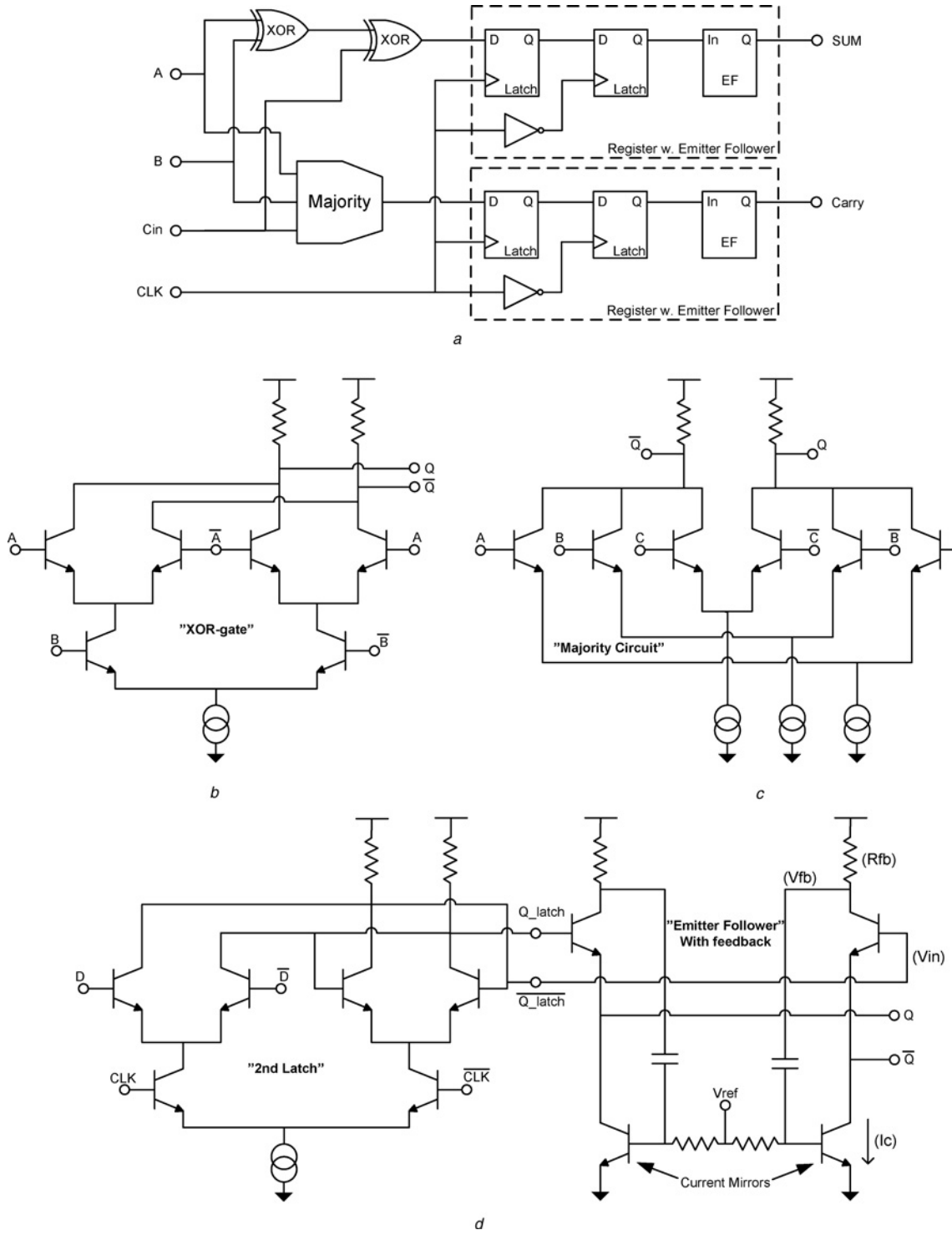

Fig. 6 *DECL gates used in the 1-bit adder circuits*

a Block diagram of the adder
b XOR-gate used for sum-output circuit
c Majority gate used for carry-output circuit
d Second latch and the output EF with feedback used for the fast registers

Two different latches have been designed for use in pipeline registers – a fast one and a slow one, as indicated in Fig. 5. The fast one is needed at the outputs of the adders, see Fig. 6*a*, where they have been optimised to be able to latch the signals going through the calculation circuitry. The low-speed latch is used for post-skewing registers as no calculations are needed in between these. As speed is proportional to current, this reduces power consumption.

Fig. 6*d* shows the last of two latches used for the fast registers together with an emitter follower (EF) on the output. The latch design is rather standard DECL; however, the EF includes feedback through capacitors to facilitate a small amount of peaking. When the input (V_{in}) to the EF decreases, the current in the EF, and thus the voltage drop across the feedback resistor, R_{fb}, becomes lower. The result is that the feedback voltage, V_{fb}, and thus the current drawn through the current mirror, I_c, becomes higher. This helps

discharging any capacitive loading caused by the next stage. On the other hand when the input increases, the current through the current mirror is lowered, which means that more current is allowed to flow to the capacitive load. As seen from the schematic, the EF current mirrors do not use resistors on the emitter for degeneration, as this would counteract the feedback action. All other current mirrors on the chip use approximately 200 mV drop over the degeneration resistors.

DECL gates use EFs at the outputs not only to drive subsequent circuitry but also to lower the signal level to match that of the next gate. However, EFs are extremely power hungry, and so for all gate outputs that only drive one subsequent gate, the EF is omitted. As can be seen from, for example, Fig. 6 this means that for the subsequent gate, the input HBTs (input A in Fig. 6*b*) will have their base–collector junction slightly forward biased because of the base having a higher potential than the collector. However, the associated reduction in speed is not significant for such low signal swings and the extra current needed to overcome this speed reduction is often much less than that needed for driving two EFs at the differential output.

3.3 Clock tree

For circuits operating at multi-GHz frequencies it is important that clock skew, either positive or negative, is controlled very carefully. Negative clock skew, as defined in [18] can be used to speed up pipeline circuits; however, if the negative clock skew is more than the signal delay through each digital block, the pipeline becomes ineffective in that the signals will be swept through the registers rather than being latched. Positive clock skew, on the other hand, will make the circuit slower. In order to be able to control the clock skew precisely, the three-level clock tree shown in Fig. 7 has been implemented. As shown, each clock buffer in a given level drives exactly the same number of buffers or registers, making all the clock signals arriving to the registers at the same time. The clock tree has been laid out

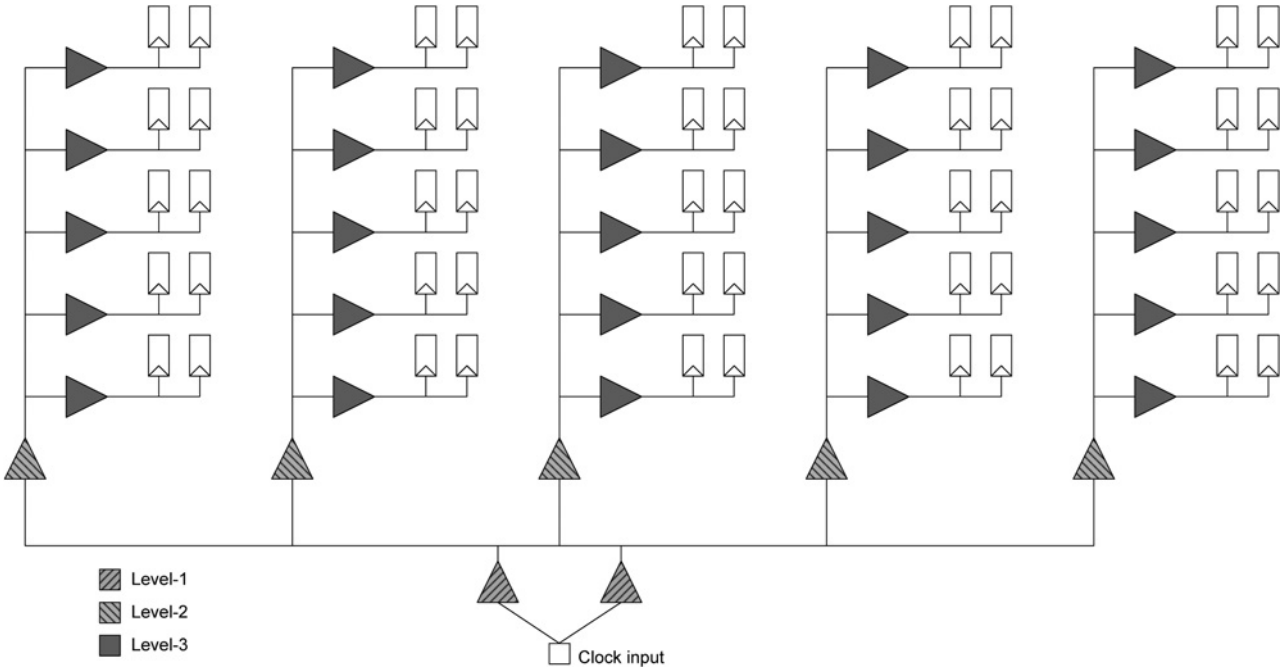

Fig. 7 *Block diagram of the three-level clock tree implemented for the pipeline accumulator*

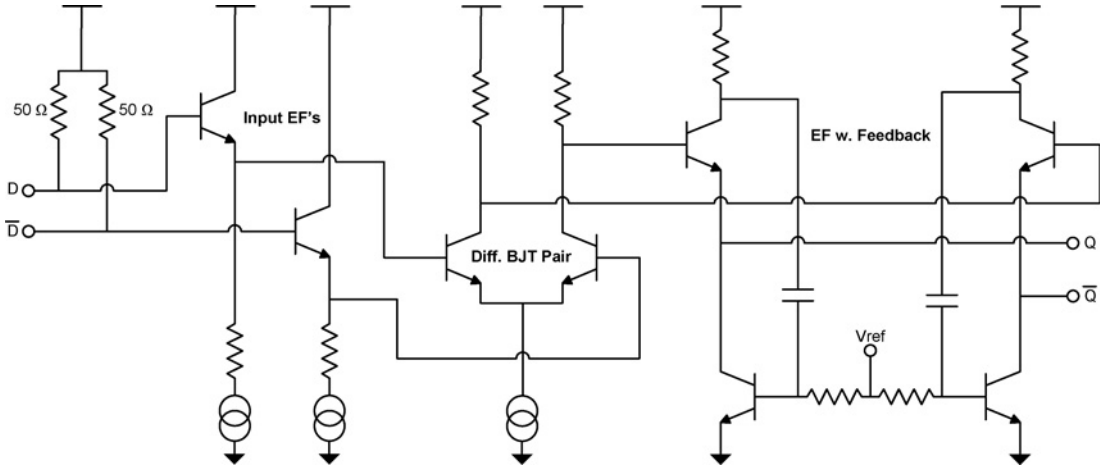

Fig. 8 *Input differential clock buffer mathed to 50 Ω and with output EF stage for high drive capability*

doi: 10.1049/iet-cds.2010.0399

carefully to ensure that lines have the same length, thereby minimising skew because of unequal travel paths.

Fig. 8 shows the input clock buffer, which deviates slightly from the internal clock buffers in that it includes an input EF stage with 50 Ω matching resistors connected to V_{CC}. Internal buffers omit this EF stage and matching resistors and take the input signal directly from the buffer in front of it. All clock buffers have a powerful output EF to drive the high loading created by the subsequent buffer stages and registers. These EF stages use the same feedback scheme as was used in Fig. 6*d* for the high-speed latch output.

3.4 Output buffers

When the accumulator is to be integrated on the same chip together with a linear DAC and a bipolar pair as the triangle-to-sine converter to form a complete DDS, no output buffers are needed for the accumulator itself. However, to test the accumulator separately, output buffers are needed. Each output is therefore equipped with an open-collector differential buffer, see Fig. 9, designed to deliver a 300 mV single-ended swing across a 50 Ω load resistor. This design is chosen as the preceeding circuitry – whether being test equipment or a high-speed DAC – is often equipped with 50 Ω input matching resistors, across which a current can be drawn. The current through the open-collector differential pair is approximately 6 mA which is high compared to all other current switches in the design; so to be able to drive the output stage, an EF is added to the input of the output buffers as indicated in the figure. As seen, the topology of this EF again follows that of the output for the fast latches and the clock buffers, Figs. 6*d* and 8, respectively.

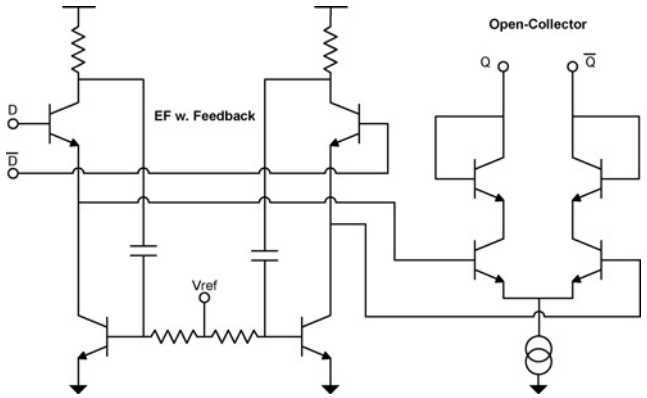

Fig. 9 *Differential open-collector output buffer with input EF implemented to be able to test the accumulator seperately*

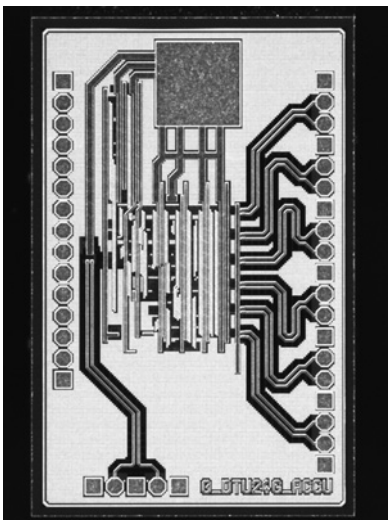

Fig. 10 *Photograph of the 12-bit accumulator die*
Chip size is 2.25 × 1.43 mm

3.5 Final accumulator IC

A photograph of the final accumulator IC is shown in Fig. 10. The IC measures 2.25 × 1.43 mm with an accumulator core area of approximately 0.66 mm^2. The core includes a total number of around 4500 transistors. The measured core power consumption is approximately 1.08 W without including the output buffers as these will be omitted when the accumulator is to be integrated with a DAC in a final DDS design.

4 Measurements

The accumulator IC has been measured on-wafer with a Tektronix TDS 6154G digital storage oscilloscope for real-time voltage curve measurements. Only one output bit was measured at a time while the remaining ones were connected directly to VCC. The monitored output is taken on-wafer with a *Z*-probe and fed through a bias-*T* where the DC connection is connected to supply and the AC-connection is connected to the oscilloscope which is internally matched to 50 Ω. The test set-up limits the clock frequency to about 20 GHz.

4.1 Output waveforms and power consumption

The simulated current at 3.0 V supply voltage was approximately 325 mA, however, when the IC was measured, the current at 3.0 V supply was only 284 mA. All current mirrors are internally biased (no external reference pin); so to reach the desired supply current and thus speed of the IC, the supply voltage had to be increased to 3.27 V, thus increasing the power consumption from the simulated 975 mW to approximately 1.08 W.

Fig. 11 shows output curves from the LSB for three different settings of FCW, that is, FCW = 2, 4 and 8. For all the presented output curves, the inverting/complement

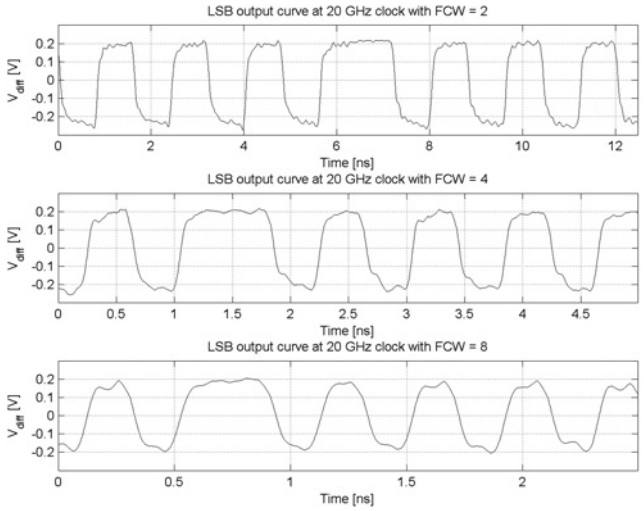

Fig. 11 *Measurements of LSB output at a clock frequency of 20 GHz for three different FCW settings (FCW = 2, 4 and 8)*
LSB is monitored with a Tektronix digital storage oscilloscope while remaining outputs are connected directly to VCC

Table 1 Measured LSB output frequencies and peak-to-peak voltages

FCW	Fund. freq. from oscilloscope data, MHz	Expected feq., MHz	Output diff. swing V_{PP_LSB}, mV
1	312.6	312.5	564
2	625.8	625	534
4	1259	1250	492
6	1887	1875	482
8	2513	2500	412
10	3175	3125	400
12	3745	3750	399
16	4975	5000	371

function (recall from Fig. 2) is captured to illustrate the functionality of the output XOR-gates. Table 1 shows a list of measured LSB output frequencies together with the differential peak-to-peak voltage, V_{PP_LSB}, for various different FCW settings. The fundamental frequencies have been obtained through the use of Matlab, by applying the auto-correlation function to the raw output data of the oscilloscope. By comparing the measured frequency with the expected frequency from simulations with Spectre Cadence, the functionality of the accumulator core can be verified. As seen from Table 1 the measured frequency is very close to the expected one for all respective FCW settings, verifying accumulator core operation. The small frequency differences observed in Table 1 are expected to be caused by the finite number of time-domain periods used in calculating the frequency. This calculation error naturally becomes more significant at higher frequencies as they are closer to the sample rate of the oscilloscope. Note that because of phase bit truncation, the LSB is in fact output bit number 6 from the accumulator, which explains why it is expected that for FCW = 1 the LSB should switch with a frequency of $2^6 \cdot \Delta F = 312.5$ MHz. Only the MSB of the accumulator output (the one used for inverting the ramp) will switch at a frequency of $\simeq$4.9 MHz as stated earlier in Section 3.1 for the minimum frequency step size.

Furthermore, as can be seen from Fig. 11 and in Table 1, when the output switching frequency goes up the peak-to-peak voltage goes down. This is often seen in high-speed digital systems. However, already at FCW = 10 the differential peak-to-peak voltage is at 400 mV, that is, a reduction of 33% compared to the nominal 600 mV, indicating that the output buffers are not fully able to drive the long lines and bias-T's used for the current measurement set-up. As the output buffers were not designed to drive this kind of external circuitry, further measurements of the chip bonded on PCB and connected directly to a high-speed DAC will be conducted in the near future. The DAC used for such future measurements will probably be the newly developed 6-bit DAC from IHP, see [19].

4.2 Comparison

Table 2 shows a comparison between recently published papers and articles on DDS and/or accumulator ICs. Apart from [7], only DDS publications with specification of the accumulator power consumption have been considered. The figure of merit (FoM) used in Table 2 is given by

$$\text{FoM} = \frac{F_{\text{clk}} \cdot j \cdot k}{P_{\text{diss}}} \ (\text{GHz} \cdot \text{bits}^2/\text{W}) \tag{5}$$

Table 2 Comparison of recently published accumulators for DDS applications

Ref.	Techn.	J^a, bits	k^a, bits	F_{clk}, GHz	Power, W	FoM, (GHz bits^2/W)
[17]	InP	4	4	41	4.1	160
[5]	InP	8	5	32	4.9	261
[2]	InP	8	6	13	2.13	293
[8]	SiGe	8	8	5	0.495	646
[9]	SiGe:C	9	8	11	0.825	960
[10]	SiGe:C	9	8	12	0.825	1047
[3][b]	SiGe:C	9	9	6	0.308	1578
[7][b]	SiGe:C	8	6	15	0.366	1967
this work	SiGe:C	12	7	20	1.08	1557

[a]For j and k refer to Fig. 1

[b]Power consumption is for complete DDS IC

where j is the number of bits in the accumulator and P_{diss} is the dissipated power. Compared to previous reported FoMs this FoM also includes the effective number of bits, k, used for sine-wave look-up (refer to Fig. 2). This has been included because larger values of k will yield lower spurious signals (see Section 3.1) at the expense of a higher power consumption because of the requirement of more post-skew registers.

In [3, 7], only the power consumption of the complete DDS ICs are reported and even at this power consumption, they obtain higher FoMs. However, they do so at 70% and 25% lower clock frequencies, respectively. Furthermore, the frequency step size for [3] is 2.4 times larger (11.7 against 4.9 MHz) compared to the IC presented here, whereas that of [7] has a 12-times-larger step size (58.6 MHz against 4.9 MHz). Thus, the presented IC obtains one of the best FoMs among the reported accumulators and operates at the highest clock frequency among those integrated in SiGe:C technology.

5 Conclusion

This article presented a 20-GHz 12-bit pipeline adder accumulator integrated in IHP SG25H1 (0.25 μm) SiGe:C technology, intended for use in DDS applications. The seven MSBs of the accumulator output are used for the phase look-up operation of the DDS; however, only 6 bits are forwarded to the DAC, because the MSB is used for inversion of the counting operation to create a digital triangle output. In order to lower power consumption and circuit complexity, all the pre-skewing registers of the accumulator were omitted from the design. The benefits and drawbacks of this reduced pipeline architecture with respect to a DDS application have been discussed and equations for finding the resulting phase jump encountered when switching the control word (changing the synthesised frequency) are presented. Although the measurement facilities did not allow testing clock frequencies higher than 20 GHz, it can be concluded that this design is the fastest SiGe:C accumulator intended for DDS applications reported so far. The measured power consumption for the accumulator core is 1.08 W without including the output buffers as these will be omitted when the accumulator is to be integrated with a DAC in a final DDS design.

Further measurements of the chip bonded on PCB together with a high-speed DAC and a bipolar differential pair to form a complete DDS system will be conducted in the near future.

doi: 10.1049/iet-cds.2010.0399

6 Acknowledgments

The authors would like to thank IHP GmbH, Frankfurt (Oder), Germany, for making the 0.25 μm SiGe:C technology available and for a great deal of support during the development and testing of this new accumulator. Furthermore, we would like to thank IPtronics A/S, Roskilde, Denmark for their knowledge sharing and design suggestions during the initial development stages of the IC.

7 References

1 Vankka, J., Halonen, K.: 'Direct digital synthesizers: theory, design and applications' (Kluwer Academic Publishers, Dordrecht, The Netherlands, 2001)
2 Turner, S.E., Kotecki, D.E.: 'Direct digital synthesizer with ROM-less architecture at 13-GHz clock frequency in InP DHBT technology', *IEEE Microw. Wirel. Compon. Lett.*, 2006, **16**, (5), pp. 296–298
3 Thuries, S., Tournier, E., Cathelin, A., Godet, S., Graffeuil, J.: 'A 6-GHz low-power BiCMOS SiGe:C 0.25 μm direct digital synthesizer', *IEEE Microw. Wirel. Compon. Lett.*, 2008, **18**, (1), pp. 46–48
4 Turner, S.E., Chan, R.T., Feng, J.T.: 'ROM-based direct digital synthesizer at 24 GHz clock frequency in InP DHBT technology', *IEEE Microw. Wirel. Compon. Lett.*, 2008, **18**, (8), pp. 566–568
5 Turner, S.E., Kotecki, D.E.: 'Direct digital synthesizer with sine-weighted DAC at 32-GHz clock frequency in InP DHBT technology', *IEEE J. Solid-State Circuits*, 2006, **41**, (10), pp. 2284–2290
6 Rücker, H., Heinemann, B., Winkler, W., *et al.*: 'A 0.13 μm SiGe BiCMOS technology featuring f_T/f_{max} of 240/330 GHz and gate delays below 3 ps', *IEEE J. Solid-State Circuits*, 2010, **45**, (9), pp. 1678–1686
7 Laemmle, B., Wagner, C., Knapp, H., Maurer, L., Weigel, R.: 'A 366 mW direct digital synthesizer at 15 GHz clock frequency in SiGe bipolar technology'. IEEE Radio Frequency Integrated Circuits Symp., 2009, pp. 415–418
8 Dai, F.F., Chimakurthy, L.S.J., Yang, D., Huang, J., Jaeger, R.C.: 'A low power 5 GHz direct digital synthesizer designed In SiGe technology'. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2004, pp. 21–24
9 Yu, X., Dai, F.F., Irwin, J.D., Jaeger, R.C.: 'A 9-bit quadrature direct digital synthesizer implemented in 0.18 μm SiGe BiCMOS technology', *IEEE Trans. Microw. Theory Tech.*, 2008, **56**, (5), pp. 1257–1266
10 Yu, X., Dai, F.F., Irwin, J.D., Jaeger, R.C.: 'A 12 GHz 1.9 W direct digital synthesizer MMIC implemented in 0.18 μm SiGe BiCMOS technology', *IEEE J. Solid-State Circuits*, 2008, **43**, (6), pp. 1384–1393
11 Thuries, S., Tournier, E.: 'A DDS-oriented phase-to-amplitude converter using a SiGe:C bipolar transistors differential pair'. IEEE Int. Workshop on Radio-Frequency Integration Technology, Singapore, 30 November–2 December 2005, pp. 211–214
12 Meyer, R.G., Sansen, W.M.C., Lui, S., Peeters, S.: 'The differential pair as a triangle-sine wave converter', *IEEE J. Solid-State Circuits*, 1976, **SC-11**, (3), pp. 418–420
13 Merlo, E., Baek, K.H., Choe, M.J.: 'Split accumulator with phase modulation for high speed low power direct digital synthesizers'. IEEE Proc. 15th Annual IEEE Int. ASIC/SOC Conf., 2002, pp. 97–101
14 Laemmle, B., Wagner, C., Knapp, H., Maurer, L., Weigel, R.: 'High speed low power phase accumulators for DDS applications in SiGe bipolar technology'. IEEE Bipolar/BiCMOS Circuits & Technology Meeting, 2009, pp. 162–165
15 Heinemann, B., Barth, R., Knoll, D., Rücker, H., Tillack, B., Winkler, W.: 'High performance BiCMOS technologies without epitaxially-buried subcollectors and deep trenches', *Semicond. Sci. Technol.*, 2007, **22**, pp. 153–157
16 O'Leary, P., Maloberti, F.: 'A direct-digital synthesizer with improved spectral performance', *IEEE Trans. Commun.*, 1991, **39**, (7), pp. 1046–1048
17 Turner, S.E., Elder, Jr. R.B., Jansen, D.S., Kotecki, D.E.: '4-bit adder-accumulator at 41-GHz clock frequency in InP DHBT technology', *IEEE Microw. Wirel. Compon. Lett.*, 2005, **15**, (3), pp. 144–146
18 Friedman, E.G.: 'Clock distribution networks in synchronous digital integrated circuits', Invited Paper, *Proc. IEEE*, 2001, **89**, (5), pp. 665–692
19 Khafaji, M., Gustat, H., Scheytt, J.: 'A 6 bit linear binary RF DAC in 0.25 μm SiGe BiCMOS for communication systems'. Proc. IMS, 2010, pp. 916–919