



Lehrstuhl für  
Eingebettete Systeme  
der Informationstechnik



## **Design and Implementation of an LDPC-based FEC encoder/decoder suitable for Storage devices**

Schriftliche Prüfungsarbeit für die Masterprüfung der Fakultät für Elektrotechnik und Informationstechnik an der Ruhr-Universität Bochum (Master-Prüfungsordnung für den Studiengang „Elektrotechnik und Informationstechnik“ an der Ruhr-Universität Bochum vom 12. August 2013)

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# 1. Abstract

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## 2. Motivation

### 3. Error Correcting Codes

For modern communications systems reliable data transmission and storage is required. To achieve this goal usually error correcting codes are used. There are different possible codes available for error correction, but I will restrain myself to LDPC[3] codes in this thesis. As these codes can archive good performance and can be used at large block lengths[6]. This is especially useful for use with NAND based solid state drives.

When describing a block code there are important parameters as the message length  $k$ . The message is what is given into the encoder and the result from the decoder. The block length  $n$ , and the rate  $R = k/n$ .

In this case error correction code are used to add additional information to data to allow errors. The errors are then corrected with that information. The addition of additional information is also called redundancy. With this redundancy it is possible to lose information while data is transmitted over a channel and decode it after the channel. After decoding the original data is recovered by using the additional information. figure 3.1 shows such a system where information is transmitted, the channel can be of different type. It can for example be a wireless transmission or memory where information is first stored and later read back.

#### 3.1. Low-Density Parity-Check (LDPC) Codes

The following section will describe LDPC codes invented by Robert Gallager[3]. Starting with a graph representation I will describe the LDPC code and then continue with a matrix representation. LDPC codes can be shown as a bipartite graph also called Tanner graph[7] based on their inventor. figure 3.2 shows an example of one, where the check and parity

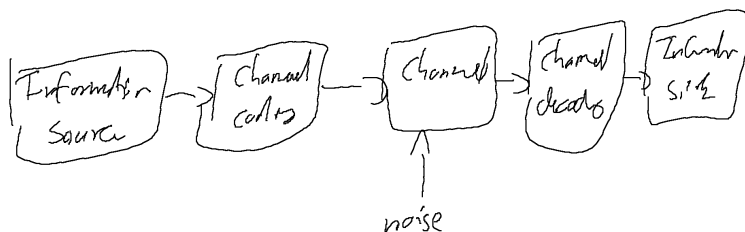


Figure 3.1.: A basic channel where information is transmitted



○ code Symbols (variable nodes)

□ parity equations (check nodes)

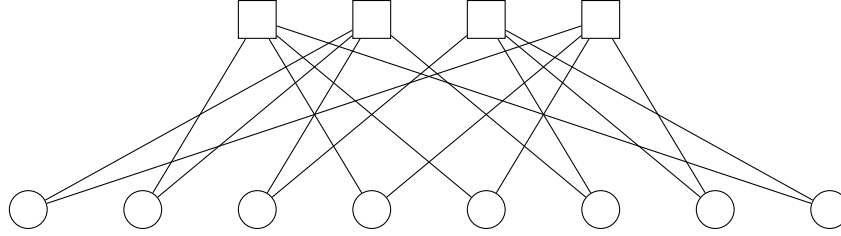


Figure 3.2.: An example Tanner graph.

nodes are connected by edges. This is an effective representation, moreover it will also help understanding the decoding algorithm later.

Instead of using the Tanner graph one can also use a matrix representation. In this matrix the ones represent the edges of the graph. Usually for a LDPC code the matrix is sparse or low density as the name implies. In equation (3.1) a matrix representing the same code as in the graph in figure 3.2 is shown. The  $\mathbf{H}$  matrix is of size  $(n - k) \times n$ . And the possible code words are given by the null space of  $\mathbf{H}$ , so in other words  $c$  is a code word if and only if  $c\mathbf{H}^T = \mathbf{0}$ [5].

$$\mathbf{H} = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \quad (3.1)$$

### 3.1.1. Quasicyclic LDPC (QC-LDPC) codes

LDPC codes can be difficult to implement, especially randomly generated ones. On the other hand structured codes can be devised to be more easily implemented. One class of these structured codes are quasicyclic LDPC codes. In these codes the parity check matrix is only built from circulant matrices and zero matrices[2]. The circulant matrices are defined by their first row as the following rows are the first one shifted. The base matrix specifies where zero matrices and where rotated circulant matrices are placed. Each circulant matrix has size  $p \times p$ . The parity check matrix has size  $(n - k) \times n = p(N - K) \times pN$ . Thus the base matrix  $\mathbf{B}$  has  $(N - K) \times N$  entries. Often times the circulant matrix is the identity matrix and is rotated by the corresponding amount in the base matrix. In this base matrix

the elements can be either a shift factor smaller than the circulant size  $0 \leq b_{ij} < p$  or  $-1$  representing a zero matrix.

In the following example the circulant matrix is a  $5 \times 5$  identity matrix.

$$\mathbf{B} = \begin{bmatrix} -1 & 0 & 2 & -1 \\ 0 & 1 & -1 & -1 \\ -1 & 1 & 0 & 2 \end{bmatrix} \quad (3.2)$$

After the expansion the matrix looks like this:

$$\mathbf{H} = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix} \quad (3.3)$$

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### 3.1.2. Encoding

#### Generator Matrix

For encoding the probably simplest algorithm is transforming the parity check matrix into systematic form  $\mathbf{H} = [-\mathbf{A}^T \quad \mathbf{I}_{n-k}]$ . Where  $\mathbf{I}_{n-k}$  is a  $n-k \times n-k$  identity matrix and  $\mathbf{A}$  has  $k \times n-k$  elements. To archive this form one could for example use gaussian elimination. With  $\mathbf{A}$  known we can construct the generator matrix  $\mathbf{G} = [\mathbf{I}_k \quad \mathbf{A}]$ . Now encoding can be done with a simple matrix multiplication. With  $u$  the information word and  $v$  the code word is given by  $v = \mathbf{G}u$ .

Take for example the matrix from equation (3.1). If we use gaussian elimination to bring the right side to identity we are left with equation (3.4). Now we take the left part of the matrix and transpose it to get  $\mathbf{A}$ . With we build  $\mathbf{G}$  in equation (3.5).

$$\mathbf{H} = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (3.4)$$

$$\mathbf{G} = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (3.5)$$

The main disadvantage of this strategy is the high computational complexity. When transforming the parity check matrix into systematic form we have a complexity of  $\mathcal{O}(n^3)$ . This is not too bad as it will mostly be done offline and only the  $\mathbf{G}$  matrix stored in the encoder, but the bigger problem is that due to the gaussian elimination the matrix is no longer sparse. Thus the matrix multiplication will result in a complexity of  $\mathcal{O}(n^2)$ [4].

### Approximate Lower Triangular Form

Richardson and Urbanke[5] describe a way to reorder the parity check matrix to reduce the encoding complexity. They bring the matrix into a so called approximate lower triangular form. This is done by only doing row and column permutation, so the low density of the matrix is kept. The resulting structure of the matrix is shown in figure 3.3. Especially advantageous is the reduced complexity for encoding, here the encoding complexity is reduced from  $\mathcal{O}(n^2)$  to  $\mathcal{O}(n + g^2)$ , where  $g$  is the gap. This gap is the number of rows that cannot be brought into triangular form, as seen in figure 3.3. We can also write

$$\mathbf{H} = \begin{bmatrix} \mathbf{A} & \mathbf{B} & \mathbf{T} \\ \mathbf{C} & \mathbf{D} & \mathbf{E} \end{bmatrix} \quad (3.6)$$

the submatrices all have the dimensions given in figure 3.3. By multiplying equation (3.6) with

$$\begin{bmatrix} \mathbf{I} & \mathbf{0} \\ -\mathbf{ET}^{-1} & \mathbf{I} \end{bmatrix} \quad (3.7)$$

the resulting matrix is

$$\begin{bmatrix} \mathbf{A} & \mathbf{B} & \mathbf{T} \\ -\mathbf{ET}^{-1}\mathbf{A} + \mathbf{C} & -\mathbf{ET}^{-1}\mathbf{B} + \mathbf{D} & \mathbf{0} \end{bmatrix} \quad (3.8)$$

. By splitting the codeword into three parts  $c = [s \ p_1 \ p_2]$  and applying the definition for valid code words  $\mathbf{H}^T = \mathbf{0}$ . It splits into

$$\mathbf{A}s^T + \mathbf{B}p_1^T + \mathbf{T}p_2^T = 0 \quad (3.9)$$

$$(-\mathbf{ET}^{-1}\mathbf{A} + \mathbf{C})s^T + (-\mathbf{ET}^{-1}\mathbf{B} + \mathbf{D})p^T = 0 \quad (3.10)$$

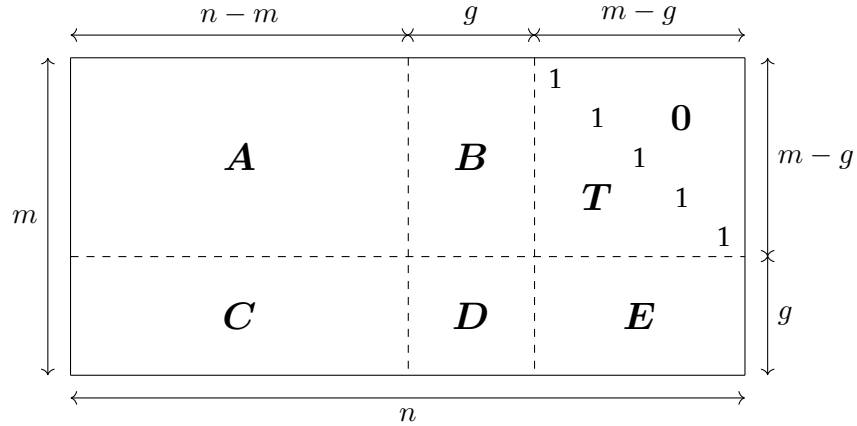


Figure 3.3.: Structure of a matrix in approximate lower triangular form.

Operation	Type
$\mathbf{A}s^T$	sparse multiplication
$\mathbf{T}^{-1}\mathbf{A}s^T$	sparse back substitution
$-\mathbf{E}\mathbf{T}^{-1}\mathbf{A}s^T$	sparse multiplication
$\mathbf{C}s^T$	sparse multiplication
$(-\mathbf{E}\mathbf{T}^{-1}\mathbf{A}s^T) + (\mathbf{C}s^T)$	vector addition
$\phi^{-1}(-\mathbf{E}\mathbf{T}^{-1}\mathbf{A}s^T + \mathbf{C}s^T)$	dense $g \times g$ multiplication

Table 3.1.: Calculations for  $p_1^T = \phi^{-1}(-\mathbf{E}\mathbf{T}^{-1}\mathbf{A} + \mathbf{C})s^T$

. The resulting equations for  $p_1$  and  $p_2$  are

$$p_1^T = -\phi^{-1}(-\mathbf{E}\mathbf{T}^{-1}\mathbf{A} + \mathbf{C})s^T \quad (3.11)$$

$$p_2^T = -\mathbf{T}^{-1}(\mathbf{A}s^T + \mathbf{B}p_1^T) \quad (3.12)$$

. The complexity of the computations can be reduced by computing  $\phi^{-1}$  offline. Offline meaning that it is precomputed and when encoding multiplying by the matrix. All the other matrix multiplications from equations (3.11) and (3.12) are done separately. Multiplications by  $\mathbf{A}$ ,  $\mathbf{B}$ ,  $\mathbf{C}$ , and  $\mathbf{E}$  are sparse and the resulting complexity for these is  $\mathcal{O}(n)$ . The multiplication with  $\mathbf{T}^{-1}$  is replaced by the system  $x^T = \mathbf{T}y^T$ . As  $\mathbf{T}$  is a sparse lower triangular matrix the system can be solved by back substitution in  $\mathcal{O}(n)$ . The only part with higher complexity is the multiplication with the dense  $g \times g$  matrix  $\phi$  where the complexity is  $\mathcal{O}(g^2)$ .

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Operation	Type
$\mathbf{A}s^T$	sparse multiplication
$\mathbf{B}p_1^T$	sparse multiplication
$(\mathbf{A}s^T) + (\mathbf{B}p_1^T)$	vector addition
$-\mathbf{T}^{-1}(\mathbf{A}s^T + \mathbf{B}p_1^T)$	sparse back substitution

Table 3.2.: Calculations for  $p_2^T = -\mathbf{T}^{-1}(\mathbf{A}s^T + \mathbf{B}p_1^T)$ 

### 3.1.3. Decoding

Decoding LDPC codes is a nontrivial problem, in fact maximum likelihood decoding is computationally infeasible. Therefore other decoding methods were developed. There are different decoding algorithms which differ in performance and complexity.

[decode dat](#)

## 4. Channel Models

As the encoded message is passed through a channel I will introduce some basic channel models in this chapter. I will only work with binary codes throughout this thesis. For binary codes it is convenient to use  $\{+1, -1\}$  as the alphabet. This simplifies the calculations of LLRs likewise it makes the bit energy  $E_b$  simple. Also the channel is memoryless, this may sound confusing at first when dealing with storage devices, but it says that each symbol is independently mangled by the channel. The input to the channel is in the input alphabet  $\mathcal{X} = \{1, -1\}$ . Whereas the the output alphabet  $\mathcal{Y}$  will change depending on the channel. Now when transmitting a codeword  $c \in \mathcal{X}^n$  the channel outputs  $y \in \mathcal{Y}^n$  and it is the receivers task to compute the original codeword  $c$  from  $y$ . Ideally this is done with few errors and close to the channel capacity.

better  
word

### 4.1. Binary Erasure Channel (BEC)

The binary erasure channel is characterized with a single parameter  $0 \leq \alpha < 1$  the erasure probability. The symbol for an erasure is  $?$ , therefore the output alphabet is  $\mathcal{Y} = \{1, -1, ?\}$ . The channel outputs  $x$  with probability  $1 - \alpha$  and  $?$  with probability  $\alpha$ . figure 4.1 shows the transitions for a BEC. So for a codeword with large length  $n$  there will be  $(1 - \alpha)n$  correct symbols, this suggests that the maximum rate is  $1 - \alpha$ . Elias[1] shows that this rate can be archived and also proves that this is the capacity.

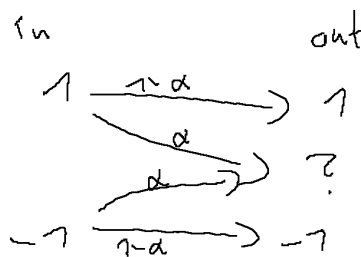


Figure 4.1.: Symmetric binary erasure channel

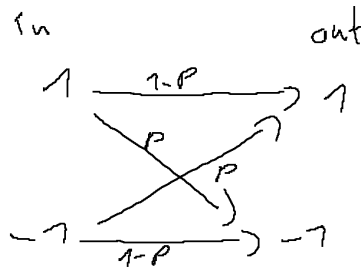


Figure 4.2.: Symmetric binary symmetric channel

## 4.2. BSC

A binary symmetric channel has the output alphabet  $\mathcal{Y} = \{1, -1\}$ . An incoming symbol has the probability  $p$  to create a crossover. With probability  $1 - p$  the symbol is correctly transmitted and with probability  $p$  it is flipped. In figure 4.2 a graph shows these probabilities. A binary symmetric channel with crossover probability  $p$  has the capacity  $1 - H(p)$  with  $H(p) = -p \log_2 p - (1 - p) \log_2 (1 - p)$  being the binary entropy function.

## 4.3. Additive White Gaussian Noise Channel

The additive white gaussian noise (AWGN) channel is the most important noise model for me as it characterizes flash memory well. It has a continuous output alphabet  $\mathcal{Y}$ . The model for the channel is  $y = x + z$  where the input is  $x \in \mathcal{X}$ .  $z$  is a variable with normal distribution with 0 mean and variance  $\sigma^2$ . It has the distribution  $f(z) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp(-\frac{z^2}{2\sigma^2})$ . The capacity for this channel is  $\frac{1}{2} \log_2(1 + \frac{1}{\sigma^2})$  as the Shannon limit shows. Often it is preferable to allow scaling of the input, so we use a signal to noise ratio  $E_b/\sigma^2$ . This allows the inputs to be arbitrary values then  $E_b$  is the energy of the transmission of a single bit. The  $\sigma^2$  is frequently called  $N_0$ , the energy of the noise that is added in a single bit transmission. When using  $E_b/N_0$  the capacity is  $\frac{1}{2} \log_2(1 + \frac{E_b}{N_0})$ . For example when having a rate of  $\frac{1}{2}$  we get a minimum signal to noise ratio required of 1.

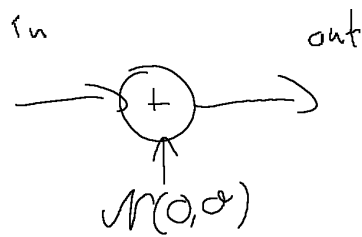


Figure 4.3.: Additive White Gaussian Noise Channel



## 5. Field Programmable Gate Array (FPGA)

In modern hardware design it is advantageous to have reprogrammable hardware elements. To create reconfigurable logic circuits basic elements consisting of lookup tables (LUT) and registers is built into an array and connected by programmable interconnects.

write  
some ba-  
sics about  
FPGA

## 6. Approach

## 7. Implementation

## 8. Results

## **A. Appendix**

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