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Design and Implementation of an LDPC-based FEC encoder/decoder suitable for Storage devices

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1. Abstract

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2. Motivation

3. Error Correcting Codes

For modern communications systems reliable data transmission and storage ist required. To achieve this goal usually error correcting codes are used. There are different possible codes available for error correction, but I will restrain myself to LDPC[1] codes in this thesis. As these codes can archive good performance and can be used at large block lengths[4]. This is especially useful for use with NAND based solid state drives.

When describing a block code there are important parameters as the message length k. The message is what is given into the encoder and the result from the decoder. The block length n is the length of the encoded message which is transmitted over the channel.And the rate $R = k/n$.

3.1. Low-Density Parity-Check (LDPC) Codes

The following section will describe LDPC codes invented by Robert Gallager[1]. Starting with a graph representation I will describe the LDPC code and then continue with a matrix representation. LDPC codes can be shown as a bipartite graph also called Tanner graph[5] based on their inventor. figure 3.1 shows an example of one, where the check and parity nodes are connected by edges. This is an effective representation, moreover it will also help understanding the decoding algorithm later.

Instead of using the Tanner graph one can also use a matrix representation. In this matrix the ones represent the edges of the graph. Usually for a LDPC code the matrix is sparse or

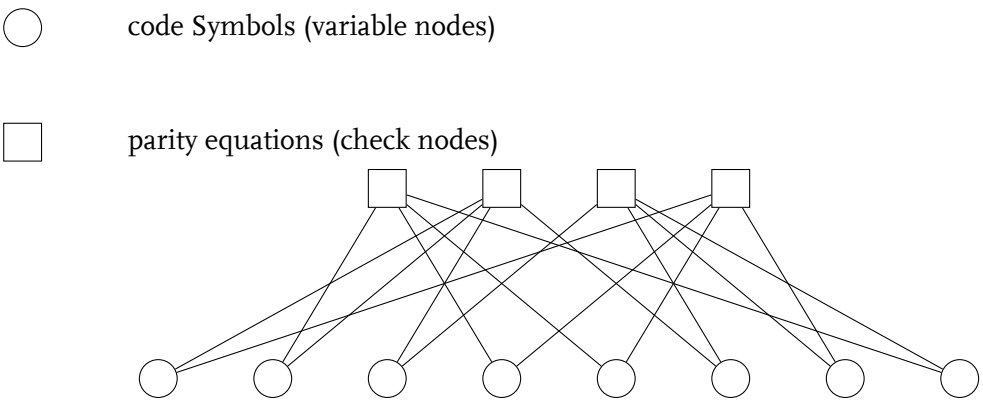

Figure 3.1.: An example Tanner graph.

low density as the name implies. In equation (3.1) a matrix representing the same code as in the graph in figure 3.1 is shown. The $\boldsymbol{H}$ matrix is of size $(n-k)xn$. And the possible code words are given by the null space of $\boldsymbol{H}$, so in other words c is a code word if and only if $c\boldsymbol{H}^T = \mathbf{0}$[3].

$$\boldsymbol{H} = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{3.1}$$

3.1.1. Encoding

Genrator Matrix

For encoding the probably simplest algorithm is transforming the parity check matrix into systematic form $\boldsymbol{H} = \begin{bmatrix} -\boldsymbol{A^T} & \boldsymbol{I_{n-k}} \end{bmatrix}$. Where $\boldsymbol{I_{n-k}}$ is a $n-k \times n-k$ identity matrix and $\boldsymbol{A}$ has $k \times n-k$ elements. To archive this form one could for example use gaussian elimination. With $\boldsymbol{A}$ known I can construct the generator matrix $\boldsymbol{G} = \begin{bmatrix} \boldsymbol{I_k} & \boldsymbol{A} \end{bmatrix}$. Now encoding can be done with a simple matrix multiplication. With u the information word and v the code word is given by $v = u\boldsymbol{G}$.

The main disadvantage of this strategy is the high computational complexity. When transforming the parity check matrix into systematic form we have a complexity of $\mathcal{O}(n^3)$. This is not to bad as it will mostly be done offline and only the $\boldsymbol{G}$ matrix stored in the encoder, but the bigger problem is that due to the gaussian elimination the matrix is no longer sparse. Thus the matrix multiplication will result in a complexity of $\mathcal{O}(n^2)$[2].

Approximate Lower Triangular Form

4. Field Programmable Gate Array (FPGA)

write some basics about FPGA

5. Approach

6. Implementation

7. Results

A. Appendix

Bibliography

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