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Design and Implementation of an LDPC-based FEC encoder/decoder suitable for Storage devices

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1. Abstract

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2. Motivation

3. Error Correcting Codes

For modern communications systems reliable data transmission and storage ist required. To achieve this goal usually error correcting codes are used. There are different possible codes available for error correction, but I will restrain myself to LDPC[1] codes in this thesis. As these codes can archive good performance and can be used at large block lengths[3]. This is especially useful for use with NAND based solid state drives.

When describing a block code there are important parameters as the message length k. The message is what is given into the encoder and the result from the decoder. , the block length n, and the rate $R = k/n$.

3.1. Low-Density Parity-Check (LDPC) Codes

The following section will describe LDPC codes invented by Robert Gallager[1]. Starting with a graph representation I will describe the LDPC code and then continue with a matrix representation. LDPC codes can be shown as a bipartite graph also called Tanner graph[4] based on their inventor. figure 3.1 shows an example of one, where the check and parity nodes are connected by edges. This is an effective representation, moreover it will also help understanding the decoding algorithm later.

Instead of using the Tanner graph one can also use a matrix representation. In this matrix the ones represent the edges of the graph. Usually for a LDPC code the matrix is sparse or low density as the name implies. In equation (3.1) a matrix representing the same code as

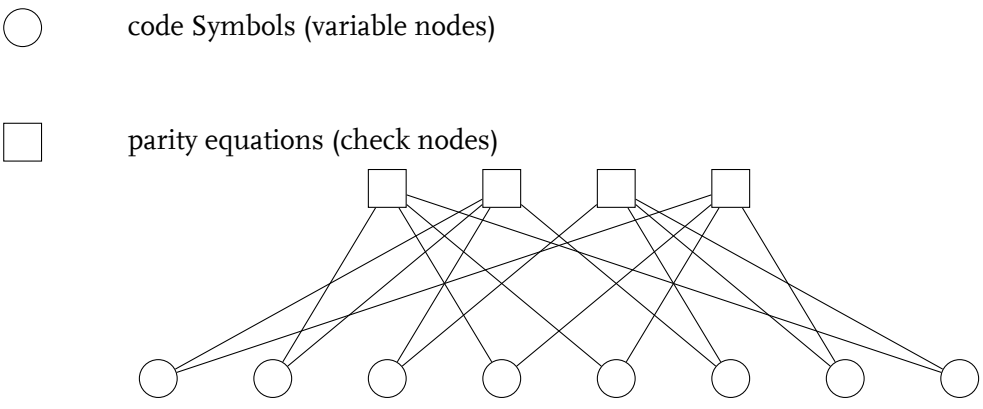

Figure 3.1.: An example Tanner graph.

in the graph in figure 3.1 is shown. The $\boldsymbol{H}$ matrix is of size $(n-k)xn$. And the possible code words are given by the null space of $\boldsymbol{H}$, so in other words c is a code word if and only if $c\boldsymbol{H}^T = \mathbf{0}$[2].

$$\boldsymbol{H} = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{3.1}$$

4. Field Programmable Gate Array (FPGA)

5. Approach

6. Implementation

7. Results

A. Appendix

Bibliography

[1] Robert R. Gallager. “Low-Density Parity-Check Codes”. In: (1963).

[2] Thomas J. Richardson and Rüdiger L. Urbanke. *Efficient Encoding of Low-Density Parity-Check Codes*. 2001. DOI: 10.1109/18.910579.

[3] Bashar Tahir, Stefan Schwarz, and Markus Rupp. “BER comparison between Convolutional, Turbo, LDPC, and Polar codes”. In: (2017). DOI: 10.1109/ICT.2017.7998249.

[4] M. Tanner. “A recursive approach to low complexity codes”. In: (1981). DOI: 10.1109/TIT.1981.1056404.