everyday genius

MT7623N Datasheet

Version: Preliminary
Release date: 2015-10-29

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Overview

MT7623N is a highly integrated multimedia network router system-on-chip used for high wireless performance, home entertainment, home automation and so on.

Applications:
- Internet service router
- Wireless router
- Smart router
- Home security gateway
- Home automation
- NAS devices
- Switch control processor

MT7623N is fabricated with advanced silicon process and integrates a Quad-core ARM® Cortex-A7 MPCoreTM operating up to 1.3GHz and more DRAM bandwidth. This SoC also includes a variety of peripherals, including HDMI TX, MIPI, RGMII, TRGMII, PCIe2.0, USB2.0 OTG and USB3.0 ports. To support popular network applications, MT7623N also implements 10/100/1000 Ethernet RGMII interfaces and supports 802.11ac/n WLAN connection thru its PCIe port.

MT7623N includes two wireless connectivity functions, WLAN, Bluetooth. The RF parts of those two blocks are put in the MT6625L chip. With two advanced radio technologies integrated into one single chip, MT7623N/MT6625L provides the best and most convenient connectivity solution among the industry. MT7623N/MT6625L implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms.

Besides the connectivity features, the multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Audio supports include FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

The hardware-based NAT engine with QoS embedded in MT7623N transporting the audio/video streams in higher priority than other non-timely services also enriches the home entertainment application. The SFQ separating P2P sessions from audio/video ones so that MT7623N guarantees the streaming service. With the advanced technology and abundant features, MT7623N is well positioned to be the core of next-generation Smart WiFi AP router, and home gateway systems.

Key Features

- Embedded Quad-core ARM® Cortex-A7 MPCore operating at 1.3GHz
  - 32KB L1 I-Cache and 32KB L1 D-Cache
  - 512KB unified L2 Cache
  - NEON/FPU
  - DVFS technology
- Mali 450 MP4
- 32-bit LPDDR2 and DDR3/L
- NOR(SPI), NAND Flash(SLC/MLC), MSDC(4-bits), eMMC4.5
- USB3.0 Host x 2 (2nd port share w/ PCIe2.0)
- USB2.0 OTG x 1
- PCIe2.0 Host x 3 (3rd port share w/ USB3.0)
- SPI, I2C, UART Lite, JTAG, MDC, MDIO, GPIO, PWM, ADC, DAC
- VoIP support (I2S, PCM)
- Audio interface (SPDIF, I2S, PCM)
- HDMI 1.4 TX
- MIPI(4-lane), CVBS(Video)
- HD H.264/MPEG-2/AVC/VC-1 video decode
- Deliver the super Samba performance via USB2.0/USB3.0/SD-XC
- TRGMII/RGMII interface (TRGMII only for MT7530)
- HW storage accelerator
  - HW NAT
  - 2Gbps wired speed
  - L2 bridge
  - IPv4 routing, NAT, NAPT
  - IPv6 routing, DS-Lite, 6RD, 6to4
- HW QoS
  - 16 hardware queues to guarantee the min/max bandwidth of each flow.
  - Seamlessly co-work with HW NAT engine.
  - 2Gbps wired speed.
  - SFQ w/ 1k queues.
- HW Crypto Engine
  - Deliver 1 Gbps IPSec throughput

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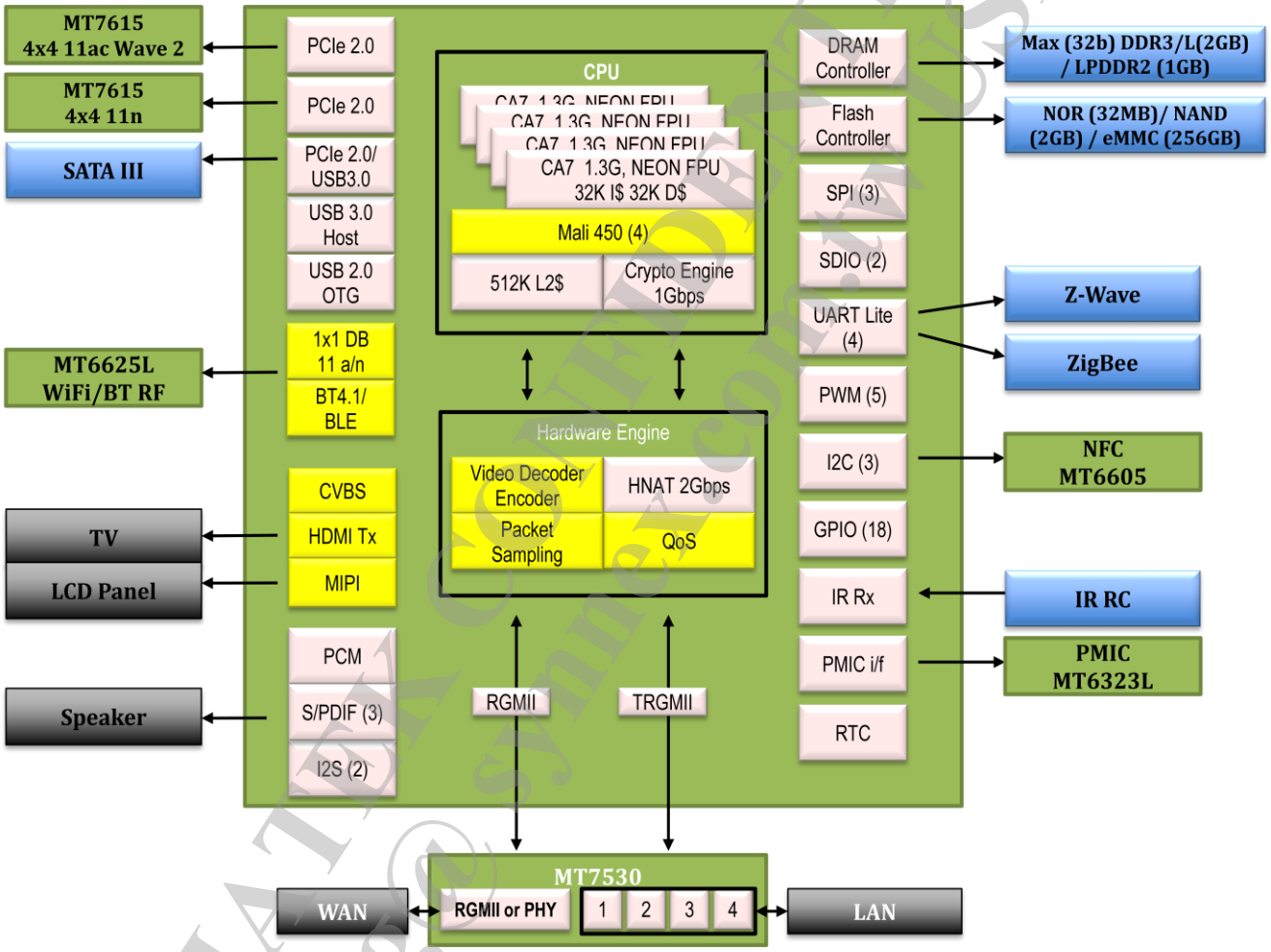
  - AES/3DES, MD5/SHA1/SHA2
- Green
  - Intelligent Clock Scaling (exclusive)
  - DDR: ODT off, Self-refresh mode
- Software: Linux 3.10.20 SDK, OpenWRT, Android L

Functional Block Diagram



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Document Revision History

Revision	Date	Author	Description
Preliminary	2014-12-26	Ken Wu	Initial Release
	2015-5-15	Leon Chung	Change pin name of Serial Flash Interface
	2015-6-15	Leon Chung	1. Section 2.2, add reset Aux and Pull columns into pin description table 2. Section 2.3.1, add EINT(External INT) column into pin share scheme table 3. Add new sections 2.3.2 and 2.3.3
	2015-6-22	Leon Chung	1. Section 2.2, add IO reset state.
	2015-7-6	Leon Chung	1. Section 3.6, add amplitude value. 2. Section 1.4, add TRGMII description. 3. Section 2.2, add GE1 note description.
	2015-7-27	Leon Chung	1. Rename part number to MT7623N
	2015-8-27	Yushu Xiao	1. Section 3.8, update power on sequence
	2015-9-15	Ken Wu Chungfa	1. Section 3.2, revised VCCK voltage range 2. Section 3.3, add case temperature
	2015-10-28	Yushu Xiao	1. Section 2.4, revised boot download mode value

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Lists of Tables and Figures

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1 General Features

1.1 Platform Features

- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A7 MPCoreTM operating at 1.3 GHz
  - NEON multimedia processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 1.05V to 1.31V
- **CONN MCU subsystem**
  - Andes N9 processor with 32KB I-cache, 16KB D-cache
- **External memory interface**
  - Supports LPDDR2, DDR3/L
  - 32-bit data bus width
  - Memory clock up to 533MHz(LPDDR2) and 800MHz(DDR3/L)
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
- **Security**
  - ARM® TrustZone® Security
  - Security boot
  - Crypto engine(IPSEC/ DES/ 3DES/ AES/ ARC4/ MD5/ SHA1/ SHA2/ GHASH/ CRC32/ PRNG)
- **Connectivity**
  - 3 PCIe2.0 (3rd port is shared w/ USB3.0)
  - 2 USB3.0 (2nd port is shared w/ PCI2.0)
  - USB2.0 high-speed dual mode supporting 8 Tx and 8 Rx endpoints
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - UART for external devices and debugging interfaces
  - SPI master for external devices
  - I2C to control peripheral devices,
  - I2S master output and master/slave input for connection with optional external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controller supporting(SD/ SDHC/ MS/ MSPRO/ MMC and SDIO2.0/3.0 protocols)
  - IR Rx
- **Operating conditions**
  - Core voltage: 1.15V
  - Processor DVFS+SRAM voltage : 1.05V~1.31V (Typ. 1.15V; Sleep mode 0.85V)
  - I/O voltage: 1.8V/3.3V
  - Memory: 1.2V/1.35V/1.5V
  - NAND: 1.8V/3.3V
  - Clock source: 26MHz, 32.768kHz
- **Package**
  - FBGA 21x21mm 485 balls
  - Ball pitch: 0.8mm

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1.2 Multimedia Features

- **Display**
  - Supports landscape or portrait panel resolution up to WUXGA (1920x1200)
  - MIPI DSI interface (4 data lanes)
  - Embedded LCD gamma correction
  - Supports true colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Supports spatial and temporal dithering
  - Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Supports color enhancement
  - Supports adaptive contrast enhancement
  - Supports image/video/graphic sharpness enhancement
  - Supports dynamic backlight scaling
  - Automatic detect film or video source
  - 3:2 pull down source detection
  - Advanced motion adaptive de-interlace with edge preserving
  - Noise Reduction
  - Supports parallel camera input

- **HDMI transmitter**
  - Support HDMI 1.4 output with HDCP 1.4
  - Audio return channel
  - Support DVI 1.0
  - EIA/CEA-861E

- **TV Encoder**
  - One 12bit DAC
  - Support NTSC, NTSC-433, PAL-BDGHINM, PAL-60
  - Automatically turn off unconnected channel
  - Support Macrovision 7.1 L1
  - CGMS-A/WSS
  - Closed Caption

- **Graphics**
  - OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 90M tri/sec and 1.2G pixel/sec @ 416MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Hardware JPEG encoder: Baseline encoding with 120M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format
  - Support Baseline JPEG decoding
  -

- **Video decoder**
  - HEVC decoder : Main profile 1080p @ 60fps with 10bit stream
  - VP8/VP9 decoder : 1080p@60fps
  - H.264 decoder: Baseline 1080p @ 60fps
  - H.264 decoder: Main/high profile 1080p@60fps
  - MPEG-4 SP/ASP decoder: 1080p @ 60fps
  - MPEG-1/2 decoder: Main profile 1080p@60fps
  - WMV9/VC-1 decoder: Advanced profile @L4
  - Sorenson Spark
  - Support DivX 3.11/4.x/5.x/6.x/HD
  - Support Xvid Video
  - Support WMV 7/8
  - Support Sorenson Spark
  - Support Real Video 8/9/10

- **Video encoder**
  - VP8 encoder: 1080p @ 30fps
  - H.263 encoder: D1 @ 30fps (SW)
  - H.264 encoder: High profile 1080p @ 30fps
  - MPEG1/2, MP@HL@1080p @ 30fps @ 40Mbps (SW)

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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- CTM
- Noise reduction
- Noise suppression
- Noise cancellation
- Dual-MIC noise cancellation
- Echo cancellation
- Echo suppression
- Dual-MIC input
- Digital MIC input

1.3 BT/WLAN with MT6625L Features

- **Common**
  - Self calibration
  - Single TCXO and TSX for BT and WLAN
  - Best-in-class current consumption performance
  - OS supported: Android
  - Intelligent BT/WLAN coexistence scheme
  - Single antenna support for WLAN/Bluetooth

- **WLAN**
  - Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w Protected Managed Frames
  - Supports WiFi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated PA with max 21dBm output power
  - Typical -77.5 dBm 2.4GHz receiver sensitivity at 11g 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 10dBm (class 1) transmit power and Balun
  - Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet loss concealment (PLC) function for better voice quality
  - Low-power scan function to reduce the power consumption in scan modes

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, WBT diplexer.
  - Fully integrated in one IPD die
  - Supports single and dual antenna operation.

1.4 Main Features Summary

The following table covers the main features offered by MT7623N. Overall, the MT7623N supports the requirements of a high-level AP/router, and a number of interfaces together with a large maximum RAM capacity.

Table 1-1 Main Features

Features	MT7623N

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CPU	ARM CA7 (1.3GHz, Quad-core), NEON
I-Cache, D-Cache	32kB, 32kB per core
L2 Cache	512KB
GPU	Mali 450 MP4 (416MHz)
HNAT/HQoS	HQoS 16 queues, SFQ 1k queues HNAT 2Gbps forwarding (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4)
DRAM data	32bit
LPDDR2	1066 Mbps (max 8Gb)
DDR3/L	1600 Mbps (max 16Gb)
SD **eMMC**	SD-XC class 10 (4bits, max 128GByte) eMMC4.5 (max 128GByte)
NAND (SLC type)	ONFI2.0 (8bits, max 60b ECC) Small page 512-Byte (max 512Mbit) Large page 2k-Byte (max 2GB) Note that pin sharing w/ eMMC4.5.
SPI Flash (NOR)	1 (max 50MHz) 3B addr mode (max 128Mbit) 4B add. mode (max 512Mbit) The 2nd chip select is by pin sharing.
HDMI	TX x 1
MIPI	4-Lane
CVBS	1 (Video)
PCIe	PCIe2.0 x 3 (3rd port pin sharing w/ USB3.0)
USB	USB2.0 OTG x 1 (w/ BC 1.2) USB3.0 x 2 (2nd port pin sharing w/ PCIe2.0)
Ethernet	TRGMII (Giga and Turbo mode only) x 1 + RGMII x 1
I2S	2 (max 192k sample rate, 24bits)
PCM	1 (4 ch)
SPDIF	1 out, 2 in
I2C	3 (Max 400kHz) The 4th I2C are by pin sharing.
SPI	3
UART Lite	3 The 3rd UART has flow control. The 4th UART Lite is by pin sharing.

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DAC	2
ADC	6
IR RX	1
JTAG	1
Package	FBGA 21 x 21 mm

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2 Pins

2.1 Ball Map (Top View)

Table 2-1 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	MSDC0_DAT7	MSDC0_DAT1	MSDC0_DAT4		NREB		NC	AVDD12_HDR		AVDD18_HDR	
B	MSDC0_CLK	MSDC0_DAT2	MSDC0_DAT6	MSDC0_DAT0		NRNB		NC	AVSS33_HDR		GPIO245	
C			GND	MSDC0_DAT5	MSDC0_RSTB	NCEB1		NC	NC	NC	GPIO244	MHL_SENCE
D	RDQ31	RDQ29	RDQ25	RDQ27	MSDC0_CMD	MSDC0_DAT3		NC	NC	NC	GPIO247	AVSS_USB_P2
E	RDQ18	RDQ16	GND	RDQM2	RDQM3	SPI0_MI	NCLE		DVDD28_NOR			SFLASH_IO_3
F			RDQ20	RDQ22	RDQS3	RDQS3_	NCEB0		DVDD28_DPI	AVDD33_HDR		SFLASH_IO_2
G	RDQ17	RDQ19	RDQ21	RDQ23			SPI0_CK		DVDD28_MSDC0		SFLASH_CS_L	SFLASH_CLK
H	RDQ30	RDQ28	GND	RDQS2	RDQS2_	GND	SPI0_CSN	SPI0_MO		GPIO248		SFLASH_IO_0
J			RDQ24	RDQ26	RCLK1	RCLK1_	VDD_EMI	GND	VCCK	VCCK	VCCK	GND
K	RRAS	DDR3RSTB	RBA2	RCS1		GND	VDD_EMI	AVDD18_MEMPLL	AVSS18_MEMPLL	VCCK	GND	VCCK_VPROC
L	RCS0	RCAS	GND	RA2	RA15	GND	VDD_EMI	TP_MEMPLL	VCCK	VCCK	GND	VCCK_VPROC
M			RA9	RWE	RBA0	GND	VDD_EMI	GND	VCCK	GND	GND	VCCK_VPROC
N	RA3	RA0	RA5	RA13		GND	VDD_EMI	VCCK	GND	GND	GND	GND
P	RA4	RBA1	GND	RA11	RA12	RA7	VDD_EMI	GND	VCCK	GND	GND	GND
R			RA6	RA1	RCLK0_	RCLK0	VDD_EMI	VCCK	GND	GND	GND	GND
T	RCKE	RA10	RA14	RA8			VREF0	VCCK	GND	GND	GND	VCCK
U	RDQ9	RDQ11	RDQM1	GND	GND			VCCK			VCCK	VCCK
V			RDQ15	RDQ13	RDQS0	RDQS0_	VCCK	VCCK		DVDD28_I2S		
W	RDQ4	RDQ6	RDQ2	RDQ0	RDQS1_	RDQS1			DVDD28_MSDC1			USB_DM1
Y	RDQ5	RDQ7	GND	RDQM0				AVDD11_PCIE_P0		AVDD33_USB	USB_DM0	USB_DP1
AA			RDQ1	RDQ3		PCIE_VRT_P0	AVSS_PCIE	AVDD11_PCIE_P1			USB_DP0	AVDD18_SSUSB
AB	RDQ8	RDQ10	RDQ14	RDQ12	DVDD18_IO_MSDC1	PCIE_CKN0	PCIE_TXN1		PCIE_CKP1	PCIE_VRT_P1	AVSS_SSUSB	USB_RXN0
AC	MSDC1_DAT1	REXTDN	MSDC1_DAT2	MSDC1_DAT3	DVDD18_IO	PCIE_CKP0	PCIE_TXP1	AVSS_PCIE	PCIE_CKN1	PCIE_CKP2	SSUSB_VRT_P0	USB_RXP0
AD	MSDC1_iNS	MSDC1_CMD	MSDC1_CLK	PCIE_TXP0	DVDD18_IO_I2S	PCIE_RXP0		PCIE_RXP1		PCIE_CKN2	USB_TXN0	
AE	GND	MSDC1_DAT0	FSOURCE_P0	PCIE_TXN0	AVDD18_PCIE	PCIE_RXN0		PCIE_RXN1		AVDD18_USB	USB_TXP0	
	1	2	3	4	5	6	7	8	9	10	11	12

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13	14	15	16	17	18	19	20	21	22	23	24	25	
CHG_DM_P2	AVDD18_USB_P2		RTC32K_CK		AVDD33_VDAC_C		DAC_A_OUTPUT	AVDD18_DAC		EINT7	26M_CLKSQ	GND	A
CHG_DP_P2	USB_VRT_P2		SRCLKENAI		VDAC_C		DAC_B_OUTPUT	AVSS18_DAC		EINT1	GND	PCM_SYNC	B
	USB_DM_P2		SRCLKENA	SYSRSTB	AVSS33_VDAC_C	GPIO255	GPIO257	GPIO250	GPIO256	EINT2	EINT5	PCM_CLK	C
AVDD33_USB_P2	USB_DP_P2	SDA1	WATCHDOG		GPIO252	GPIO251	GPIO254	GPIO253	EINT4	EINT3	PCM_TX	PCM_RX	D
SFLASH_IO_1	USB_VBUS_P2	SDA2			URXD1	UTXD0	URXD0	EINT6	EINT0	SPI1_CSN			E
DVDD18_IO_MSDC0		SCL2	PWRAP_SPI0_CK		IR	UTXD1	URTS2	UCTS2	SPI1_MO	SPI2_CSN	SPI1_MI	SPI1_CK	F
DVDD18_IO_NOR			PWRAP_SPI0_MI		PWRAP_SPI0_CK2	UTXD2	URXD2	JTDO	SPI2_MO	SPI2_MI			G
DVDD18_IO_DPI	SCL1		PWRAP_SPI0_MO	PWRAP_INT	PWRAP_SPI0_CSN2		JTMS	JTCK	SPI2_CK	GND	AUX_IN4	AUX_IN5	H
GND	VCCK		PWRAP_SPI0_CSN			SPDIF_OUT	JTAG_RESET	JTDI	AUX_IN3	AUX_IN2	AVSS18_AP	AVDD18_AP	J
VCCK_VPROC	VCCK_VPROC		VCCK_VPROC		SPDIF_IN1	SPDIF_IN0	TESTMODE	REFP	AUX_IN0	AUX_IN1			K
VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	GND	GND	SCL0	SDA0	HDMITX_REXT	CEC	HDMITX_CH1_M	HDMITX_CH1_P	HDMITX_CH2_P	HDMITX_CH2_M	L
VCCK_VPROC	VCCK_VPROC	GND		GND	AVDD18_PLLGP	AVSS18_PLLGP	GND		HDMITX_CH0_M	HDMITX_CH0_P			M
GND	GND	GND	GND	DVDD28_RGMII	GND	GND		GND	HDMITX_CLK_M	HDMITX_CLK_P	AVSS18_HDMITX	AVDD18_HDMITX	N
GND	VCCK	GND					GND		HDMISCK	HTPLG			P
VCCK	VCCK	GND	DVDD18_IO_RGMII						G2_TXD0	HDMISD	G2_TXD2	G2_TXD1	R
		GND		DVDD_GE1_VREF	DVDD_GE1_IO			GND	G2_RXCLK	G2_TXD3	G2_TXEN		T
				DVDD_GE1_IO		GND	GND	G2_TXCLK	G1_RXD2	G1_RXDV	G1_RXD3		U
	DSI_TE	AUD_EXT_CK2	LCM_RST	I2S1_BCK		G2_RXD2	G2_RXD0	G2_RXDV	G1_RXCLK	GND	G1_RXD1	G1_RXD0	V
AVDD11_SSUSB_P0	AUD_EXT_CK1			I2S1_LRCK	G2_RXD1	G2_RXD3	MDC	MDIO	G1_TXCLK				W
		PWM4	PWM1	I2S1_DATA_IN	I2S1_DATA	I2S0_BCK	I2S0_LRCK	WB_RSTB	GND	G1_TXD2	G1_TXD1	G1_TXD0	Y
	MIPI_TDP2	PWM2	PWM0	PWM3	I2S1_MCLK	I2S0_MCLK	I2S0_DATA_IN	GPIO61	G1_TXD3	G1_TXEN			AA
DVDD18_MIPITX	MIPI_TDN2	MIPI_TDP3	AVSS_SSUSB	USB_RXN1	I2S0_DATA	WB_CRTL2	WB_CRTL0	WB_SDATA	GPIO62	AVSS18_WBG	WB_SEN	XIN_WBG	AB
DVSS18_MIPITX	MIPI_VRT	MIPI_TDN3	AVDD11_SSUSB_P1	USB_RXP1	SSUSB_VRT_P1	WB_CRTL3	WB_CRTL1	TEST_GQP	TEST_GQN	WB_SCLK	TEST_GIN	TEST_GIP	AC
MIPI_TCN	MIPI_TDP0	MIPI_TDP1	USB_TXN1		AVDD18_WBG	WB_CRTL4		WB_RXIN	WB_RXQN	AVSS18_WBG	WB_TXQP	WB_TXQN	AD
MIPI_TCP	MIPI_TDN0	MIPI_TDN1	USB_TXP1		DVDD18_IO_WBCT	WB_CRTL5		WB_RXIP	WB_RXQP	WB_TXIP	WB_TXIN	AVSS18_WBG	AE
13	14	15	16	17	18	19	20	21	22	23	24	25	

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2.2 Pin Descriptions

Table 2-2 Pin Description

Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
GPIO								
C20	GPIO257	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO257
C22	GPIO256	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO256
C19	GPIO255	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO255
D20	GPIO254	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO254
D21	GPIO253	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO253
D18	GPIO252	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO252
D19	GPIO251	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO251
C21	GPIO250	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO250
H10	GPIO248	OL	1	-	PD	1.8	4/8/12/16	GPIO248
D11	GPIO247	I	1	-	PD	1.8	5v open-drain	GPIO247
B11	GPIO245	I	1	-	PD	1.8	5v open-drain	GPIO245
C11	GPIO244	I	1	-	PD	1.8	5v open-drain	GPIO244
AB22	GPIO62	I	1	PD	PU/PD	1.8	2/4/6/8	GPIO62
AA21	GPIO61	I	1	PD	PU/PD	1.8	2/4/6/8	GPIO61
EINT								
E22	EINT0	OL	2	PD	PU/PD	3.3	4/8/12/16	External interrupt input0
B23	EINT1	OL	2	PD	PU/PD	3.3	4/8/12/16	External interrupt input1
C23	EINT2	OL	2	PD	PU/PD	3.3	4/8/12/16	External interrupt input2
D23	EINT3	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input3
D22	EINT4	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input4
C24	EINT5	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input5
E21	EINT6	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input6
A23	EINT7	OL	6	PD	PU/PD	3.3	4/8/12/16	External interrupt input7
UART								
E19	UTXD0	OH	1	-	PD	1.8	5v open-drain	UART port0 TX data
E20	URXD0	I	1	-	PD	1.8	5v open-drain	UART port0 RX data
F19	UTXD1	I	0	PD	PD	1.8	5v open-drain	UART port1 TX data
E18	URXD1	I	0	PD	PD	1.8	5v open-drain	UART port1 RX data
G19	UTXD2	I	0	PD	PU/PD	3.3	4/8/12/16	UART port2 TX data
G20	URXD2	I	0	PD	PU/PD	3.3	4/8/12/16	UART port2 RX data
F21	UCTS2	I	0	PD	PU/PD	3.3	4/8/12/16	UART port2 clear to send

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
F20	URTS2	I	0	PD	PU/PD	3.3	4/8/12/16	UART port2 request to send
JTAG								
G21	JTDO	OL	1	PU	PU/PD	1.8	2/4/6/8	JTAG data output
J21	JTDI	I	1	PU	PU/PD	1.8	2/4/6/8	JTAG data input
H20	JTMS	I	1	PU	PU/PD	1.8	2/4/6/8	JTAG mode select
H21	JTCK	I	1	PU	PU/PD	1.8	2/4/6/8	JTAG clock
J20	JTAG_RESET	I	0	PU	PU/PD	1.8	2/4/6/8	JTAG target reset
I2C								
L18	SCL0	I	1	-	PD	1.8	5v open-drain	I2C port0 clock
L19	SDA0	I	1	-	PD	1.8	5v open-drain	I2C port0 data
H14	SCL1	I	1	-	PD	1.8	5v open-drain	I2C port1 clock
D15	SDA1	I	1	-	PD	1.8	5v open-drain	I2C port1 data
F15	SCL2	I	1	-	PD	1.8	5v open-drain	I2C port2 clock
E15	SDA2	I	1	-	PD	1.8	5v open-drain	I2C port2 data
SPI								
G7	SPI0_CK	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 clock
H7	SPI0_CSN	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 chip select
E6	SPI0_MI	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 data in
H8	SPI0_MO	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 data out
F25	SPI1_CK	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 clock
E23	SPI1_CSN	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 chip select
F24	SPI1_MI	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 data in
F22	SPI1_MO	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 data out
H22	SPI2_CK	I	0	PD	PD	1.8	5v open-drain	SPI port2 clock
F23	SPI2_CSN	I	0	PD	PD	1.8	5v open-drain	SPI port2 chip select
G23	SPI2_MI	I	0	PD	PD	1.8	5v open-drain	SPI port2 data in
G22	SPI2_MO	I	0	PD	PD	1.8	5v open-drain	SPI port2 data out
PWM								
AA16	PWM0	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
Y16	PWM1	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
AA15	PWM2	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
AA17	PWM3	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
Y15	PWM4	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
SFlash								

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
G12	SFLASH_CLK	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash clock
G11	SFLASH_CS_L	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash chip select
H12	SFLASH_IO_0	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #0
E13	SFLASH_IO_1	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #1
F12	SFLASH_IO_2	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #2
E12	SFLASH_IO_3	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #3
NAND								
F7	NCEB0	I	0	PU	PU/PD	3.3	4/8/12/16	NAND flash chip select0
C6	NCEB1	I	0	PU	PU/PD	3.3	4/8/12/16	NAND flash chip select1
A6	NREB	I	0	PD	PU/PD	3.3	4/8/12/16	NAND flash read enable
E7	NCLE	I	0	PD	PU/PD	3.3	4/8/12/16	NAND flash command latch enable
B6	NRNB	I	0	PU	PU/PD	3.3	4/8/12/16	NAND flash ready/busy
MSDC								
B1	MSDC0_CLK	OL	1	PD	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 clock (eMMC4.5)
D5	MSDC0_CMD	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 command (eMMC4.5)
B4	MSDC0_DAT0	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #0 (eMMC4.5)
A3	MSDC0_DAT1	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #1 (eMMC4.5)
B2	MSDC0_DAT2	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #2 (eMMC4.5)
D6	MSDC0_DAT3	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #3 (eMMC4.5)
A4	MSDC0_DAT4	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #4 (eMMC4.5)
C4	MSDC0_DAT5	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #5 (eMMC4.5)
B3	MSDC0_DAT6	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #6 (eMMC4.5)
A2	MSDC0_DAT7	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #7 (eMMC4.5)
C5	MSDC0_RSTB	OH	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 reset output (eMMC4.5)
AD3	MSDC1_CLK	OL	1	PD	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 clock
AD2	MSDC1_CMD	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 command
AD1	MSDC1_INS	I	0	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 card insert
AE2	MSDC1_DAT0	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #0
AC1	MSDC1_DAT1	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #1
AC3	MSDC1_DAT2	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #2
AC4	MSDC1_DAT3	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #3
T/RGMII	*5							
V22	GE1_RXCLK	I				1.5/1.8		TRGMII1 RX clock
U23	GE1_RXDV	I				1.5/1.8		TRGMII1 RX data valid

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
V25	GE1_RXD0	I				1.5/1.8		TRGMII1 RX data bit #0
V24	GE1_RXD1	I				1.5/1.8		TRGMII1 RX data bit #1
U22	GE1_RXD2	I				1.5/1.8		TRGMII1 RX data bit #2
U24	GE1_RXD3	I				1.5/1.8		TRGMII1 RX data bit #3
W22	GE1_TXCLK	OL				1.5/1.8		TRGMII1 TX clock
AA23	GE1_TXEN	OL				1.5/1.8		TRGMII1 TX data valid
Y25	GE1_TXD0	OL				1.5/1.8		TRGMII1 TX data bit #0
Y24	GE1_TXD1	OL				1.5/1.8		TRGMII1 TX data bit #1
Y23	GE1_TXD2	OL				1.5/1.8		TRGMII1 TX data bit #2
AA22	GE1_TXD3	OL				1.5/1.8		TRGMII1 TX data bit #3
T22	GE2_RXCLK	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX clock
V21	GE2_RXDV	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data valid
V20	GE2_RXD0	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #0
W18	GE2_RXD1	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #1
V19	GE2_RXD2	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #2
W19	GE2_RXD3	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #3
U21	GE2_TXCLK	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX clock
T24	GE2_TXEN	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data valid
R22	GE2_TXD0	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #0
R25	GE2_TXD1	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #1
R24	GE2_TXD2	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #2
T23	GE2_TXD3	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #3
PHY Mgn.								
W20	MDC	I	0	PD	PU/PD	3.3	4/8/12/16	PHY management clock
W21	MDIO	I	0	PD	PU/PD	3.3	4/8/12/16	PHY management data
HDMI								
R23	HDMISD	I	1	-	PD	1.8	5v open-drain	HDMI I2C data
P22	HDMISCK	I	1	-	PD	1.8	5v open-drain	HDMI I2C clock
M22	HDMITX_CH0_M	A				1.8		HDMITX channel 0 M
M23	HDMITX_CH0_P	A				1.8		HDMITX channel 0 P
L22	HDMITX_CH1_M	A				1.8		HDMITX channel 1 M
L23	HDMITX_CH1_P	A				1.8		HDMITX channel 1 P
L25	HDMITX_CH2_M	A				1.8		HDMITX channel 2 M
L24	HDMITX_CH2_P	A				1.8		HDMITX channel 2 P

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		State *1	Aux *2	Pull				
N22	HDMITX_CLK_M	A				1.8		HDMITX channel CK M
N23	HDMITX_CLK_P	A				1.8		HDMITX channel CK P
L20	HDMITX_REXT	A				1.8		External resistor for HDMITX bias
P23	HTPLG	I	1	-	PD	1.8	5v open-drain	HDMI HTPLG pin from HDMI sink
C12	MHL_SENCE	I	0	-	PD	1.8	5v open-drain	MHL Cable Detection Sense Input.
L21	CEC	I	1	-	PD	1.8	5v open-drain	Consumer Electronics Control
PCIe								
AA6	PCIE_VRT_P0	A				3.3		PCIe port0 reference pin
AB6	PCIE_CKN0	A				3.3		PCIe port0 reference clock (negative)
AC6	PCIE_CKP0	A				3.3		PCIe port0 reference clock (positive)
AE4	PCIE_TXN0	A				3.3		PCIe port0 differential transmit TX -
AD4	PCIE_TXP0	A				3.3		PCIe port0 differential transmit TX+
AE6	PCIE_RXN0	A				3.3		PCIe port0 differential receive RX -
AD6	PCIE_RXP0	A				3.3		PCIe port0 differential receive RX +
AB10	PCIE_VRT_P1	A				3.3		PCIe port1 reference pin
AC9	PCIE_CKN1	A				3.3		PCIe port1 reference clock (negative)
AB9	PCIE_CKP1	A				3.3		PCIe port1 reference clock (positive)
AB7	PCIE_TXN1	A				3.3		PCIe port1 differential transmit TX -
AC7	PCIE_TXP1	A				3.3		PCIe port1 differential transmit TX+
AE8	PCIE_RXN1	A				3.3		PCIe port1 differential receive RX -
AD8	PCIE_RXP1	A				3.3		PCIe port1 differential receive RX +
AD10	PCIE_CKN2	A				3.3		PCIe port2 reference clock (negative)
AC10	PCIE_CKP2	A				3.3		PCIe port2 reference clock (positive)
USB								
AC11	SSUSB_VRT_P0	A				3.3		USB port0 reference pin (USB3.0) PCIe port2 reference pin
Y11	USB_DM0	A				3.3		USB port0 HS/FS/LS data pin Data- (USB3.0)
AA11	USB_DP0	A				3.3		USB port0 HS/FS/LS data pin Data+ (USB3.0)
AB12	USB_RXN0	A				3.3		USB port0 SS data pin RX- (USB3.0) PCIe port2 differential receive RX -
AC12	USB_RXP0	A				3.3		USB port0 SS data pin RX+ (USB3.0) PCIe port2 differential receive RX +
AD11	USB_TXN0	A				3.3		USB port0 SS data pin TX- (USB3.0) PCIe port2 differential transmit TX -

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		State *1	Aux *2	Pull					
AE11	USB_TXP0	A				3.3		USB port0 SS data pin TX+ (USB3.0) PCIe port2 differential transmit TX+	
AC18	SSUSB_VRT_P1	A				3.3		USB port1 reference pin (USB3.0)	
W12	USB_DM1	A				3.3		USB port1 data pin Data- (USB3.0)	
Y12	USB_DP1	A				3.3		USB port1 data pin Data+ (USB3.0)	
AB17	USB_RXN1	A				3.3		USB port1 SS data pin RX- (USB3.0)	
AC17	USB_RXP1	A				3.3		USB port1 SS data pin RX+ (USB3.0)	
AD16	USB_TXN1	A				3.3		USB port1 SS data pin TX- (USB3.0)	
AE16	USB_TXP1	A				3.3		USB port1 SS data pin TX+ (USB3.0)	
A13	CHG_DM_P2	A				3.3		USB port2 charger DM (BC1.1)	
B13	CHG_DP_P2	A				3.3		USB port2 charger DP (BC1.1)	
C14	USB_DM_P2	A				3.3		USB port2 data pin Data- (USB2.0 OTG)	
D14	USB_DP_P2	A				3.3		USB port2 data pin Data+ (USB2.0 OTG)	
E14	USB_VBUS_P2	A				3.3		USB port2 power for connected device +3.3V	
B14	USB_VRT_P2	A				3.3		USB port2 reference pin (USB2.0 OTG)	
DDR								**DDR3/L (1.5/1.35V)**	**LPDDR2 (1.2V)**
W4	RDQ0	I/O						Data bit #0	Data bit #23
AA3	RDQ1	I/O						Data bit #1	Data bit #22
W3	RDQ2	I/O						Data bit #2	Data bit #3
AA4	RDQ3	I/O						Data bit #3	Data bit #20
W1	RDQ4	I/O						Data bit #4	Data bit #4
Y1	RDQ5	I/O						Data bit #5	Data bit #2
W2	RDQ6	I/O						Data bit #6	Data bit #3
Y2	RDQ7	I/O						Data bit #7	Data bit #21
AB1	RDQ8	I/O						Data bit #8	Data bit #19
U1	RDQ9	I/O						Data bit #9	Data bit #11
AB2	RDQ10	I/O						Data bit #10	Data bit #16
U2	RDQ11	I/O						Data bit #11	Data bit #12
AB4	RDQ12	I/O						Data bit #12	Data bit #17
V4	RDQ13	I/O						Data bit #13	Data bit #9
AB3	RDQ14	I/O						Data bit #14	Data bit #18
V3	RDQ15	I/O						Data bit #15	Data bit #14
E2	RDQ16	I/O						Data bit #16	Data bit #25
G1	RDQ17	I/O						Data bit #17	Data bit #14

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description	
		State *1	Aux *2	Pull					
E1	RDQ18	I/O						Data bit #18	Data bit #26
G2	RDQ19	I/O						Data bit #19	Data bit #11
F3	RDQ20	I/O						Data bit #20	Data bit #27
G3	RDQ21	I/O						Data bit #21	Data bit #12
F4	RDQ22	I/O						Data bit #22	Data bit #30
G4	RDQ23	I/O						Data bit #23	Data bit #8
J3	RDQ24	I/O						Data bit #24	Data bit #13
D3	RDQ25	I/O						Data bit #25	Data bit #24
J4	RDQ26	I/O						Data bit #26	Data bit #10
D4	RDQ27	I/O						Data bit #27	Data bit #28
H2	RDQ28	I/O						Data bit #28	Data bit #9
D2	RDQ29	I/O						Data bit #29	Data bit #31
H1	RDQ30	I/O						Data bit #30	Data bit #15
D1	RDQ31	I/O						Data bit #31	Data bit #29
N2	RA0	O						Address bit #0	Address bit #11
R4	RA1	O						Address bit #1	Address bit #2
L4	RA2	O						Address bit #2	Address bit #5
N1	RA3	O						Address bit #3	Address bit #6
P1	RA4	O						Address bit #4	Address bit #10
N3	RA5	O						Address bit #5	Address bit #4
R3	RA6	O						Address bit #6	Address bit #3
P6	RA7	O						Address bit #7	Address bit #12
T4	RA8	O						Address bit #8	Address bit #14
M3	RA9	O						Address bit #9	Bank Address bit #2
T2	RA10	O						Address bit #10	Address bit #0
P4	RA11	O						Address bit #11	Address bit #13
P5	RA12	O						Address bit #12	Bank Address #0
N4	RA13	O						Address bit #13	Address bit #15
T3	RA14	O						Address bit #14	Address bit #1
L5	RA15	O						Address bit #15	RCAS
M5	RBA0	O						Bank Address #0	RRAS
P2	RBA1	O						Bank Address #1	Bank Address #1
K3	RBA2	O						Bank Address #2	Address bit #9
K1	RRAS	O						RAS	Address bit #8

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description	
		State *1	Aux *2	Pull					
L2	RCAS	O						CAS	Address bit #7
M4	RWE	O						RWE	RWE
R6	RCLK0	O						Clock	Clock
R5	RCLK0_	O						Clock	Clock
J5	RCLK1	O						Clock	Clock
J6	RCLK1_	O						Clock	Clock
Y4	RDQM0	O						DM#0	DM#2
U3	RDQM1	O						DM#1	DM#0
E4	RDQM2	O						DM#0	DM#3
E5	RDQM3	O						DM#1	DM#1
L1	RCS0	O						CS	CS
K4	RCS1	O						CS	CS
V5	RDQS0	I/O						DQS#0	DQS#2
V6	RDQS0_	I/O						DQS#0	DQS#2
W6	RDQS1	I/O						DQS#1	DQS#0
W5	RDQS1_	I/O						DQS#1	DQS#0
H4	RDQS2	I/O						DQS#0	DQS#3
H5	RDQS2_	I/O						DQS#0	DQS#3
F5	RDQS3	I/O						DQS#1	DQS#1
F6	RDQS3_	I/O						DQS#1	DQS#1
T1	RCKE	O						CKE	CKE
AC2	REXTDN	O						REXTDN	REXTDN
K2	DDR3RSTB	O						Reset	Reset
CVBS									
B18	VDAC_C	A						VDAC CVBS channel output	
MIPI									
AD13	MIPI_TCN	I	1	-	NP	1.8		DSI0 CK lane N	
AE13	MIPI_TCP	I	1	-	NP	1.8		DSI0 CK lane P	
AC15	MIPI_TDN3	I	1	-	NP	1.8		DSI0 lane3 N	
AB15	MIPI_TDP3	I	1	-	NP	1.8		DSI0 lane3 P	
AB14	MIPI_TDN2	I	1	-	NP	1.8		DSI0 lane2 N	
AA14	MIPI_TDP2	I	1	-	NP	1.8		DSI0 lane2 P	
AE15	MIPI_TDN0	I	1	-	NP	1.8		DSI0 lane0 N	
AD15	MIPI_TDP0	I	1	-	NP	1.8		DSI0 lane0 P	

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
AE14	MIPI_TDN1	I	1	-	NP	1.8		DSI0 lane1N
AD14	MIPI_TDP1	I	1	-	NP	1.8		DSI0 lane1 P
AC14	MIPI_VRT	A				1.8		External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground
I2S								
AA19	I2S0_MCLK	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S master clock for CODEC
Y19	I2S0_BCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S bit clock
Y20	I2S0_LRCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S word select
AB18	I2S0_DATA	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S data output
AA20	I2S0_DATA_IN	I	1	PD	PU/PD	3.3	4/8/12/16	I2S data input
AA18	I2S1_MCLK	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S master clock for CODEC
V17	I2S1_BCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S bit clock
W17	I2S1_LRCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S word select
Y18	I2S1_DATA	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S data output
Y17	I2S1_DATA_IN	I	1	PD	PU/PD	3.3	4/8/12/16	I2S data input
PCM								
C25	PCM_CLK	I	0	PD	PU/PD	3.3	4/8/12/16	PCM clock
B25	PCM_SYNC	I	0	PD	PU/PD	3.3	4/8/12/16	PCM frame sync.
D24	PCM_TX	I	0	PD	PU/PD	3.3	4/8/12/16	PCM TX data
D25	PCM_RX	I	0	PD	PU/PD	3.3	4/8/12/16	PCM RX data
SPDIF								
K19	SPDIF_IN0	I	0	PD	PU/PD	3.3	4/8/12/16	SPDIF input channel 0
K18	SPDIF_IN1	I	0	PD	PU/PD	3.3	4/8/12/16	SPDIF input channel 1
J19	SPDIF_OUT	I	0	PD	PU/PD	3.3	4/8/12/16	SPDIF output channel
LCD								
V14	DSI_TE	I	0	PD	PU/PD	1.8	2/4/6/8	DSI tearing effect control
V16	LCM_RST	I	0	PD	PU/PD	1.8	2/4/6/8	LCM reset
WBG								
AB20	WB_CRTL0	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AC20	WB_CRTL1	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AB19	WB_CRTL2	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AC19	WB_CRTL3	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AD19	WB_CRTL4	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AE19	WB_CRTL5	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AB24	WB_SEN	OL	1	PD	PU/PD	1.8	2/4/6/8	SPI for CONN_RF

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
AC23	WB_SCLK	OL	1	PD	PU/PD	1.8	2/4/6/8	SPI for CONN_RF
Y21	WB_RSTB	OL	1	PD	PU/PD	1.8	2/4/6/8	Reset for CONN_RF
AB21	WB_SDATA	I	1	PD	PU/PD	1.8	2/4/6/8	SPI for CONN_RF
AD21	WB_RXIN	A				1.8		RX_IN for WIFI/BT RX
AD22	WB_RXQN	A				1.8		RX_QN for WIFI/BT RX
AD24	WB_TXQP	A				1.8		TX_QP for WIFI/BT TX
AD25	WB_TXQN	A				1.8		TX_QN for WIFI/BT TX
AE21	WB_RXIP	A				1.8		RX_IP for WIFI/BT RX
AE22	WB_RXQP	A				1.8		RX_QP for WIFI/BT RX
AE23	WB_TXIP	A				1.8		TX_IP for WIFI/BT TX
AE24	WB_TXIN	A				1.8		TX_IN for WIFI/BT TX
AC21	TEST_GQP	A				1.8		FT test Pin
AC22	TEST_GQN	A				1.8		FT test Pin
AC24	TEST_GIN	A				1.8		FT test Pin
AC25	TEST_GIP	A				1.8		FT test Pin
AB25	XIN_WBG	A				1.8		26MHz clock input for WBG
PMIC								
H17	PWRAP_INT	I	0	PD	PU/PD	1.8	2/4/6/8	PMIC interrupt
H16	PWRAP_SPI0_MO	OL	1	PD	PU/PD	1.8	2/4/6/8	PMIC SPI data out
G16	PWRAP_SPI0_MI	OL	1	PD	PU/PD	1.8	2/4/6/8	PMIC SPI data in
F16	PWRAP_SPI0_CK	OL	1	PD	PU/PD	1.8	2/4/6/8	PMIC SPI clock
G18	PWRAP_SPI0_CK2	OL	1	PD	PU/PD	1.8	2/4/6/8	GPIO
J16	PWRAP_SPI0_CSN	OH	1	PU	PU/PD	1.8	2/4/6/8	PMIC SPI chip select
H18	PWRAP_SPI0_CSN2	OH	1	PU	PU/PD	1.8	2/4/6/8	GPIO
DAC								
A20	DAC_A_OUTPUT	A				1.8		DAC output
B20	DAC_B_OUTPUT	A				1.8		DAC output
ABB								
K21	REFP	A				1.8		Positive reference port for internal circuit
A24	26M_CLKSQ	A				1.8		26MHz clock input for AP
K22	AUX_IN0	A				1.8		AuxADC external input channel 0
K23	AUX_IN1	A				1.8		AuxADC external input channel 1
J23	AUX_IN2	A				1.8		AuxADC external input channel 2
J22	AUX_IN3	A				1.8		AuxADC external input channel 3

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
H24	AUX_IN4	A				1.8		AuxADC external input channel 4
H25	AUX_IN5	A				1.8		AuxADC external input channel 5
MISC								
A16	RTC32K_CK	I	1	PD	PU/PD	1.8	2/4/6/8	Real time clock 32.768 kHz
B16	SRCLKENAI	I	1	PD	PU/PD	1.8	2/4/6/8	26MHz co-clock enable input
C16	SRCLKENA	OH	1	PU	PU/PD	1.8	2/4/6/8	26MHz co-clock enable output
C17	SYSRSTB	I	-	PU	PU	1.8		Power on reset
D16	WATCHDOG	OH	1	PD	PU/PD	1.8	2/4/6/8	Watchdog reset
K20	TESTMODE	I	-	PD	PD	1.8		Test mode
AE3	FSOURCE_P0	A				1.8		E-FUSE blowing power control
F18	IR	I	0	PD	PU/PD	1.8		Infra red receiver
L8	TP_MEMPLL	A				1.8		PLL test
W14	AUD_EXT_CK1	I	3	PD	PU/PD	3.3	4/8/12/16	Audio clock in1
V15	AUD_EXT_CK2	I	3	PD	PU/PD	3.3	4/8/12/16	Audio clock in2
C9	NC							No connection
D9	NC							No connection
B8	NC							No connection
A8	NC							No connection
D8	NC							No connection
C8	NC							No connection
C10	NC							No connection
D10	NC							No connection
Power								
J10, J11, J14, J9, K10, L10, L9, M9, N8, P14, P9, R13, R14, R8, T12, T8, U11, U12, U8, V7, V8	VCCK	P				1.15		Digital core power supply
K12, K13, K14, K16, L12, L13, L14, L15, M12, M13, M14	VCCK_VPROC	P				0.85 1.05 1.15 1.31		CPU core power supply
AC5	DVDD18_IO	P				1.8		Digital I/O power supply

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
H13	DVDD18_IO_DPI	P				1.8		Digital I/O power supply
AD5	DVDD18_IO_I2S	P				1.8		Digital I/O power supply
F13	DVDD18_IO_MSDC0	P				1.8		Digital I/O power supply
AB5	DVDD18_IO_MSDC1	P				1.8		Digital I/O power supply
G13	DVDD18_IO_NOR	P				1.8		Digital I/O power supply
R16	DVDD18_IO_RGMII	P				1.8		Digital I/O power supply
AE18	DVDD18_IO_WBCT	P				1.8		Digital I/O power supply
AB13	DVDD18_MIPITX	P				1.8		Digital I/O power supply
F9	DVDD28_DPI	P				3.3		Digital I/O power supply
V10	DVDD28_I2S	P				3.3		Digital I/O power supply
G9	DVDD28_MSDC0	P				1.8 3.3		Digital I/O power supply
W9	DVDD28_MSDC1	P				3.3		Digital I/O power supply
E9	DVDD28_NOR	P				3.3		Digital I/O power supply
T7	VREF0	P				0.75 0.675 0.6		DRAM reference voltage power supply
J7, K7, L7, M7, N7, P7, R7	VDD_EMI	P				1.5 1.35 1.2		DRAM I/O power supply
T17	DVDD_GE1_VREF	P				0.9		GE1 reference voltage power supply
T18, U17	DVDD_GE1_IO	P				1.8		GE1 I/O power supply
N17	DVDD28_RGMII	P				3.3		GE2 I/O power supply
Y8	AVDD11_PCIE_P0	P				1.15		PCIe port0 analog power supply
AA8	AVDD11_PCIE_P1	P				1.15		PCIe port1 analog power supply
W13	AVDD11_SSUSB_P0	P				1.15		USB port0 analog power supply
AC16	AVDD11_SSUSB_P1	P				1.15		USB port1 analog power supply
J25	AVDD18_AP	P				1.8		ADC analog power supply
K8	AVDD18_MEMPLL	P				1.8		DRAM PLL analog power supply
AE5	AVDD18_PCIE	P				1.8		PCIe analog power supply
M18	AVDD18_PLLGP	P				1.8		PLL group analog power supply
AA12	AVDD18_SSUSB	P				1.8		SSUSB analog power supply
AE10	AVDD18_USB	P				1.8		USB analog power supply
A14	AVDD18_USB_P2	P				1.8		USB analog power supply
AD18	AVDD18_WBG	P				1.8		WiFi/BT analog power supply
Y10	AVDD33_USB	P				3.3		USB analog power supply

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
D13	AVDD33_USB_P2	P				3.3		USB analog power supply
A11	AVDD18_HDR	P				1.8		Analog power supply
A18	AVDD33_VDAC_C	P				3.3		VDAC analog power supply
A21	AVDD18_DAC	P				1.8		DAC analog power supply
A9	AVDD12_HDR	P				1.2		Analog power supply
F10	AVDD33_HDR	P				3.3		Analog power supply
N25	AVDD18_HDMITX	P				1.8		HDMI TX analog power supply
GROUND								
K9	AVSS18_MEMPLL	G						
AB23, AD23, AE25	AVSS18_WBG	G						
J24	AVSS18_AP	G						
AA7, AC8	AVSS_PCIE	G						
AB11, AB16	AVSS_SSUSB	G						
D12	AVSS_USB_P2	G						
M19	AVSS18_PLLGP	G						
AC13	DVSS18_MIPITX	G						
C18	AVSS33_VDAC_C	G						
B21	AVSS18_DAC	G						
B9	AVSS33_HDR	G						
N24	AVSS18_HDMITX	G						

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Pin	Name	Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
A1, A25, AE1, B24, C3, E3, H23, H3, H6, J12, J13, J8, K11, K6, L11, L16, L17, L3, L6, M10, M11, M15, M17, M20, M6, M8, N10, N11, N12, N13, N14, N15, N16, N18, N19, N21, N6, N9, P10, P11, P12, P13, P15, P20, P3, P8, R10, R11, R12, R15, R9, T10, T11, T15, T21, T9, U19, U20, U4, U5, V23, Y22, Y3	GND	G						Ground

NOTE:

1. I: Input
   O: Output
   OH: Output high
   OL: Output low
   I/O: Bi-directional
   P: Power
   G: Ground
   NC: Not connected
   A: Analog
2. AUX: Aux function. (Please reference to next section for detail.)
3. The internal pull resistance value is 75kΩ.
4. PD: Internal pull-down
   PU: Internal pull-up
   NP: No pull-down/up

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5. GE1 only has turbo(250MHz) and giga(125MHz) mode. And the turbo mode only for MT7530 (Giga Switch).

2.2.1 Constant Tie Pins

Table 2-3: Constant tied pins

Pin name	Description
TESTMODE	Test mode (tie to GND)
FSOURCE_P	EFUSE blowing (tie to GND)

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2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7623N provides up to 159 GPIO pins. Users can configure registers specify the pin function. For more information, see the Programmer's Guide. The pin's default function mode is specified with **bold** type words.

2.3.1 Pin share scheme

Table 2-4 Pin Share

Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
PWRAP_SPI0_MI	148	GPIO0	**B0:PWRAP_SPIDO**	B0:PWRAP_SPIDI				
PWRAP_SPI0_MO	149	GPIO1	**B0:PWRAP_SPIDI**	B0:PWRAP_SPIDO				
PWRAP_INT	150	**GPIO2**	I0:PWRAP_INT					
PWRAP_SPI0_CK	151	GPIO3	**O:PWRAP_SPICK_I**					
PWRAP_SPI0_CSN	152	GPIO4	**O:PWRAP_SPICS_B_I**					
PWRAP_SPI0_CK2	155	GPIO5	**O:PWRAP_SPICK2_I**					
PWRAP_SPI0_CSN2	156	GPIO6	**O:PWRAP_SPICS2_B_I**					
SPI1_CSN	153	**GPIO7**	O:SPI1_CS					
SPI1_MI	154	**GPIO8**	I0:SPI1_MI	O:SPI1_MO				
SPI1_MO	157	**GPIO9**	O:SPI1_MO	I0:SPI1_MI				
RTC32K_CK	158	GPIO10	**I0:RTC32K_CK**					
WATCHDOG	159	GPIO11	**O:WATCHDOG**					
SRCLKENA	160	GPIO12	**O:SRCLKENA**					
SRCLKENAI	161	GPIO13	**I0:SRCLKENAI**					
URXD2	162	**GPIO14**	I1:URXD2	O:UTXD2				
UTXD2	163	**GPIO15**	O:UTXD2	I1:URXD2				
PCM_CLK	166	**GPIO18**	B0:PCM_CLK0					B0:AP_PCM_CLKO
PCM_SYNC	167	**GPIO19**	B0:PCM_SYNC					B0:AP_PCM_SYNC
PCM_RX	N/A	**GPIO20**	I0:PCM_RX			O:PCM_TX		I0:AP_PCM_RX
PCM_TX	N/A	**GPIO21**	O:PCM_TX			I0:PCM_RX		O:AP_PCM_TX
EINT0	0	GPIO22	I1:UCTS0	**O: PCIE0_PERST_N**				
EINT1	1	GPIO23	O:URTS0	**O: PCIE1_PERST_N**				
EINT2	2	GPIO24	I1:UCTS1	**O: PCIE2_PERST_N**				
EINT3	3	**GPIO25**	O:URTS1					
EINT4	4	**GPIO26**	I1:UCTS3					I1: PCIE2_WAKE_N
EINT5	5	**GPIO27**	O:URTS3					I1: PCIE1_WAKE_N
EINT6	6	GPIO28	O:DRV_VBUS					I1: PCIE0_WAKE_N
EINT7	7	GPIO29	**I0:IDDIG**	I0: MSDC1_WP				**O: PCIE2_PERST_N**
I2S1_DATA	15	GPIO33	**B0:I2S1_DATA**		O:PCM_TX			O: AP_PCM_TX
I2S1_DATA_IN	16	GPIO34	**B0:I2S1_DATA_IN**		I0:PCM_RX			I0: AP_PCM_RX
I2S1_BCK	17	GPIO35	**B0:I2S1_BCK**		B0:PCM_CLK0			B0: AP_PCM_CLKO
I2S1_LRCK	18	GPIO36	**B0:I2S1_LRCK**		B0:PCM_SYNC			B0: AP_PCM_SYNC

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Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
I2S1_MCLK	19	GPIO37	**B0:I2S1_MCLK**					
JTMS	21	GPIO39	**B1:JTMS**					
JTCK	22	GPIO40	**I0:JTCK**					
JTDI	23	GPIO41	**I1:JTDI**					
JTDO	24	GPIO42	**O:JTDO**					
NCLE	25	**GPIO43**	O:NCLE	O: SFLASH_CS2_L				
NCEB1	26	**GPIO44**	O:NCEB1	I0:IDDIG				
NCEB0	27	**GPIO45**	O:NCEB0	O:DRV_VBUS				
IR	28	**GPIO46**	I0:IR					
NREB	29	**GPIO47**	O:NREB					
NRNB	30	**GPIO48**	I1:NRNB					
I2S0_DATA	31	GPIO49	**B0:I2S0_DATA**		O:PCM_TX			O: AP_I2S_DO
SPI0_CSN	35	**GPIO53**	O:SPI0_CS		O:SPDIF		O:PWM1	
SPI0_CK	36	**GPIO54**	O:SPI0_CK		I0:SPDIF_IN1			
SPI0_MI	37	**GPIO55**	I0:SPI0_MI	O:SPI0_MO	I0: MSDC1_WP		O:PWM2	
SPI0_MO	38	**GPIO56**	O:SPI0_MO	I0:SPI0_MI	I0:SPDIF_IN0			
SDA1	39	GPIO57	**B1:SDA1**					
SCL1	40	GPIO58	**B1:SCL1**					
WB_RSTB	41	GPIO60	**O:WB_RSTB**					
GPIO61	42	GPIO61	**I0:TEST_FD**					
GPIO62	43	GPIO62	**I0: TEST_FC**					
WB_SCLK	44	GPIO63	**O:WB_SCLK**					
WB_SDATA	45	GPIO64	**B0:WB_SDATA**					
WB_SEN	46	GPIO65	**O:WB_SEN**					
WB_CRTL0	47	GPIO66	**B0:WB_CRTL0**					
WB_CRTL1	48	GPIO67	**B0:WB_CRTL1**					
WB_CRTL2	49	GPIO68	**B0:WB_CRTL2**					
WB_CRTL3	50	GPIO69	**B0:WB_CRTL3**					
WB_CRTL4	51	GPIO70	**B0:WB_CRTL4**					
WB_CRTL5	52	GPIO71	**B0:WB_CRTL5**					
I2S0_DATA_IN	53	GPIO72	**B0:I2S0_DATA_IN**		I0:PCM_RX	O:PWM0	O:DISP_PWM	I0: AP_I2S_DI
I2S0_LRCK	54	GPIO73	**B0:I2S0_LRCK**		B0:PCM_SYNC			B0: AP_I2S_LRCK
I2S0_BCK	55	GPIO74	**B0:I2S0_BCK**		B0:PCM_CLK0			B0: AP_I2S_BCK
SDA0	56	GPIO75	**B1:SDA0**					
SCL0	57	GPIO76	**B1:SCL0**					
SDA2	58	GPIO77	**B1:SDA2**					
SCL2	59	GPIO78	**B1:SCL2**					
URXD0	60	GPIO79	**I1:URXD0**	O:UTXD0				
UTXD0	61	GPIO80	**O:UTXD0**	I1:URXD0				
URXD1	62	**GPIO81**	I1:URXD1	O:UTXD1				
UTXD1	63	**GPIO82**	O:UTXD1	I1:URXD1				

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Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
LCM_RST	64	**GPIO83**	O:LCM_RST					
DSI_TE	65	**GPIO84**	I0:DSI_TE					
MIPI_TDN3	N/A	GPI91	**O:MIPI_TDN3**					
MIPI_TDP3	N/A	GPI92	**O: MIPI_TDP3**					
MIPI_TDN2	N/A	GPI93	**O: MIPI_TDN2**					
MIPI_TDP2	N/A	GPI94	**O: MIPI_TDP2**					
MIPI_TCN	N/A	GPI95	**O: MIPI_TCN**					
MIPI_TCP	N/A	GPI96	**O: MIPI_TCP**					
MIPI_TDN1	N/A	GPI97	**O: MIPI_TDN1**					
MIPI_TDP1	N/A	GPI98	**O: MIPI_TDP1**					
MIPI_TDN0	N/A	GPI99	**O: MIPI_TDN0**					
MIPI_TDP0	N/A	GPI100	**O: MIPI_TDP0**					
SPI2_CSN	74	**GPIO101**	O:SPI2_CS		B1:SCL3			
SPI2_MI	75	**GPIO102**	I0:SPI2_MI	O:SPI2_MO	B1:SDA3			
SPI2_MO	76	**GPIO103**	O:SPI2_MO	I0:SPI2_MI	B1:SCL3			
SPI2_CK	77	**GPIO104**	O:SPI2_CK		B1:SDA3			
MSDC1_CMD	78	GPIO105	**B0:MSDC1_CMD**		B1:SDA1			O:I2SOUT_BCK
MSDC1_CLK	79	GPIO106	**O:MSDC1_CLK**		B1:SCL1			O:I2SOUT_LRCK
MSDC1_DAT0	80	GPIO107	**B0:MSDC1_DAT0**				O:UTXD0	O:I2SOUT_DATA_OUT
MSDC1_DAT1	81	GPIO108	**B0:MSDC1_DAT1**		O:PWM0		I1:URXD0	O:PWM1
MSDC1_DAT2	82	GPIO109	**B0:MSDC1_DAT2**		B1:SDA2		O:UTXD1	O:PWM2
MSDC1_DAT3	83	GPIO110	**B0:MSDC1_DAT3**		B1:SCL2		I1:URXD1	O:PWM3
MSDC0_DAT7	84	GPIO111	**B0:MSDC0_DAT7**			B0:NLD7		
MSDC0_DAT6	85	GPIO112	**B0:MSDC0_DAT6**			B0:NLD6		
MSDC0_DAT5	86	GPIO113	**B0:MSDC0_DAT5**			B0:NLD5		
MSDC0_DAT4	87	GPIO114	**B0:MSDC0_DAT4**			B0:NLD4		
MSDC0_RSTB	88	GPIO115	**O:MSDC0_RSTB**			B0:NLD8		
MSDC0_CMD	89	GPIO116	**B0:MSDC0_CMD**			O:NALE		
MSDC0_CLK	90	GPIO117	**O:MSDC0_CLK**			O:NWEB		
MSDC0_DAT3	91	GPIO118	**B0:MSDC0_DAT3**			B0:NLD3		
MSDC0_DAT2	92	GPIO119	**B0:MSDC0_DAT2**			B0:NLD2		
MSDC0_DAT1	93	GPIO120	**B0:MSDC0_DAT1**			B0:NLD1		
MSDC0_DAT0	94	GPIO121	**B0:MSDC0_DAT0**			B0:NLD0	O:WATCHDOG	
CEC	95	GPIO122	**B0:CEC**			B1:SDA2	I1:URXD0	
HTPLG	96	GPIO123	**I0:HTPLG**			B1:SCL2	O:UTXD0	
HDMISCK	97	GPIO124	**B0:HDMISCK**			B1:SDA1	O:PWM3	
HDMISD	98	GPIO125	**B0:HDMISD**			B1:SCL1	O:PWM4	
I2S0_MCLK	99	GPIO126	**B0:I2S0_MCLK**					O: AP_I2S_MCLK
SPI1_CK	111	**GPIO199**	O:SPI1_CK					
SPDIF_OUT	112	**GPIO200**	O:SPDIF_OUT					I1:URXD2
SPDIF_IN0	113	**GPIO201**	I0:SPDIF_IN0					O:UTXD2

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SPDIF_IN1	114	**GPIO202**	I0:SPDIF_IN1					
PWM0	115	**GPIO203**	O:PWM0	O:DISP_PWM				
PWM1	116	**GPIO204**	O:PWM1					
PWM2	117	**GPIO205**	O:PWM2					
PWM3	118	**GPIO206**	O:PWM3					
PWM4	119	**GPIO207**	O:PWM4					
AUD_EXT_CK1	120	GPIO208	I0:AUD_EXT_CK1	O:PWM0	**O: PCIE0_PERST_N**		O:DISP_PWM	
AUD_EXT_CK2	121	GPIO209	I0:AUD_EXT_CK2	I0: MSDC1_WP	**O: PCIE1_PERST_N**		O:PWM1	
SFLASH_IO_3	122	**GPIO236**	B0: SFLASH_IO_3	I0:IDDIG				
SFLASH_IO_2	123	**GPIO237**	B0: SFLASH_IO_2	O:DRV_VBUS				
SFLASH_IO_1	124	**GPIO238**	B0: SFLASH_IO_1					
SFLASH_IO_0	125	**GPIO239**	B0: SFLASH_IO_0					
SFLASH_CS_L	126	**GPIO240**	O:SFLASH_CS_L					
SFLASH_CLK	127	**GPIO241**	O:SFLASH_CLK					
URTS2	128	**GPIO242**	O:URTS2	O:UTXD3	I1:URXD3	B1:SCL1		
UCTS2	129	**GPIO243**	I1:UCTS2	I1:URXD3	O:UTXD3	B1:SDA1		
GPIO244	130	GPIO244	**B0: TEST_HRSD**					
GPIO245	131	GPIO245	**B0:TEST_HRSC**					
MHL_SENCE	132	**GPIO246**						
GPIO247	N/A	GPIO247	**I0: TEST_HRCB**					
GPIO248	133	GPIO248	**O:TEST_HT**					
GPIO250	135	GPIO250	**B0: TEST_MD7**					I1: PCIE0_CLKREQ_N
GPIO251	136	GPIO251	**B0: TEST_MD6**					I1: PCIE0_WAKE_N
GPIO252	137	GPIO252	**B0: TEST_MD5**					I1: PCIE1_CLKREQ_N
GPIO253	138	GPIO253	**B0: TEST_MD4**					I1: PCIE1_WAKE_N
GPIO254	139	GPIO254	**B0: TEST_MD3**					I1: PCIE2_CLKREQ_N
GPIO255	140	GPIO255	**B0: TEST_MD2**					I1: PCIE2_WAKE_N
GPIO256	141	GPIO256	**B0: TEST_MD1**					
GPIO257	142	GPIO257	**B0: TEST_MD0**					
MSDC1_INS	146	**GPIO261**	I0:MSDC1_INS					
G2_TXEN	N/A	**GPIO262**	B0: G2_TXEN					
G2_TXD3	N/A	**GPIO263**	B0: G2_TXD3					
G2_TXD2	N/A	**GPIO264**	B0: G2_TXD2					
G2_TXD1	N/A	**GPIO265**	B0: G2_TXD1					
G2_TXD0	N/A	**GPIO266**	B0: G2_TXD0					
G2_TXCLK	N/A	**GPIO267**	B0: G2_TXC					
G2_RXCLK	N/A	**GPIO268**	B0: G2_RXC					
G2_RXD0	N/A	**GPIO269**	B0: G2_RXD0					
G2_RXD1	N/A	**GPIO270**	B0: G2_RXD1					
G2_RXD2	N/A	**GPIO271**	B0: G2_RXD2					
G2_RXD3	N/A	**GPIO272**	B0: G2_RXD3					

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Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
G2_RXDV	N/A	**GPIO274**	B0: G2_RXDV					
MDC	N/A	**GPIO275**	O: MDC					
MDIO	N/A	**GPIO276**	B0: MDIO					
JTAG_RESET	147	**GPIO278**	I0:JTAG_RESET					

Note:
" Bold" = Default function mode.
"O" = output function
"I0" = input function, high active
"I1" = input function, low active
"B0" = bi-direction function, high active
"B1" = bi-direction function, low active

2.3.2 EINT Usage Tips

For the GPIOs used ad external interrupt source, there are some notes need take attention.

Pin Name	Notes
EINT0	Need Enable De-bounce Feature
EINT1	Need Enable De-bounce Feature
EINT2	Need Enable De-bounce Feature
EINT3	Need Enable De-bounce Feature
EINT4	Need Enable De-bounce Feature
EINT5	Need Enable De-bounce Feature
EINT6	Need Enable De-bounce Feature
EINT7	Need Enable De-bounce Feature

2.3.3 MIPI GPIO Usage Tips

MIPI pins are listed in below table, and they are analog and digital share pins. In GPIO mode, these MIPI pins can only be use as GPI pins, and can't be used as GPO pins. In order to get the good performance, all these pins are either in MIPI CSI mode or in GPI mode, and it is not suggested that part of these pins are in MIPI CSI mode and other pins are in GPI mode.

Pin Name	Notes
PAD_TDN3	GPI91
PAD_TDP3	GPI92
PAD_TDN2	GPI93

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Pin Name	Notes
PAD_TDP2	GPI94
MIPI_TCN	GPI95
MIPI_TCP	GPI96
MIPI_TDN1	GPI97
MIPI_TDP1	GPI98
MIPI_TDN0	GPI99
MIPI_TDP0	GPI100

2.3.4 xMII PHY/MAC Pin Mapping

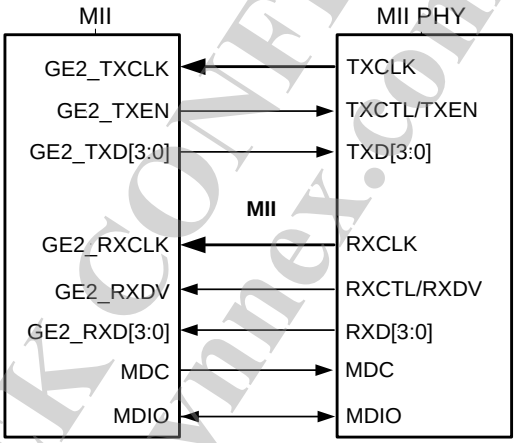

Figure 2-1 MII → MII PHY

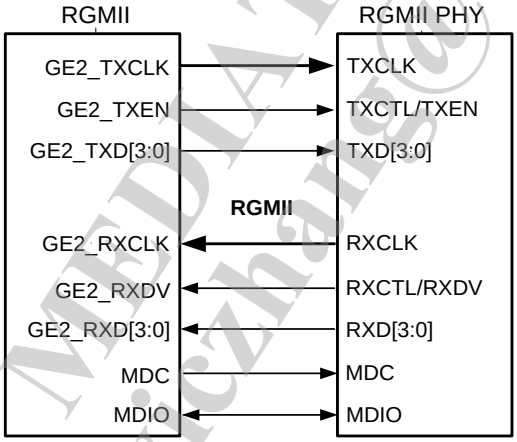

Figure 2-2 RGMII → RGMII PHY

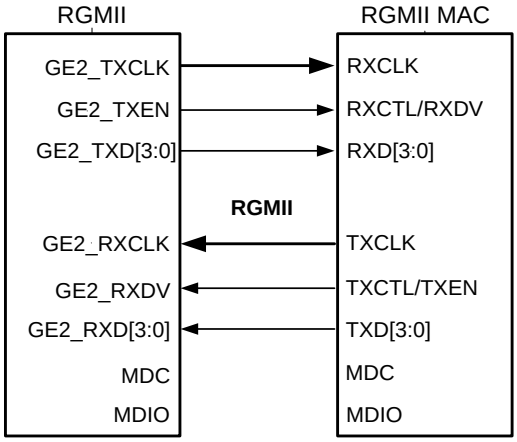

Figure 2-3 RGMII→ RGMII MAC

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2.4 Strapping Options

Table 2-5 Strapping

Pin Name	Strapping Name	Description
{NCLE, NREB}	Boot Order	0: eMMC → USB DL → SD-Card → NAND 1: NAND → USB DL → SD-Card → eMMC 2: USB DL → SD-Card → eMMC → NAND 3: USB DL → SD-Card → eMMC → NAND
JTAG_RESET	Boot Download Mode	0: Trigger USB DL directly 1: According to strapping boot order

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD28_DPI DVDD28_I2S DVDD28_MSDC0 DVDD28_MSDC1 DVDD28_NOR DVDD28_RGMII	3.3V supply voltage	-0.3	3.63	V
AVDD33_USB AVDD33_USB_P2 AVDD33_VDAC_C AVDD33_HDR	3.3V supply voltage	-0.3	3.465	V
DVDD18_IO DVDD18_IO_DPI DVDD18_IO_I2S DVDD18_IO_MSDC0 DVDD18_IO_MSDC1 DVDD18_IO_NOR DVDD18_IO_RGMII DVDD18_IO_WBCT DVDD18_MIPITX DVDD28_MSDC0 DVDD_GE1_IO	1.8V supply voltage	-0.3	2.1	V
AVDD18_AP AVDD18_MEMPLL AVDD18_PCIE AVDD18_PLLGP AVDD18_SSUSB AVDD18_USB AVDD18_USB_P2 AVDD18_WBG AVDD18_HDR AVDD18_DAC AVDD18_HDMITX	1.8V supply voltage	-0.3	1.89	V
VDD_EMI	1.5V supply voltage	-0.3	1.9	V
	1.35V supply voltage	-0.3	1.9	V
	1.2V supply voltage	-0.3	1.9	V
AVDD11_PCIE_P0 AVDD11_PCIE_P1 AVDD11_SSUSB_P0 AVDD11_SSUSB_P1 AVDD12_HDR	1.15V supply voltage	-0.3	1.2	V

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3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD28_DPI DVDD28_I2S DVDD28_MSDC0 DVDD28_MSDC1 DVDD28_NOR DVDD28_RGMII	3.3V supply voltage	2.97	3.3	3.63	V
AVDD33_USB AVDD33_USB_P2 AVDD33_VDAC_C AVDD33_HDR	3.3V supply voltage	3.135	3.3	3.465	V
DVDD18_IO DVDD18_IO_DPI DVDD18_IO_I2S DVDD18_IO_MSDC0 DVDD18_IO_MSDC1 DVDD18_IO_NOR DVDD18_IO_RGMII DVDD18_IO_WBCT DVDD18_MIPITX DVDD28_MSDC0 DVDD_GE1_IO	1.8V supply voltage	1.62	1.8	1.98	V
AVDD18_AP AVDD18_MEMPLL AVDD18_PCIE AVDD18_PLLGP AVDD18_SSUSB AVDD18_USB AVDD18_USB_P2 AVDD18_WBG AVDD18_HDR AVDD18_DAC AVDD18_HDMITX	1.8V supply voltage	1.71	1.8	1.89	V
VDD_EMI	1.5V supply voltage	1.425	1.5	1.575	V
	1.35V supply voltage	1.215	1.35	1.485	V
	1.2V supply voltage	1.14	1.2	1.3	V
AVDD11_PCIE_P0 AVDD11_PCIE_P1 AVDD11_SSUSB_P0 AVDD11_SSUSB_P1 AVDD12_HDR	1.15V supply voltage	1.0925	1.15	1.2075	V
VCCK	Digital core supply voltage	1.035	1.15	1.265	V
VCCK_VPROC *1	Digital processor supply voltage	0.85	1.15	1.31	V

Note: the voltage range is for CPU DVFS turn on.

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3.3 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

Table 3-3 Thermal Characteristics

Symbol	Description	Performance	
		Typ	Unit
T_J	Maximum junction temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance for JEDEC 4L system PCB	19.26	°C/W
θ_{JA}	Thermal Resistance for 6L RFB PCB	17.91	°C/W
θ_{JC}	Thermal Resistance for JEDEC system PCB	6.59	°C/W
ψ_{Jt}	Thermal Characterization parameter for JEDEC 4L system PCB	2.68	°C/W
ψ_{Jt}	Thermal Characterization parameter for 6L RFB PCB	3.14	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4”x4.5”)

Symbol	Parameters	Min.	Typ.	Max.	Unit
Tc	Case Temperature	-10	-	113	C

Note: The device is mounted on a 4L PCB, 200 x 170 x 1.6mm, natural convection and without thermal solution.

3.4 Current Consumption

Please check with application note.

Table 3-4 Current Consumption

3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 0 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.6 External XTAL Specification

Table 3-5 External XTAL Specifications

Frequency	26 Mhz
Amplitude	350(min)/500(typ.)/1000(max) mV
Duty cycle	50+-5%

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3.7 AC Electrical Characteristics

3.7.1 DDR SDRAM Interface

The LPDDR2 SDRAM interface complies with 533 MHz timing requirements for standard LPDDR2 SDRAM. The interface drivers are SSTL_12 drivers matching the EIA/JEDEC standard JESD209-2B.

Table 3-6 LPDDR2 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Average clock period	1.875	100	ns	
tCH(avg)	Average clock high pulse width	0.45	0.55	tCK(avg)	
tCL(avg)	Average clock low pulse width	0.45	0.55	tCK(avg)	
tCH(abs)	Absolute clock high pulse width	0.43	0.57	tCK(avg)	
tCL(abs)	Absolute clock low pulse width	0.43	0.57	tCK(avg)	
tCKE	CKE min. pulse width	3	-	tCK(avg)	
tIS	Command/Address setup time to CK	220	-	ps	
tIH	Command/Address hold time from CK	220	-	ps	
tDQSCK	DQS output access time from SDRAM CLK	2500	5500	ps	
tDQSQ	Data skew of DQS and associated DQ	-	200	ps	
tQHS	Data hold skew factor	-	230	ps	
tQSH	DQS Output High Pulse Width	tCH(abs) - 0.05	-	tCK(avg)	
tQSL	DQS Output Low Pulse Width	tCL (abs) - 0.05	-	tCK(avg)	
tQHP	Data Half Period	min(tQSH,tQSL)		tCK(avg)	
tQH	DQ/DQS output hold time from DQS	tQHP - tQHS	-	ns	
tRPRE	Read preamble	0.9	-	tCK(avg)	
tRPST	Read postamble	tCL(abs) - 0.05	-	tCK(avg)	
tDH	DQ and DQM input hold time	210	-	ps	
tDS	DQ and DQM input setup time	210	-	ps	
tDIPW	DQ and DM input pulse width	0.35	-	tCK(avg)	
tDQSS	Write command to 1st DQS latching transition	0.75	1.25	tCK(avg)	
tDQSH	DQS input high pulse width	0.4	-	tCK(avg)	
tDQSL	DQS input low pulse width	0.4	-	tCK(avg)	
tDSS	DQS falling edge setup time to CK	0.2	-	tCK(avg)	
tDSH	DQS falling edge hold time from CK	0.2	-	tCK(avg)	

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Symbol	Description	Min	Max	Unit	Remark
tWPRE	DQS write preamble	0.35	-	tCK(avg)	
tWPST	DQS write postamble	0.4	-	tCK(avg)	

The DDR3 SDRAM interface complies with 800 MHz timing requirements for standard DDR3 SDRAM. The interface drivers are SSTL_15 drivers matching the EIA/JEDEC standard JESD79-3E.

Table 3-7 DDR3 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Average clock period	1.25	-	ns	
tCH(avg)	Average clock high pulse width	0.47	0.53	tCK(avg)	
tCL(avg)	Average clock low pulse width	0.47	0.53	tCK(avg)	
tCH(abs)	Absolute clock high pulse width	0.43	-	tCK(avg)	
tCL(abs)	Absolute clock low pulse width	0.43	-	tCK(avg)	
tIS	Command/Address setup time to CK	170	-	ps	
tIH	Command/Address hold time from CK	120	-	ps	
tDQSCK	DQS output access time from CK	-225	225	ps	
tDQSQ	Data skew of DQS and associated DQ	-	100	ps	
tQSH	DQS output high time	0.4	-	tCK(avg)	
tQSL	DQS output low time	0.4	-	tCK(avg)	
tQH	DQ/DQS output hold time from DQS	0.38	-	tCK(avg)	
tRPRE	DQS read preamble	0.9	-	tCK(avg)	
tRPST	DQS read postamble	0.3	-	tCK(avg)	
tDH	DQ hold time from DQS	45	-	ps	
tDS	DQ setup time to DQS	10	-	ps	
tDIPW	DQ and DM input pulse width	360	-	Ps	
tDQSS	DQS rising edge to CK rising edge	-0.27	0.27	tCK(avg)	
tDQSH	DQS input high pulse width	0.45	0.55	tCK(avg)	
tDQSL	DQS input low pulse width	0.45	0.55	tCK(avg)	
tDSS	DQS falling edge setup time to CK	0.18	-	tCK(avg)	
tDSH	DQS falling edge hold time from CK	0.18	-	tCK(avg)	
tWPRE	DQS write preamble	0.9	-	tCK(avg)	
tWPST	DQS write postamble	0.3	-	tCK(avg)	

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3.7.2 RGMII Interface

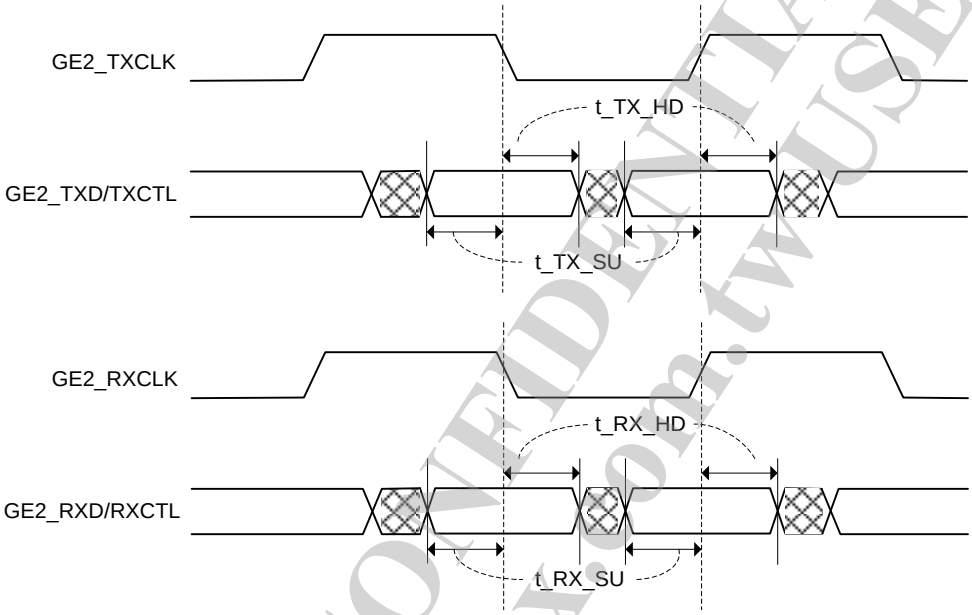

Figure 3-1 RGMII Timing

Table 3-8 RGMII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. GE0_TXD*, GE0_TXEN)	1.2	-	ns	output load: 5 pF
t_TX_HD	Hold time for output signals	1.2	-	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

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3.7.3 MII Interface (25 Mhz)

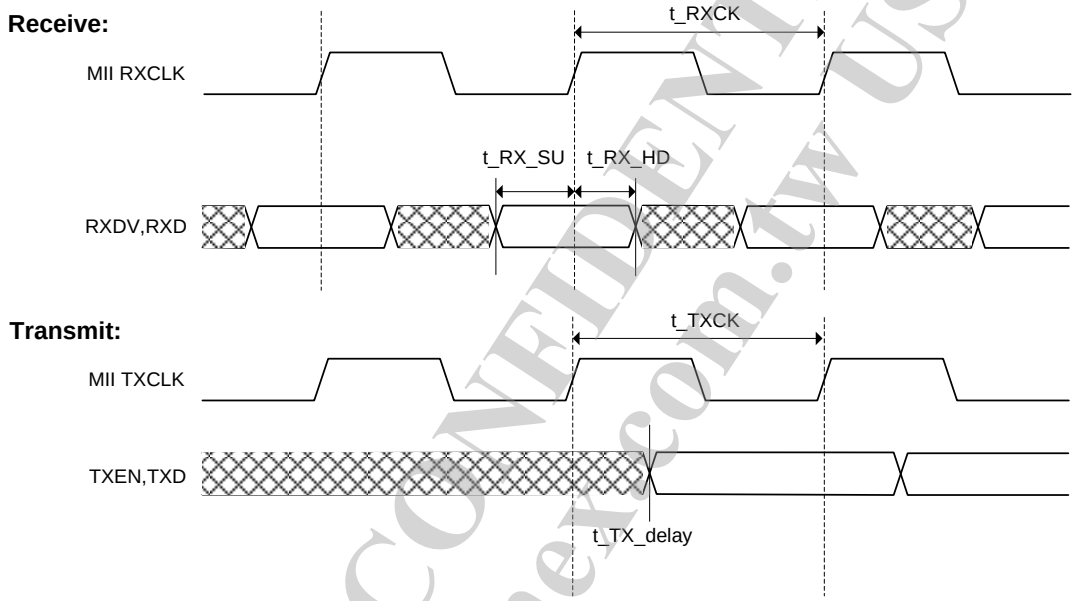

Figure 3-2 MII Timing

Table 3-9 MII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Delay to output signals (e.g. GE0_TXD*, GE0_TXEN)	6	22	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	10	-	ns	
t_RX_HD	Hold time for input signals	5	-	ns	

Note: For 25 Mhz TXCLK & RXCLK

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3.7.4 SPI Interface

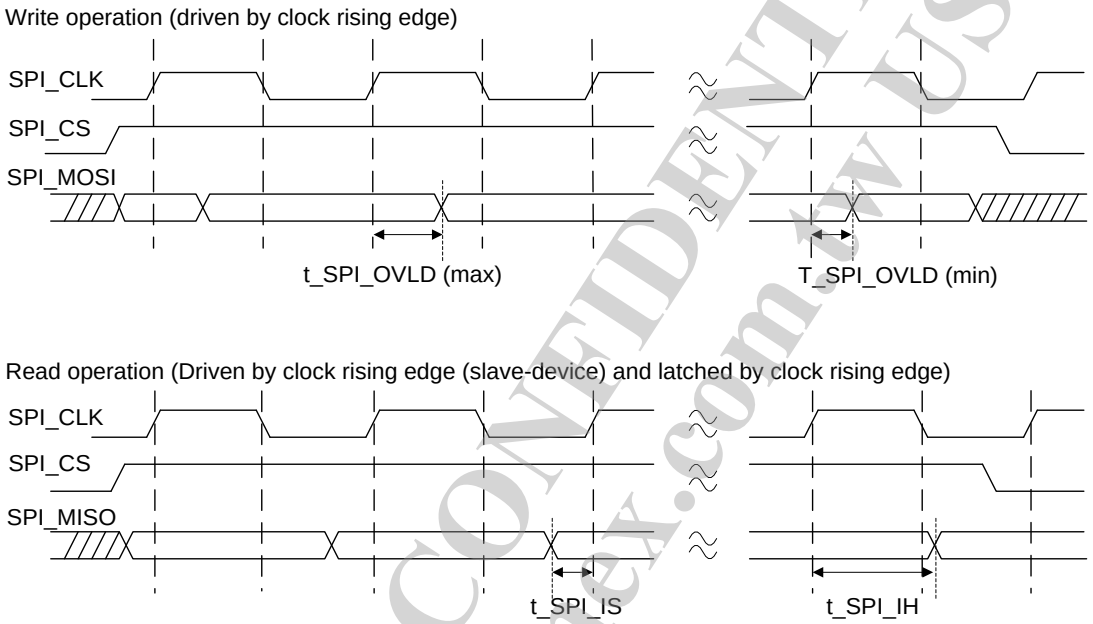

Figure 3-3 SPI Timing

Table 3-10 SPI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_SPI_IS	Setup time for SPI input	6.0	-	ns	
t_SPI_IH	Hold time for SPI input	-1.0	-	ns	
t_SPI_OVLD	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5 pF

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3.7.5 I2S Interface

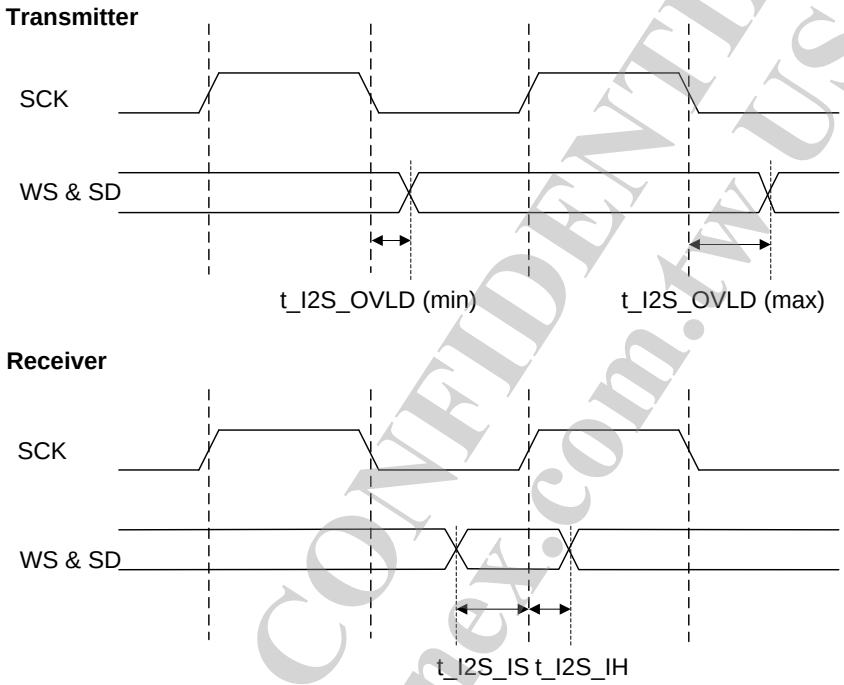

Figure 3-4 I2S Timing

Table 3-11 I2S Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_I2S_IS	Setup time for I2S input (data & WS)	3.5	-	ns	
t_I2S_IH	Hold time for I2S input (data & WS)	0.5	-	ns	
t_I2S_OVLD	I2S_CLK to I2S output (data & WS) valid	2.5	10.0	ns	output load: 5 pF

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3.7.6 PCM Interface

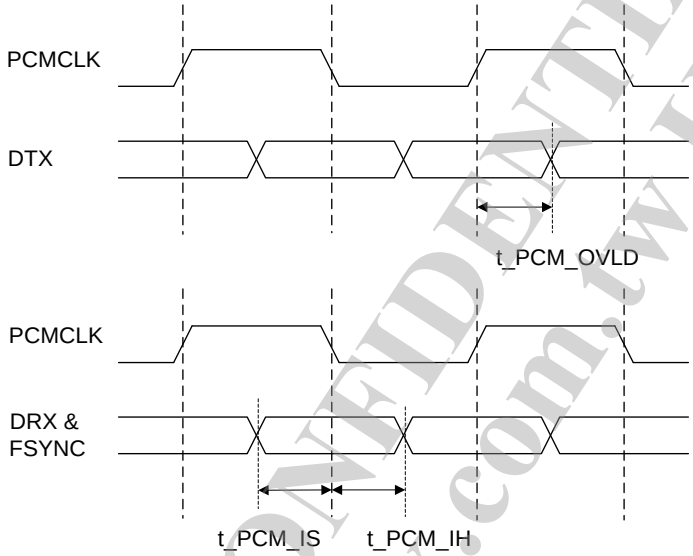

Figure 3-5 PCM Timing

Table 3-12 PCM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_PCM_IS	Setup time for PCM input to PCM_CLK fall	3.0	-	ns	
t_PCM_IH	Hold time for PCM input to PCM_CLK fall	1.0	-	ns	
t_PCM_OVLD	PCM_CLK rise to PCM output valid	10.0	35.0	ns	output load: 5 pF

3.7.7 I2C Interface

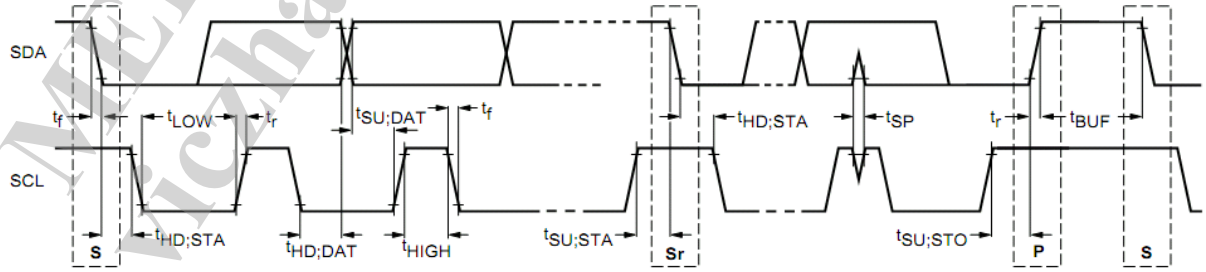

Figure 3-6 I2C Timing

Table 3-13 I2C Interface Diagram Key

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Symbol	Description	Min	Max	Unit	Remark
fSCL	SCL clock frequency	0	400	kHz	
tBUF	Bus free time between a STOP and START condition	1.3	-	us	
tHD	Hold time (repeated) START condition. After this period, the first clock pulse is generated	-	-	us	
tLOW	LOW period of the SCL clock	1.3	-	us	
tHIGH	HIGH period of the SCL clock	0.6		us	
tSU:STA	Setup time for a repeated START condition	0.6	-	us	
Thd:DAT	Data hold time:	-	-	us	
tSU:DAT	Data setup time	100	-	ns	
tr	Rise time of both SDA and SCL signals	20	300	ns	
tf	Fall time of both SDA and SCL signals	20	300	ns	
tSU:STO	Setup time for STOP condition	0.6	-	us	

3.7.8 SDIO Interface

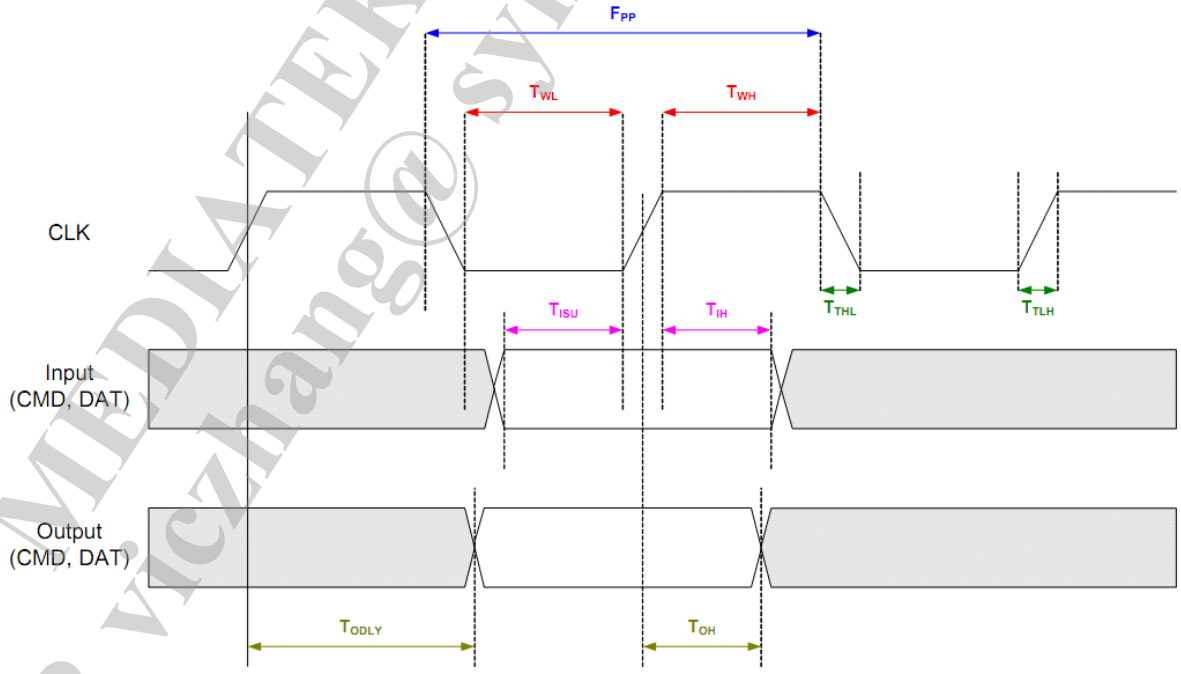

Figure 3-7 SDIO Timing

Table 3-14 SDIO Interface Diagram Key

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Symbol	Description	Min	Max	Unit	Remark
fPP	Clock frequency data transfer mode	0	50	MHz	
tWL	Clock low	7		ns	
tWH	Clock high	7		ns	
tTLH	Clock rise		3	ns	
tTHL	Clock fll		3	ns	
tISU	Input setup	6		ns	
tIH	Input hold	2		ns	
tOH	Output hold	2.5		ns	
tO_DLY(max)	Output dellay time	0	14	ns	

3.7.9 NAND Flash Interface (Samsung Compatible Device)

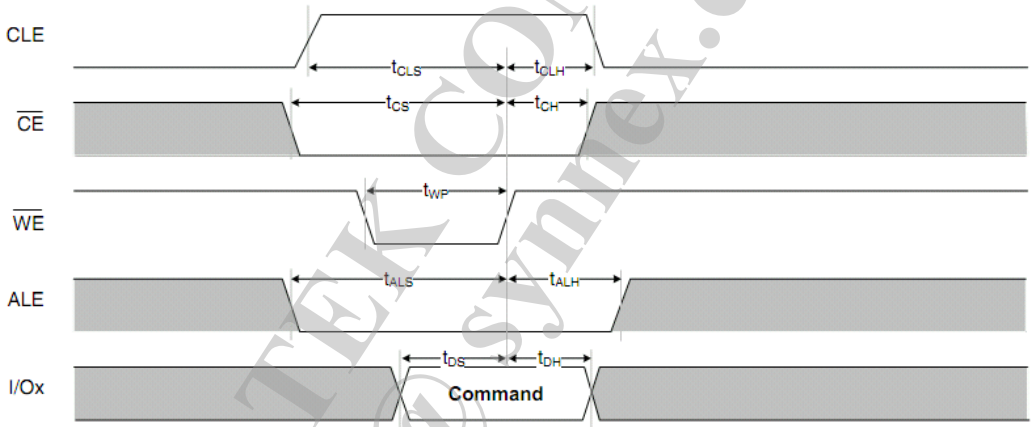

Figure 3-8 NAND Flash Command Timing

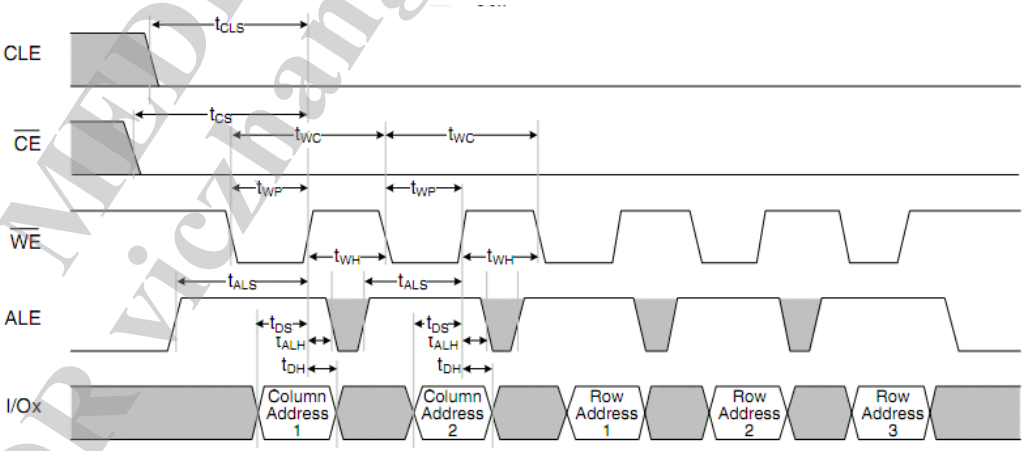

Figure 3-9 NAND Flash Address Latch Timing

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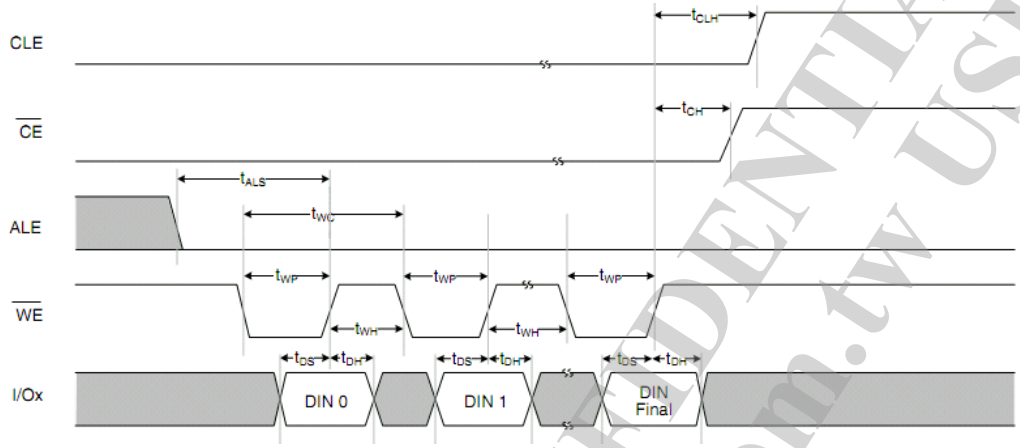

Figure 3-10 NAND Flash Write Timing

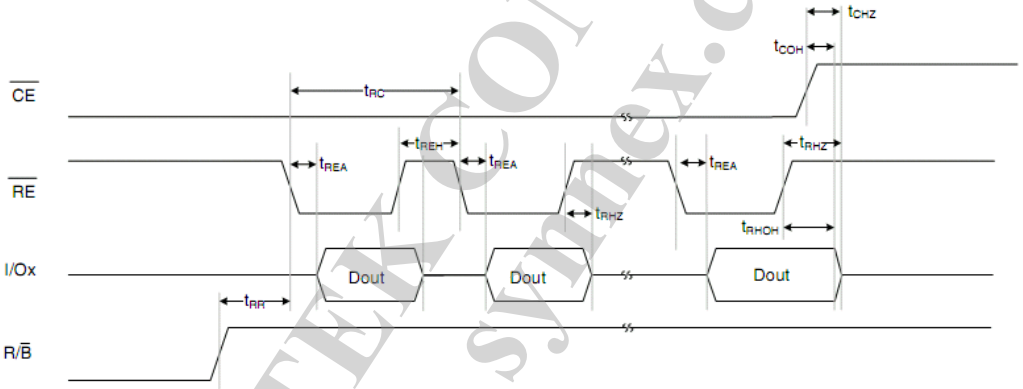

Figure 3-11 NAND Flash Read Timing

Table 3-15 NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCLS	CLE setup time	12	-	ns	
tCLH	CLE hold time	5		ns	
Tcs	CE setup time	20		ns	
tCH	CE hold time	5		ns	
tWP	WE pulse width	12		ns	
tALS	ALE setup time	12		ns	
tALH	ALE hold time	5		ns	
tDS	Data setup time	15		ns	
tDH	Data hold time	5		ns	
tWC	Write cycle time	25		ns	

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Symbol	Description	Min	Max	Unit	Remark
tWH	WE high hold time	10		ns	

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3.8 Power On Sequence

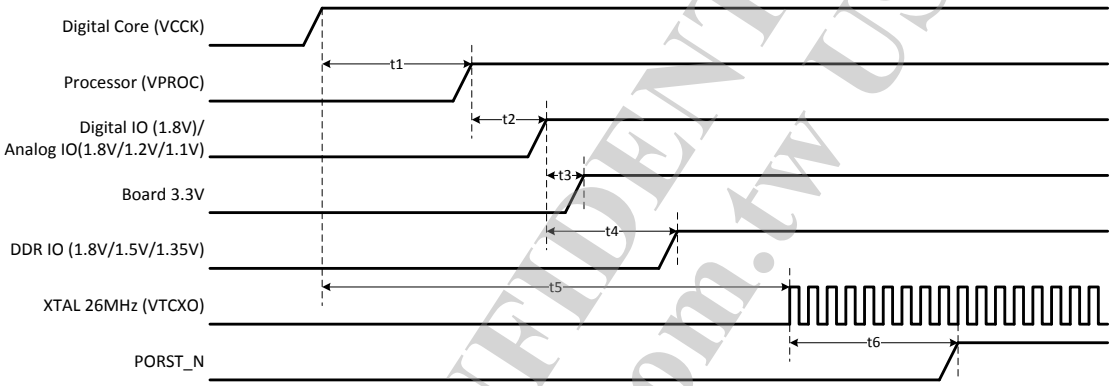

Figure 3-12 Power ON Sequence

Table 3-16 Power ON Sequence Diagram Key

Symbol	Description	Min	Max	Unit
t1	Digital core power on to processer(CA7) power on	8	10	ms
t2	Processor(CA7) power on to digital IO(1.8V) and analog IO(1.8V/1.2V/1.1V) power on	2	4	ms
t3	Digital IO power(1.8V) on to board 3.3V power on	2	4	ms
t4	Digital IO power(1.8V) on to DDR IO(1.8V/1.5V/1.35V) power on	6	8	ms
t5	Digital core power on to XTAL start	0	30	ms
t6	XTAL start to PORST_N de-assertion	41	164	ms

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4 Package Information

4.1 Dimensions - FBGA (21 x 21mm)

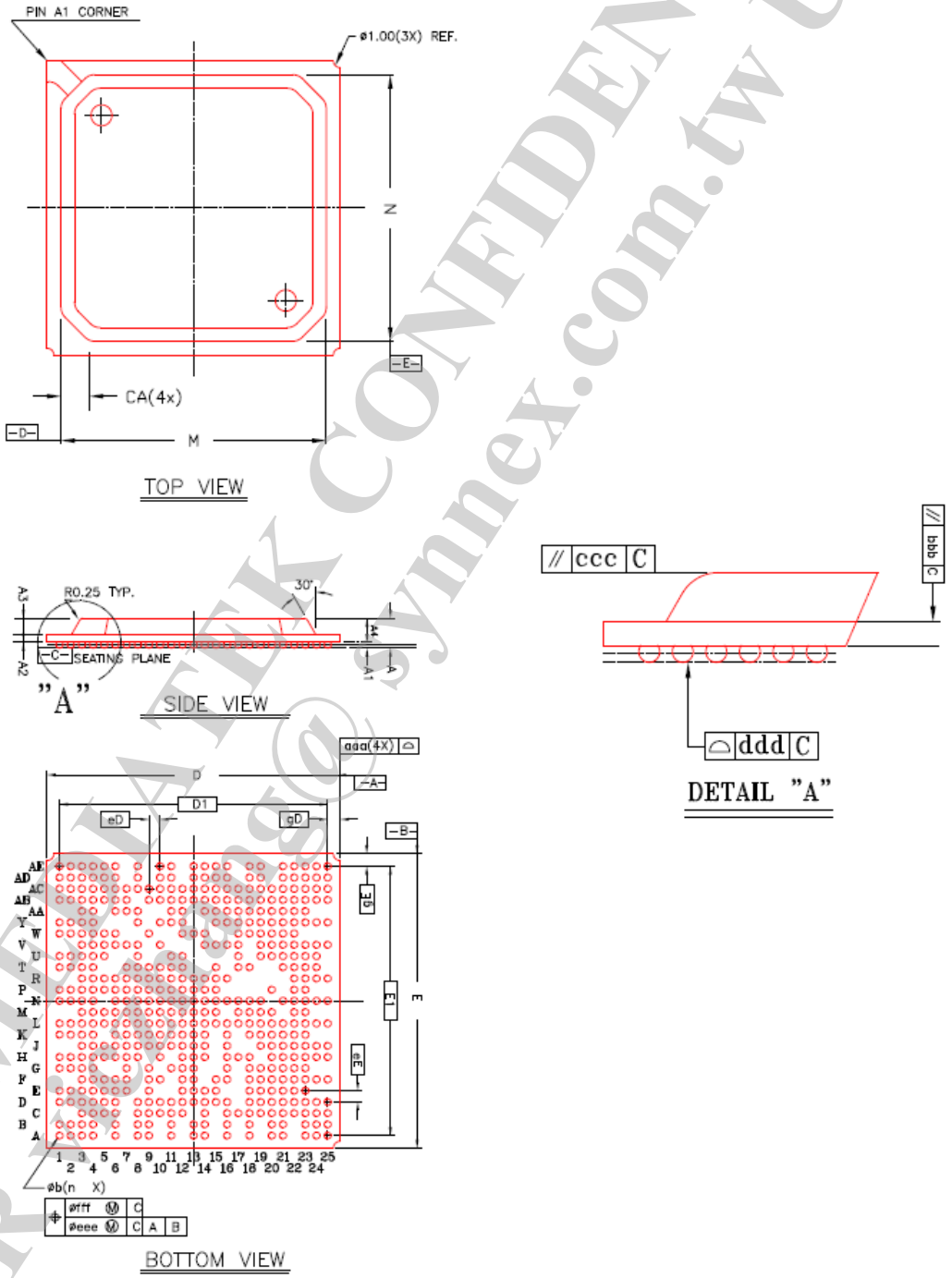

Figure 4-1 Package Dimension

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4.1.1 Diagram Key

Table 4-1 Package Diagram Key

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			FBGA		
Body Size	X	D	20.85	21	21.15
	Y	E	20.85	21	21.15
Ball Pitch	X	eD		0.80	
	Y	eE		0.80	
Mold Thickness		A3		1.17 Ref.	
Substrate Thickness		A2		0.56 Ref.	
Substrate+Mold Thickness		A4	1.66	1.73	1.80
Total Thickness		A	2.00	2.13	2.26
Ball Diameter				0.50	
Ball Stand Off		A1	0.35	0.40	0.45
Ball Width		b	0.45	0.50	0.55
Mold Area	X	M		19.00	
	Y	N		19.00	
Chamfer		CA		2.00*45°	
Package Edge Tolerance		aaa		0.15	
Substrate Flatness		bbb		0.10	
Mold Flatness		ccc		0.20	
Coplanarity		ddd		0.15	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.08	
Ball Count		n		485	
Edge Ball Center to Center	X	D1		19.20	
	Y	E1		19.20	
Edge Ball Center to Package Edge	X	gD		0.90	
	Y	gE		0.90	

NOTE:

1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: bbb, ddd.
5. The pattern of pin 1 fiducial is for reference only.

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4.2 Reflow Profile Guideline

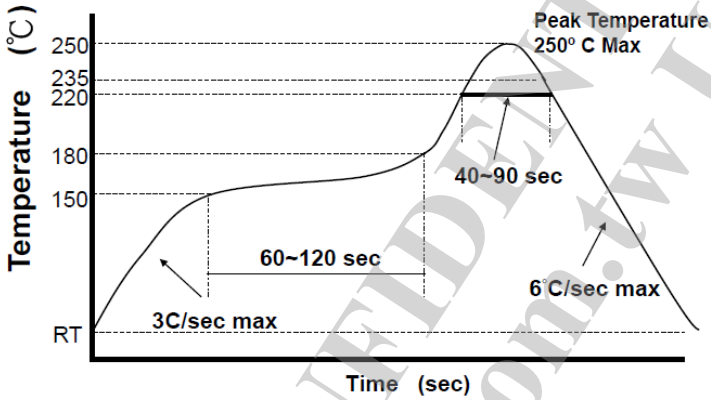

Figure 4-2 Reflow profile

Notes:

1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

4.3 Top Marking

MT7623NI: Part number
YYWW: Date code
####: Internal control code
LLLLLLLLL: Lot number
".": Pin #1 dot

Figure 4-3 Top marking

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4.4 Ordering Information

Part Number	Package (Green/RoHS Compliant)
MT7623NI	21 x 21mm, 485-balls FBGA

Note: a heat sink is required in max ambient temperature.

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