MT7986A Datasheet

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Overview

MT7986A is a highly integrated wireless network router system-on-chip used for high wireless performance, home entertainment, and home automation and so on.

Applications:
- Internet Service Router
- Wireless Router
- Wireless Repeater
- Home Security Gateway
- Home Automation
- NAS Devices

MT7986A is fabricated with advanced silicon process and integrates a Quad-core ARM® Cortex-A53 MPCoreTM operating up to 2.0GHz and more DRAM bandwidth. This SoC also includes a variety of peripherals, including one USB3.0/USB2.0 (Host), one USB2.0 (Host), and one PCIE2.0 2lane (RC) ports. To support popular network applications, MT7986A also implements two 2.5Gbps HSGMII Ethernet interface. MT7986A combines with two RF chips, they can provide dual-band concurrent chipset solution for WIFI6E AX6000 wireless router platform. User also can create tri-band solution by connecting wireless NIC card thru its PCIe port.

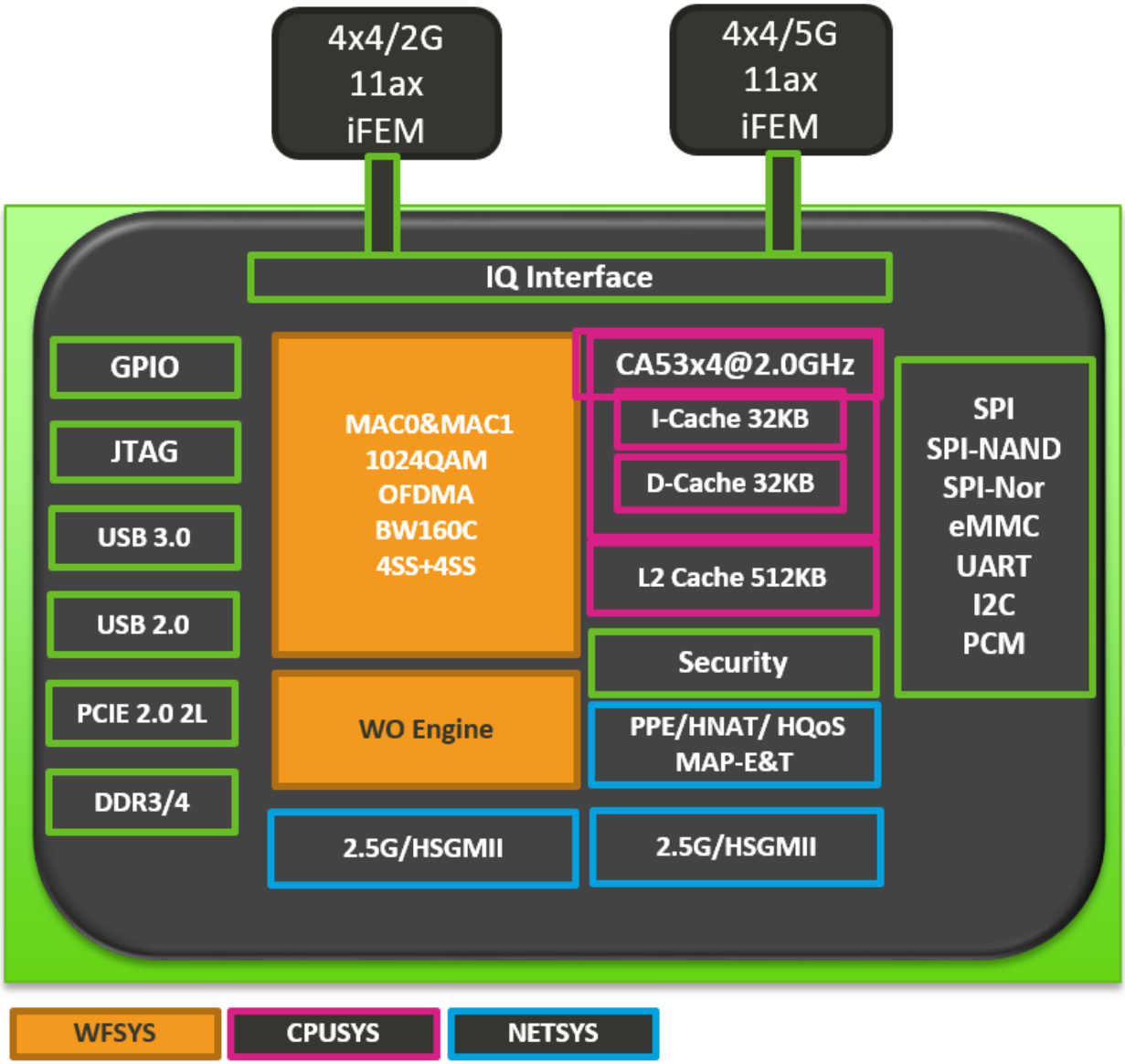
Besides the connectivity features, the hardware-based NAT engine with QoS embedded in MT7986A transporting the audio/video streams in higher priority than other non-timely services also enriches the home entertainment application. The SFQ separating P2P sessions from audio/video ones so that MT7986A guarantees the streaming service.

With the advanced technology and abundant features, MT7986A is well positioned to be the core of next-generation Smart WiFi AP router, and home gateway systems.

Key Features

- Embedded Quad-core ARM® Cortex-A53 MPCore operating at 2.0GHz
  - 32KB L1 I-Cache and 32KB L1 D-Cache
  - 512KB unified L2 Cache
  - NEON/FPU
- Discrete 16-bit DDR3/4 chip
- NOR (SPI), NAND Flash (SPI, SLC), eMMC5.1
- USB3.0/USB2.0 Host x1
- USB2.0 Host x1
- PCIE2.0 2-lane HOST x1
- Audio PCM interface x1
- SPI, I2C, UART Lite, JTAG, MDC, MDIO, GPIO, PWM
- Two HSGMII(2.5Gbps) interfaces
- WiFi
  - Lead in 4x4+4x4 WIFI6E integration
  - Airtime Fairness
  - Spectrum Analyzer
- HW NAT
  - Etherent/WiFi
  - Wired speed
  - IPv4 routing, NAT, NAPT
  - IPv6 routing, DS-Lite, 6RD
- HW QoS
  - 128 hardware queues to guarantee the min/max bandwidth of each flow.
  - Seamlessly co-work with HW NAT engine.
  - SFQ w/ 1k queues.
- Security
  - Secure boot
  - Crypto Suite
  - Anti Clone
- Green
  - Intelligent Clock Scaling (exclusive)
  - DDR: ODT off, Self-refresh mode

Functional Block Diagram



Document Revision History

Revision	Date	Author	Description
0.90	2021-9-03	Wen-Hsuan.Hu	Initial Release
0.94	2021-9-08	Wen-Hsuan.Hu	Update
0.95	2021-9-10	Wen-Hsuan.Hu	Update DDR pin name for DDR3 type
0.96	2021-9-14	Chihcheng Wang	Update Thermal parameters
0.97	2021-9-17	Wen-Hsuan.Hu	Update DDR3/4 support size
0.98	2021-10-21	Wen-Hsuan.Hu	Update recommend T-Ambient
1.0	2021-12-07	Wen-Hsuan.Hu	Update top side mark.
1.01	2021-12-07	Wen-Hsuan.Hu	Update ordering information MT7986A to MT7986AV.
1.1	2022-1-11	Wen-Hsuan.Hu	1. Add WRI timing. 2. Update pin description AA19/AE10 name for DDR3
1.11	2022-1-14	Wen-Hsuan.Hu	1. Update pin description about SPI0~2. 2. Update power on sequence parameter description for T4
1.12	2022-2-15	Chihlung.Tsou	1. Update pin default value
1.13	2022-3-8	Wen-Hsuan.Hu	1. Modify T6 timing in power on seqence. 2. Add I2C IO timing spec.

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1 General Features

1.1 Platform Features

- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A53 MPCoreTM operating at 2.0 GHz
  - NEON processing engine with Advanced SIMD and Floating-point Extension
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - Cryptography Extension
- **WIFI MCU subsystem**
  - Andes processor with I/D cache
- **Memory interface**
  - Supports discrete DDR3/4 chip
  - 16-bit data bus width
  - Memory speed up to DDR3-2133 and DDR4-3200
  - Supports self-refresh/partial self-refresh mode
  - Programmable slew rate for memory controller's IO pads
  - Advanced bandwidth arbitration control
- **External interface**
  - 1 USB3.0/USB2.0 (Host)
  - 1 USB2.0 (Host)
  - 1 PCIE2.0 2lane (Host)
  - UART for external devices and debugging interfaces
  - SPI master for external devices
  - SPI NOR flash interface
  - SPI NAND flash interface
  - eMMC v5.1 inferface
  - I2C to control peripheral devices
  - General Purpose Input/Output
  - PWM (Pulse Width Modulation)
  - Audio PCM interface
- **Operating conditions**
  - Logic voltage: 0.85V
  - CPU voltage: 1.023V
  - I/O voltage: 1.8V/3.3V
  - DDR DRAM Interface: 1.2/1.5V/1.8V
  - Clock source: 40MHz
- **Package**
  - MFC VFBGA 16.85x16.85mm 570 balls
  - Ball pitch: 0.65mm

1.2 Wireless Connectivity Features

1.2.1 Wi-Fi MAC

1.2.1.1 Features

Wi-Fi MAC supports the following features:

- Support Dual band Dual Concurrent
- Support all date rates of 802.11a/b/g/n/ac/ax
- Support short GI and all data rates of 802.11n including MCS0 to MCS7
- Support 802.11ac MCS0 to MCS9
- Support 802.11ax MCS0 to MCS11
- AMPDU/AMSDU RX (de-aggregation) and TX (aggregation) support
- TX beamformer and RX beamformee
- TX rate adaptation
- TX power control
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP hardware processing
  - GCMP hardware processing
- Management/control frame filtering

1.2.2 WLAN Baseband

1.2.2.1 Features

Wi-Fi baseband supports the following features:

- Support Dual band Dual Concurrent
- 20/40/80/160 MHz channels
- HE MCS0-11 BW20/40/80/160MHz with Nss=1~4
- Short Guard Interval
- Space-time block code (STBC)
- Low Density Parity check (LDPC)
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- Support radar detection
- Beamformer (explicit/implicit)
  - Eecoded BW20/40/80/160 up to 4x4 BF matrix apply
- Beamformee
  - Decoded BW20/40/80/160 up to 4x3 MU matrix feedback
- UL OFDMA / MU-MIMO
- DL OFDMA / MU-MIMO
- Max RU number in 2G band is 8
- Max RU number in 5/6G band is 16

1.3 Wired Ethernet Features

- **Frame Engine**
  - Packet DMA (PDMA)
    - 4 Tx descriptor and 4 Rx descriptor rings
    - Scattter/Gather DMA
    - Configurable 4/8/16/32 32-bit burst legnth and delayed interrupt
    - Support LRO and TSO
  - QoS DMA (QDMA)
    - Supports 128 Tx physical queues and 4 sets of scheduler
    - Per Tx queue forward/drop packet accounting
    - Per Tx queue forward byte accounting
    - Supports Tx queue min/max rate control and SP/WFQ egress scheduler
    - Supports up to 1024 virtual queues for 8 sets of SFQ
  - Packet Switch Engine (PSE)
    - Wire-speed NAT/NAPT routing
    - Egress rate limiting/shaping
    - IP/TCP/UDP checksum offload
    - IP/TCP/UDP checksum generaton
    - VLAN & PPPoE header insertion
    - TCP segmentation offload
  - Packet Process Engine (PPE)
    - IPv4 NAP/NAPT, IPv6 Routing and Tunnel IP (DS-Lite, 6RD, MAPE/T)
    - 1/2/4/8/16/32K session/flow
    - Flow offloading technology for flexible/high performance packet L3/L4 packet processing
    - Support NAT/NAPT wire-speed within 128 flows for any packet size

  Note that PPE features mentioned above require software porting to function.

- **WiFi WARP**
  - Ethernet/WiFi offlaod, forwarding packet directly
  - Dynamic buffer allocate and release

- **GigaMAC (GMAC)**
  - Support IEEE 802.3x full duplex flow control
  - Support HSGMII interface
    - HSGMII supports 10/100/1000Mbps speed change through auto negotiation and configurable 2.5Gbps SerDes link

1.4 Main Features Summary

The following table covers the main features offered by MT7986A.

Table 1-1 Main Features

Feature	Description
CPU	ARM CA53 (2.0GHz, Quad-core)
I-Cache, D-Cache	32kB, 32kB per core
L2 Cache	512KB
Security	Support 2* 256-bit Multi-key on OTP efuse Support 64 versions OTP efuse for Anti-roll back
DRAM data width	16bit
DRAM type	DDR3-2133:256MB/512MB (2Gb/4Gb support) DDR4-3200:512MB/1GB/2GB (4Gb/8Gb/16Gb support) DDR4-2666:512MB/1GB/2GB (4Gb/8Gb/16Gb support)
WIFI	4x4 11ax 2.4GHz + 4x4 11ax 5GHz Integrated PA, LNA and TR-SW 20/40/80/160MHz bandwidth Support up to 1024QAM Support external LNA and PA support (option)
Ethernet	HSGMII x2
HNAT/HQoS	HQoS 128 queues, SFQ 1K queues HNAT (IPv4, IPv6 routing, DS-Lite, 6RD)
USB	USB3.0/2.0 x1, USB2.0 x1
PCIE	PCIe2.0 2lane HOST
SPI NAND Flash	ECC (BCH code) acceleration capable of 24-bit error correction (w/. ECC engine)
SPI Flash (NOR)	Max 52MHz data bit width x1/x2/x4 Support 4-byte address mode compatible with 3-byte address mode
eMMC	eMMC v5.1 @104MHz 1.8V
I2C	I2C x 1 Max 400kHz Support 7/10-bit addressing
SPI	SPI x 1 Support DMA and FIFO mode
UART	UART-Lite(2-pins) x 1 UART(4-pins) x2
PCM	Audio output PCM interface x1
Package	16.85 x 16.85 mm, MFC VFBGA-570B

2 Pin

2.1 Pin Map (Top View)

Table 2-1 Pin Map (Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC		DVSS	WF0_DIG_RESETB	WF0_HB1		WF0_HB5		AFE0_WF1_QP	AFE0_WF1_IN	DVSS	AFE0_WF3_QP
B	NC	EMMC_DATA_5	EMMC_DATA_4	EMMC_DATA_3	WF0_TOP_CLK	WF0_HB3	WF0_HB0	WF0_HB7	DVSS	AFE0_WF1_QN	AFE0_WF1_IP	DVSS	AFE0_WF3_QN
C	EMMC_DATA_6	EMMC_DATA_2	EMMC_DATA_1	EMMC_DATA_0	DVSS	DVSS	DVSS	WF0_HB9	DVSS	DVSS	DVSS	DVSS	DVSS
D	DVDD18IO_RT_C0	EMMC_DATA_7	EMMC_CK	EMMC_CMD	DVSS	WF0_TOP_DATA	WF0_HB2	WF0_HB0_B	DVSS	DVSS	AFE0_WF0_QN	DVSS	DVSS
E	DVDD33IO_RT_C0	SPI1_CS	EMMC_DSL	EMMC_RSTB	DVSS	WF0_XO_REQ	WF0_HB4	WF0_HB6	WF0_HB8		AFE0_WF0_QP		DVSS
F		SPI1_MISO	SPI1_CLK	DVSS	DVDD18IO_WF0	WF0_CBA_RESETB	DVSS	DVSS	WF0_HB10		DVSS	AFE0_WF0_IN	AFE0_WF0_IP
G	DVSS	DVSS	SPI1_MOSI	PWM0	PWM1	TESTMODE	DVSS		DVSS	DVSS	DVSS	DVSS	DVSS
H	PCIE_LN0_RXN	PCIE_LN0_RXP	DVSS	SPI0_MISO	SPI0_CS	SPI0_CLK			DVSS		DVSS	DVSS	DVSS
J	PCIE_LN0_TXP	PCIE_LN0_TXN	DVSS	SPI0_MOSI	SPI0_WP	SPI0_HOLD		DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS
K	DVSS	DVSS	DVSS					DVDD_CORE	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS
L	PCIE_CKN	PCIE_CKP	DVSS	DVSS	DVDD18IO_RT_C2				DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS
M	PCIE_LN1_TXP	PCIE_LN1_TXN	DVSS	AVDD09_PCIE		DVSS			DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS
N	DVSS	DVSS	AVDD18_PCIE	AVDD09_PCIE					DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS
P	PCIE_LN1_RXN	PCIE_LN1_RXP	DVSS			DVSS	DVSS	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS
R	AUXIN0	AUXIN1	AUXIN2	PLLGP_TN	PLLGP_TP	MD			DVSS	DVSS	DVSS	DVSS	DVSS
T		REFP	AVSS18_AP	DVDD33IO_RB_C0	DVDD33IO_RB_C1	AVDD18_PLLGP	AVSS18_PLLGP		DVSS	DVSS	DVSS	DVSS	DVSS
U	AVDD18_AP	SYS_WATCHDOG	GPIO_1	GPIO_9	GPIO_0	GPIO_11			DVSS	DVDD_PROC_L	DVSS	DVSS	DVSS
V	GPIO_7	UART1_CTS	UART1_RTS						DVSS	DVDD_PROC_L	DVDD_PROC_L	AVDD18_EMI0	AVDDQ_EMI0
W		UART1_RXD	UART1_TXD		UART2_RXD	UART2_TXD			DVSS	DVDD_PROC_L	DVDD_PROC_L	DVSS	DVSS
Y	GPIO_10	GPIO_13	GPIO_6	UART2_CTS	UART2_RTS	PCIE_PERESET_N			DVSS	DVDD_PROC_L	DVDD_PROC_L	DVSS	DVSS
AA		GPIO_14	GPIO_8	DVSS				DVSS	EMI_RESET_N	DVSS	DVSS	DVSS	DVSS
AB	DVDD18IO_RB_C0	GPIO_12	UART0_TXD	DVSS	DVSS	DVSS	DVSS	EMI0_DQ14	DVSS	EMI0_DQS1_C	DVSS	DVSS	EMI0_DQ15
AC		UART0_RXD	SYSRSTB	DVSS	EMI0_DQ12	EMI0_DQ10	EMI0_DQ8	DVSS	DVSS	EMI0_DQS1_T	DVSS	DVSS	EMI0_DQ13
AD	DVDD18IO_RB_C1	PCM_CLK	PCM_DTX	DVSS	DVSS	DVSS	DVSS	DVSS	EMI0_DM1	DVSS	DVSS	EMI0_DQ9	DVSS
AE	NC	PCM_DRX	PCM_FS	EMI_EXTR	EMI0_DQ6	EMI0_DQ2	EMI0_DQ4	EMI0_DQS0_C	EMI0_DQS0_T	EMI0_DQ7	DVSS	EMI0_DQ11	EMI0_DQ1
AF	NC	NC	GPIO_15	DVSS		DVSS	EMI0_DQ0		DVSS	EMI0_DQ3	EMI0_DM0	DVSS	EMI0_DQ5

Table 2-2 Pin Map (Right Side)

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	AFE0_WF3_IN	DVSS	AFE0_XIN_WBG	WF1_TOP_CLK		WF1_HB3		WF1_HB7	AFE1_WF1_QN	DVSS	AFE1_WF1_IP	NC	NC
B	AFE0_WF3_IP	DVSS	AFE1_XIN_WBG	WF1_DIG_RESETB	DVSS	WF1_HB1	WF1_HB0	WF1_HB5	AFE1_WF1_QP	DVSS	AFE1_WF1_IN	AFE1_WF3_QN	NC
C	DVSS	DVSS	DVSS	WF1_XO_REQ	WF1_TOP_DATA	WF1_HB2	DVSS	DVSS	AFE1_WF0_QN	AFE1_WF0_QP	DVSS	AFE1_WF3_QP	
D	AFE0_WF2_QP	AFE0_AVDD18_WBG	AFE0_AVDD18_WBG	AFE1_AVDD18_WBG	WF1_CBA_RESETB	WF1_HB4	DVSS	DVSS	AFE1_WF0_IN	AFE1_WF0_IP	DVSS	AFE1_WF3_IN	AFE1_WF3_IP
E	AFE0_WF2_QN	AFE0_WF2_IN	DVSS	AFE1_AVDD18_WBG	AFE0_AVDD12_WBG	WF1_HB0_B	WF1_HB6			DVSS	AFE1_WF2_QN	AFE1_WF2_QP	DVSS
F	DVSS	AFE0_WF2_IP	DVSS	DVSS			WF1_HB8	DVSS		AFE1_WF2_IP	AFE1_WF2_IN	DVSS	DVSS
G			DVSS	DVSS			DVSS		DVSS	DVSS	DVSS	DVSS	AFE1_XIN_WBG
H			DVSS	DVSS	DVDD_CORE		DVSS			AFE1_AVDD12_WBG	DVSS		AVDD18_CKSQ
J	DVSS	DVSS	DVSS	DVSS	DVDD_CORE				DVSS	DVDD18IO_LT	DVDD18IO_WF1	AVDD12_CKSQ	
K	DVDD_CORE	DVSS	DVSS	DVSS	DVDD_CORE			WF2G_LED	WF5G_LED		SPI2_WP	SPI2_MISO	SPI2_CS
L	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE			GPIO_4	GPIO_5		SPI2_MOSI	SPI2_HOLD	
M	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS				GPIO_2	GPIO_3	SPI2_CLK	DVSS	DVDD33IO_LT
N	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS	DVSS	DVSS		SG1_AVDD09_SSUSB	SG1_AVDD18_SSUSB	DVSS	SG0_SSUSB_RXP	SG0_SSUSB_RXN
P	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS			DVSS		DVSS	SG0_SSUSB_TXN	SG0_SSUSB_TXP	
R	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS			DVSS	SG0_AVDD18_SSUSB	SG0_AVDD09_SSUSB	DVSS	DVSS	DVSS
T	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVSS	SG1_SSUSB_TXN	SG1_SSUSB_TXP
U	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVSS		U3_AVDD09_SSUSB	U3_AVDD18_SSUSB	U2_0_AVDD33_USB		DVSS	SG1_SSUSB_RXN	SG1_SSUSB_RXP
V	AVDDQ_EMI0	AVDDQ_EMI0_CA	AVDDQ_EMI0_CA	AVDDQ_EMI0	DVSS		U2_0_AVDD12_USB	U2_0_AVDD18_USB	U2_1_AVDD33_USB	DVSS	U3_SSUSB_RXP	U3_SSUSB_RXN	
W	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	U2_1_AVDD18_USB	U2_1_AVDD12_USB		U3_SSUSB_TXP	U3_SSUSB_TXN		
Y	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	
AA	DVSS	DVSS	DVSS	EMI_TP	EMI_TN	EMI0_A12	DVSS	EMI0_A5	DVSS	VQPS	DVSS	U2_0_USB_DM	U2_0_USB_DP
AB	DVSS	EMI0_CK_T	DVSS	EMI0_RAS_N	DVSS	DVSS	EMI0_BA1	EMI0_A1	DVSS	AVDD15_POR	DVSS	U2_1_USB_DM	U2_1_USB_DP
AC	DVSS	EMI0_CK_C	DVSS	EMI0_CAS_N	DVSS	DVSS	EMI0_A3	EMI0_A9	EMI0_WE_N	DVSS	AVDD18_POR	DVDD33IO_LB	
AD	DVSS	EMI0_CKE0	EMI0_CS0_N	EMI0_A10	EMI0_A0	EMI0_A11	EMI0_A6	DVSS	DVSS	BG_OUT	7531_INT	SMI_MDC	DVDD18IO_LB
AE	EMI0_A7	EMI0_A13	DVSS	DVSS	EMI0_A2	EMI0_A8	EMI0_BA0	DVSS	DVSS	I2C_SCL	RSTB	SMI_MDIO	NC
AF		EMI0_ODT	EMI0_ACT_N	EMI0_A4		DVSS		EMI0_BG0	DVSS	I2C_SDA		NC	NC

2.2 Pin Descriptions

Table 2-3 Pin Description

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
GPIO											
U5	GPIO_0	I	NP	I	0	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
U3	GPIO_1	I	NP	I	0	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
M22	GPIO_2	I	NP	I	0	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
M23	GPIO_3	I	NP	I	0	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
L21	GPIO_4	I	NP	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
L22	GPIO_5	I	PU	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
Y3	GPIO_6	OL	PU	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO / JTAG TDO
V1	GPIO_7	I	PU	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO / JTAG TDI
AA3	GPIO_8	I	PU	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO / JTAG TMS
U4	GPIO_9	I	PU	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO / JTAG TCK
Y1	GPIO_10	I	PU	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO / JTAG TRSTN
U6	GPIO_11	OL	PD	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
AB2	GPIO_12	I	PD	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
Y2	GPIO_13	I	PD	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
AA2	GPIO_14	I	PD	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
AF3	GPIO_15	I	PD	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	General Purpose IO
UART											
AC2	UART0_RXD	I	PU	I	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART RX data
AB3	UART0_TXD	I	PU	OH	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART TX data
V2	UART1_CTS	I	PU	I	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART CTS
V3	UART1_RTS	OH	PU	OH	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART RTS
W2	UART1_RXD	I	PU	I	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART RX data
W3	UART1_TXD	OH	PU	OH	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART TX data
Y4	UART2_CTS	I	PU	I	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART CTS
Y5	UART2_RTS	OH	PU	OH	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART RTS
W5	UART2_RXD	I	PU	I	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART RX data
W6	UART2_TXD	OH	PU	OH	1	PU	16	PU/PD	3.3	2/4/6/8/10/12/14/16	UART TX data
PWM											
G4	PWM0	I	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	PWM0
G5	PWM1	OL	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	PWM1
I2C											
AE23	I2C_SCL	I	NP	I	1	NP	16	PD	3.3	2/4/6/8/10/12/14/16	I2C serial clock
AF23	I2C_SDA	I	NP	I	1	NP	16	PD	3.3	2/4/6/8/10/12/14/16	I2C serial data
SPI											

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
H6	SPI0_CLK	OL	PD	OL	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Clock
H5	SPI0_CS	OL	NP	OH	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Chip Select
J6	SPI0_HOLD	OL	NP	OH	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash HOLD
H4	SPI0_MISO	OL	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Master Input, Slave Output
J4	SPI0_MOSI	OL	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Master Output, Slave Input
J5	SPI0_WP	OL	NP	OH	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Write Protect
F3	SPI1_CLK	OL	PD	OL	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Clock
E2	SPI1_CS	OH	NP	OH	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Chip Select
F2	SPI1_MISO	I	NP	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Master Input, Slave Output
G3	SPI1_MOSI	OL	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Master Output, Slave Input
M24	SPI2_CLK	OL	PD	OL	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Clock
K26	SPI2_CS	OH	NP	OH	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Chip Select
L25	SPI2_HOLD	I	NP	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash HOLD
K25	SPI2_MISO	I	NP	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Master Input, Slave Output
L24	SPI2_MOSI	OL	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Master Output, Slave Input
K24	SPI2_WP	I	NP	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial Flash Write Protect
EMMC											
D3	EMMC_CK	OL	PD	OL	1	PD	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Clock
D4	EMMC_CMD	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Command
C4	EMMC_DATA_0	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 0
C3	EMMC_DATA_1	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 1
C2	EMMC_DATA_2	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 2
B4	EMMC_DATA_3	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 3
B3	EMMC_DATA_4	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 4
B2	EMMC_DATA_5	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 5
C1	EMMC_DATA_6	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 6
D2	EMMC_DATA_7	I	PU	I	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Bit 7
E3	EMMC_DSL	I	PD	I	1	PD	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Data Strobe
E4	EMMC_RSTB	OH	PU	OH	1	PU	16	PU/PD	1.8	2/4/6/8/10/12/14/16	EMMC Reset
Audio PCM											
AD2	PCM_CLK	OL	PD	OL	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	PCM Clock
AE2	PCM_DRX	I	PD	I	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	PCM Data RX
AD3	PCM_DTX	OL	PD	OL	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	PCM Data TX

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
AE3	PCM_FS	OH	PD	OH	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	PCM FS
DDR Interface											
AE4	EMI_EXTR / EMI_EXTR	A	-	A	-	-	-	-	-	-	DRAM calibration resistor
AA9	EMI_RESET_N / EMI_RESET_N	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD18	EMI0_A0 / EMI0_A0	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB21	EMI0_A1 / EMI0_A1	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD17	EMI0_A10 / EMI0_WE_N	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD19	EMI0_A11 / EMI0_A9	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AA19	EMI0_A12 / EMI0_A12	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE15	EMI0_A13 / EMI0_A8	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE18	EMI0_A2 / EMI0_A2	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC20	EMI0_A3 / EMI0_BA0	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF17	EMI0_A4 / EMI0_BA2	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AA21	EMI0_A5 / EMI0_A4	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD20	EMI0_A6 / EMI0_A7	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE14	EMI0_A7 / EMI0_A6	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE19	EMI0_A8 / EMI0_A13	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC21	EMI0_A9 / EMI0_A11	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF16	EMI0_ACT_N / EMI0_A10	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE20	EMI0_BA0 / EMI0_A5	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB20	EMI0_BA1 / EMI0_BA1	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF21	EMI0_BG0 / EMI0_A3	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC17	EMI0_CAS_N / EMI0_CAS_N	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC15	EMI0_CK_C / EMI0_CK_C	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB15	EMI0_CK_T / EMI0_CK_T	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD15	EMI0_CKE0 / EMI0_CKE0	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD16	EMI0_CS0_N / EMI0_CS0_N	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF11	EMI0_DM0 / EMI0_DM0	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD9	EMI0_DM1 / EMI0_DM1	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF7	EMI0_DQ0 / EMI0_DQ0	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE13	EMI0_DQ1 / EMI0_DQ3	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC6	EMI0_DQ10 / EMI0_DQ9	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE12	EMI0_DQ11 / EMI0_DQ14	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC5	EMI0_DQ12 / EMI0_DQ11	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC13	EMI0_DQ13 / EMI0_DQ10	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB8	EMI0_DQ14 / EMI0_DQ15	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB13	EMI0_DQ15 / EMI0_DQ8	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE6	EMI0_DQ2 / EMI0_DQ6	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF10	EMI0_DQ3 / EMI0_DQ1	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE7	EMI0_DQ4 / EMI0_DQ2	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF13	EMI0_DQ5 / EMI0_DQ5	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
AE5	EMI0_DQ6 / EMI0_DQ4	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE10	EMI0_DQ7 / EMI0_DQ7	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC7	EMI0_DQ8 / EMI0_DQ13	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AD12	EMI0_DQ9 / EMI0_DQ12	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE8	EMI0_DQS0_C / EMI0_DQS0_C	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AE9	EMI0_DQS0_T / EMI0_DQS0_T	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB10	EMI0_DQS1_C / EMI0_DQS1_C	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC10	EMI0_DQS1_T / EMI0_DQS1_T	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AF15	EMI0_ODT / EMI0_A14	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AB17	EMI0_RAS_N / EMI0_RAS_N	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
AC22	EMI0_WE_N / EMI0_ODT	A	-	A	-	-	-	-	1.2/1.5	-	DDR4/DDR3 chip interface
USB / SSUSB											
V25	U3_SSUSB_RXN	A	-	A	-	-	-	-	0.9	-	SSUSB data pin RX -
V24	U3_SSUSB_RXP	A	-	A	-	-	-	-	0.9	-	SSUSB data pin RX +
W24	U3_SSUSB_TXN	A	-	A	-	-	-	-	0.9	-	SSUSB data pin TX -
W23	U3_SSUSB_TXP	A	-	A	-	-	-	-	0.9	-	SSUSB data pin TX +
AA25	U2_0_USB_DM	A	-	A	-	-	-	-	3.3	-	USB HS/FS/LS data pin Data -
AA26	U2_0_USB_DP	A	-	A	-	-	-	-	3.3	-	USB HS/FS/LS data pin Data +
AB25	U2_1_USB_DM	A	-	A	-	-	-	-	3.3	-	USB HS/FS/LS data pin Data -
AB26	U2_1_USB_DP	A	-	A	-	-	-	-	3.3	-	USB HS/FS/LS data pin Data +
PCIE											
H1	PCIE_LN0_RXN	A	-	A	-	-	-	-	0.9	-	PCIE_LN0 data pin RX -
H2	PCIE_LN0_RXP	A	-	A	-	-	-	-	0.9	-	PCIE_LN0 data pin RX +
J2	PCIE_LN0_TXN	A	-	A	-	-	-	-	0.9	-	PCIE_LN0 data pin TX -
J1	PCIE_LN0_TXP	A	-	A	-	-	-	-	0.9	-	PCIE_LN0 data pin TX +
P1	PCIE_LN1_RXN	A	-	A	-	-	-	-	0.9	-	PCIE_LN1 data pin RX -
P2	PCIE_LN1_RXP	A	-	A	-	-	-	-	0.9	-	PCIE_LN1 data pin RX +
M2	PCIE_LN1_TXN	A	-	A	-	-	-	-	0.9	-	PCIE_LN1 data pin TX -
M1	PCIE_LN1_TXP	A	-	A	-	-	-	-	0.9	-	PCIE_LN1 data pin TX +
L1	PCIE_CKN	A	-	A	-	-	-	-	0.9	-	PCIE CKN
L2	PCIE_CKP	A	-	A	-	-	-	-	0.9	-	PCIE CKP
Y6	PCIE_PERESET_N	I	PU	I	-	PU	-	PU	3.3	-	PCIE reset
MT7531 interface (SMI)											
AD24	7531_INT	I	PD	I	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	MT7531 Ethernet switch
AD25	SMI_MDC	OL	PU	OL	1	PD	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial management clock
AE25	SMI_MDIO	I	PU	I	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Serial management data
SGMII											
N26	SG0_SSUSB_RXN	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin RX -
N25	SG0_SSUSB_RXP	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin RX +
P24	SG0_SSUSB_TXN	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin TX -
P25	SG0_SSUSB_TXP	A	-	A	-	-	-	-	0.9	-	SGMII 0 data pin TX +

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
U25	SG1_SSUSB_RXN	A	-	A	-	-	-	-	0.9	-	SGMII 1 data pin RX -
U26	SG1_SSUSB_RXP	A	-	A	-	-	-	-	0.9	-	SGMII 1 data pin RX +
T25	SG1_SSUSB_TXN	A	-	A	-	-	-	-	0.9	-	SGMII 1 data pin TX -
T26	SG1_SSUSB_TXP	A	-	A	-	-	-	-	0.9	-	SGMII 1 data pin TX +
WiFi 2.4G RF Interface											
K21	WF2G_LED	OL	NP	OL	0	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	2G LED
F6	WF0_CBA_RESETB	OL	NP	OH	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	Reset RF chip analog
A5	WF0_DIG_RESETB	OH	NP	OH	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	Reset RF chip digital
E6	WF0_XO_REQ	OH	NP	OH	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	OSC clock request to RF chip
B5	WF0_TOP_CLK	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G SPI clock
D6	WF0_TOP_DATA	I	NP	I	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G SPI data
B7	WF0_HB0	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI clock
D8	WF0_HB0_B	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI clock
A6	WF0_HB1	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf0 data[0]
F9	WF0_HB10	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf0 data[1]
D7	WF0_HB2	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf1 data[0]
B6	WF0_HB3	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf1 data[1]
E7	WF0_HB4	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf2 data[0]
A8	WF0_HB5	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf2 data[1]
E8	WF0_HB6	I	NP	OL	I	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf3 data[0]
B8	WF0_HB7	I	NP	OL	I	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf3 data[1]
E9	WF0_HB8	I	NP	OL	I	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf4 data[0]
C8	WF0_HB9	I	NP	OL	I	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	2G WRI wf4 data[1]
A16	AFE0_XIN_WBG	A	-	A	-	-	-	-	1.8	-	2G OSC clock input from RF chip
F12	AFE0_WF0_IN	A	-	A	-	-	-	-	1.8	-	2G WF0 I_Channel differential N node
F13	AFE0_WF0_IP	A	-	A	-	-	-	-	1.8	-	2G WF0 I_Channel differential P node
D11	AFE0_WF0_QN	A	-	A	-	-	-	-	1.8	-	2G WF0 Q_Channel differential N node
E11	AFE0_WF0_QP	A	-	A	-	-	-	-	1.8	-	2G WF0 Q_Channel differential P node
A11	AFE0_WF1_IN	A	-	A	-	-	-	-	1.8	-	2G WF1 I_Channel differential N node
B11	AFE0_WF1_IP	A	-	A	-	-	-	-	1.8	-	2G WF1 I_Channel differential P node
B10	AFE0_WF1_QN	A	-	A	-	-	-	-	1.8	-	2G WF1 Q_Channel differential N node
A10	AFE0_WF1_QP	A	-	A	-	-	-	-	1.8	-	2G WF1 Q_Channel differential P node
E15	AFE0_WF2_IN	A	-	A	-	-	-	-	1.8	-	2G WF2 I_Channel differential N node
F15	AFE0_WF2_IP	A	-	A	-	-	-	-	1.8	-	2G WF2 I_Channel differential P node
E14	AFE0_WF2_QN	A	-	A	-	-	-	-	1.8	-	2G WF2 Q_Channel differential N node
D14	AFE0_WF2_QP	A	-	A	-	-	-	-	1.8	-	2G WF2 Q_Channel differential P node
A14	AFE0_WF3_IN	A	-	A	-	-	-	-	1.8	-	2G WF3 I_Channel differential N node
B14	AFE0_WF3_IP	A	-	A	-	-	-	-	1.8	-	2G WF3 I_Channel differential P node
B13	AFE0_WF3_QN	A	-	A	-	-	-	-	1.8	-	2G WF3 Q_Channel differential N node

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
A13	AFE0_WF3_QP	A	-	A	-	-	-	-	1.8	-	2G WF3 Q_Channel differential P node
WiFi 5G RF Interface											
K22	WF5G_LED	OL	NP	OL	1	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	5G LED
D18	WF1_CBA_RESETB	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	Reset RF chip analog
B17	WF1_DIG_RESETB	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	Reset RF chip digital
C17	WF1_XO_REQ	OH	NP	OH	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	OSC clock request to RF chip
A17	WF1_TOP_CLK	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G SPI clock
C18	WF1_TOP_DATA	I	NP	I	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G SPI data
B20	WF1_HB0	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI clock
E19	WF1_HB0_B	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI clock
B19	WF1_HB1	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI WF1 data[0]
C19	WF1_HB2	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI WF1 data[1]
A19	WF1_HB3	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI wf1 data[0]
D19	WF1_HB4	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI wf1 data[1]
B21	WF1_HB5	OL	NP	OL	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI wf2 data[0]
E20	WF1_HB6	I	NP	I	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI wf2 data[1]
A21	WF1_HB7	I	NP	I	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI wf3 data[0]
F20	WF1_HB8	I	NP	I	1	NP	16	PU/PD	1.8	2/4/6/8/10/12/14/16	5G WRI wf3 data[1]
B16	AFE1_XIN_WBG	-	-	-	-	-	-	-	-	-	NC in MT7986A
G26	AFE1_XIN_WBG	A	-	A	-	-	-	-	1.8	-	5G OSC clock input from RF chip
D22	AFE1_WF0_IN	A	-	A	-	-	-	-	1.8	-	5G WF0 I_Channel differential N node
D23	AFE1_WF0_IP	A	-	A	-	-	-	-	1.8	-	5G WF0 I_Channel differential P node
C22	AFE1_WF0_QN	A	-	A	-	-	-	-	1.8	-	5G WF0 Q_Channel differential N node
C23	AFE1_WF0_QP	A	-	A	-	-	-	-	1.8	-	5G WF0 Q_Channel differential P node
B24	AFE1_WF1_IN	A	-	A	-	-	-	-	1.8	-	5G WF1 I_Channel differential N node
A24	AFE1_WF1_IP	A	-	A	-	-	-	-	1.8	-	5G WF1 I_Channel differential P node
A22	AFE1_WF1_QN	A	-	A	-	-	-	-	1.8	-	5G WF1 Q_Channel differential N node
B22	AFE1_WF1_QP	A	-	A	-	-	-	-	1.8	-	5G WF1 Q_Channel differential P node
F24	AFE1_WF2_IN	A	-	A	-	-	-	-	1.8	-	5G WF2 I_Channel differential N node
F23	AFE1_WF2_IP	A	-	A	-	-	-	-	1.8	-	5G WF2 I_Channel differential P node
E24	AFE1_WF2_QN	A	-	A	-	-	-	-	1.8	-	5G WF2 Q_Channel differential N node
E25	AFE1_WF2_QP	A	-	A	-	-	-	-	1.8	-	5G WF2 Q_Channel differential P node
D25	AFE1_WF3_IN	A	-	A	-	-	-	-	1.8	-	5G WF3 I_Channel differential N node
D26	AFE1_WF3_IP	A	-	A	-	-	-	-	1.8	-	5G WF3 I_Channel differential P node
B25	AFE1_WF3_QN	A	-	A	-	-	-	-	1.8	-	5G WF3 Q_Channel differential N node
C25	AFE1_WF3_QP	A	-	A	-	-	-	-	1.8	-	5G WF3 Q_Channel differential P node
MISC											
G6	TESTMODE	I	PD	I	-	PD	-	PD	3.3	-	Test mode
AC3	SYSRSTB	I	PU	I	-	PU	-	PU	3.3	-	System reset

Pin	Name	Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
AE24	RSTB	A	-	A	-	-	-	-	-	-	Power ready to RF chip
U2	SYS_WATCHDOG	OH	NP	OH	-	NP	16	PU/PD	3.3	2/4/6/8/10/12/14/16	Watchdog reset
R4	PLLGP_TN	A	-	A	-	-	-	-	-	-	Used in test function (PLLGP)
R5	PLLGP_TP	A	-	A	-	-	-	-	-	-	Used in test function (PLLGP)
AD23	BG_OUT	A	-	A	-	-	-	-	-	-	Used in test function (POR)
T2	REFP	A	-	A	-	-	-	-	-	-	Used in test function (TSAUX)
R6	MD	A	-	A	-	-	-	-	-	-	Used in test function (TSAUX)
R1	AUXIN0	A	-	A	-	-	-	-	-	-	Used in test function (TSAUX)
R2	AUXIN1	A	-	A	-	-	-	-	-	-	Used in test function (TSAUX)
R3	AUXIN2	A	-	A	-	-	-	-	-	-	Used in test function (TSAUX)
AA18	EMI_TN	A	-	A	-	-	-	-	-	-	Used in test function (DDRPHY)
AA17	EMI_TP	A	-	A	-	-	-	-	-	-	Used in test function (DDRPHY)
Power											
AD26	DVDD18IO_LB	P	-	P	-	-	-	-	1.8	-	IO power supply
J23	DVDD18IO_LT	P	-	P	-	-	-	-	1.8	-	IO power supply
AB1	DVDD18IO_RB_C0	P	-	P	-	-	-	-	1.8	-	IO power supply
AD1	DVDD18IO_RB_C1	P	-	P	-	-	-	-	1.8	-	IO power supply
D1	DVDD18IO_RT_C0	P	-	P	-	-	-	-	1.8	-	IO power supply
L5	DVDD18IO_RT_C2	P	-	P	-	-	-	-	1.8	-	IO power supply
F5	DVDD18IO_WF0	P	-	P	-	-	-	-	1.8	-	IO power supply
J24	DVDD18IO_WF1	P	-	P	-	-	-	-	1.8	-	IO power supply
AC25	DVDD33IO_LB	P	-	P	-	-	-	-	3.3	-	IO power supply
M26	DVDD33IO_LT	P	-	P	-	-	-	-	3.3	-	IO power supply
T4	DVDD33IO_RB_C0	P	-	P	-	-	-	-	3.3	-	IO power supply
T5	DVDD33IO_RB_C1	P	-	P	-	-	-	-	3.3	-	IO power supply
E1	DVDD33IO_RT_C0	P	-	P	-	-	-	-	3.3	-	IO power supply
E18	AFE0_AVDD12_WBG	P	-	P	-	-	-	-	1.2	-	AFE0 power supply
D15	AFE0_AVDD18_WBG	P	-	P	-	-	-	-	1.8	-	AFE0 power supply
D16	AFE0_AVDD18_WBG	P	-	P	-	-	-	-	1.8	-	AFE0 power supply
H23	AFE1_AVDD12_WBG	P	-	P	-	-	-	-	1.2	-	AFE1 power supply
D17	AFE1_AVDD18_WBG	P	-	P	-	-	-	-	1.8	-	AFE1 power supply
E17	AFE1_AVDD18_WBG	P	-	P	-	-	-	-	1.8	-	AFE1 power supply
J25	AVDD12_CKSQ	P	-	P	-	-	-	-	1.2	-	CKSQ power supply
H26	AVDD18_CKSQ	P	-	P	-	-	-	-	1.8	-	CKSQ power supply
AB23	AVDD15_POR	P	-	P	-	-	-	-	1.5/1.2	-	POR power detect, connect to latest stable power DDR VDDQ.
AC24	AVDD18_POR	P	-	P	-	-	-	-	1.8	-	POR power supply
U1	AVDD18_AP	P	-	P	-	-	-	-	1.8	-	TXAUX power supply
T6	AVDD18_PLLGP	P	-	P	-	-	-	-	1.8	-	PLLGP power supply
V12	AVDD18_EMI0	P	-	P	-	-	-	-	1.8	-	DDR power supply
V13	AVDDQ_EMI0	P	-	P	-	-	-	-	1.5/1.2	-	DDR power supply
V14	AVDDQ_EMI0	P	-	P	-	-	-	-	1.5/1.2	-	DDR power supply

Pin	Name		Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
			State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
V17	AVDDQ_EMI0		P	-	P	-	-	-	-	1.5/1.2	-	DDR power supply
V15	AVDDQ_EMI0_CA		P	-	P	-	-	-	-	1.5/1.2	-	DDR power supply
V16	AVDDQ_EMI0_CA		P	-	P	-	-	-	-	1.5/1.2	-	DDR power supply
R23	SG0_AVDD09_SSUSB		P	-	P	-	-	-	-	0.9	-	SGMII0 power supply
R22	SG0_AVDD18_SSUSB		P	-	P	-	-	-	-	1.8	-	SGMII0 power supply
N22	SG1_AVDD09_SSUSB		P	-	P	-	-	-	-	0.9	-	SGMII1 power supply
N23	SG1_AVDD18_SSUSB		P	-	P	-	-	-	-	1.8	-	SGMII1 power supply
V20	U2_0_AVDD12_USB		P	-	P	-	-	-	-	1.2	-	USB power supply
V21	U2_0_AVDD18_USB		P	-	P	-	-	-	-	1.8	-	USB power supply
U22	U2_0_AVDD33_USB		P	-	P	-	-	-	-	3.3	-	USB power supply
W21	U2_1_AVDD12_USB		P	-	P	-	-	-	-	1.2	-	USB power supply
W20	U2_1_AVDD18_USB		P	-	P	-	-	-	-	1.8	-	USB power supply
V22	U2_1_AVDD33_USB		P	-	P	-	-	-	-	3.3	-	USB power supply
U20	U3_AVDD09_SSUSB		P	-	P	-	-	-	-	0.9	-	SSUSB power supply
U21	U3_AVDD18_SSUSB		P	-	P	-	-	-	-	1.8	-	SSUSB power supply
M4	AVDD09_PCIE		P	-	P	-	-	-	-	0.9	-	PCIE power supply
N4	AVDD09_PCIE		P	-	P	-	-	-	-	0.9	-	PCIE power supply
N3	AVDD18_PCIE		P	-	P	-	-	-	-	1.8	-	PCIE power supply
AA23	VQPS		P	-	P	-	-	-	-	1.8	-	EFUSE power supply
Power												
K8,J9,J10,K10,L10,M10,N10,P10,K11,L11,M11,N11,P11,K14,L14,M14,N14,P14,R14,T14,U14,L15,M15,N15,P15,R15,T15,U15,H18,J18,K18,L18		DVDD_CORE	P	-	P	-	-	-	-	0.85	-	Core power
U10,V10,W10,Y10,V11,W11,Y11		DVDD_PROC_L	P	-	P	-	-	-	-	1.023	-	CPU power
Ground												
G1,K1,N1,G2,K2,N2,H3,J3,K3,L3,M3,P3,A4,F4,L4,AA4,AB4,AC4,AD4,AF4,C5,D5,E5,AB5,AD5,C6,M6,P6,AB6,AD6,AF6,C7,F7,G7,P7,AB7,AD7,F8,J8,P8,AA8,AC8,AD8,B9,C9,D9,G9,H9,K9,L9,M9,N9,P9,R9,T9,U9,V9,W9,Y9,AB9,AC9,AF9,C10,D10,G10,R10,T10,AA10,AD10,C11,F11,G11,H11,J11,R11,T11,U11,AA11,AB11,AC11,AD11,AE11,A12,B12,C12,D12,G12,H12,J12,K12,L12,M12,N12,P12,R12,T12,U12,W12,Y12,AA12,AB12,AC12,AF12,C13,D13,E13,G13,H13,J13,K13,L13,M13,N13,P13,R13,T13,U13,W13,Y13,AA13,AD13,C14,F14,J14,W1		DVSS	G	-	G	-	-	-	-	-	-	

Pin	Name		Reset *1		After Reset *1				Pull *3, *4	Voltage (V)	Driving (mA)	Description
			State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
4,Y14,AA14,AB14,AC14,AD14,A15,B15,C15,J15,K15,W15,Y15,AA15,C16,E16,F16,G16,H16,J16,K16,L16,M16,N16,P16,R16,T16,U16,W16,Y16,AA16,AB16,AC16,AE16,F17,G17,H17,J17,K17,L17,M17,N17,P17,R17,T17,U17,W17,Y17,AE17,B18,M18,N18,P18,R18,T18,U18,V18,W18,Y18,AB18,AC18,N19,T19,W19,Y19,AB19,AC19,AF19,C20,D20,G20,H20,N20,T20,Y20,AA20,C21,D21,F21,P21,R21,T21,Y21,AD21,AE21,G22,J22,T22,Y22,AA22,AB22,AD22,AE22,AF22,A23,B23,E23,G23,P23,V23,Y23,AC23,C24,D24,G24,H24,N24,R24,T24,U24,Y24,AA24,AB24,F25,G25,M25,R25,Y25,E26,F26,R26											
T7		AVSS18_PLLGP	G	-	G	-	-	-	-	-	-	
T3		AVSS18_AP	G	-	G	-	-	-	-	-	-	
NC												
A1,B1,AE1,AF1,A2,AF2,A25,AF25,A26,B26,AE26,AF26		NC	NC	-	NC	-	-	-	-	-	-	

NOTE:

1. I: Input
   OH: Output high
   OL: Output low
   A: Analog
   P: Power
   G: Ground
   NC: No connection
2. The internal pull resistance value is 10 kΩ.
3. PD: Internal pull-down
   PU: Internal pull-up
   NP: No pull-down/up
4. The IO always has internal 5Kohm +-20% pull-down. While IO is set as GPIO mode, the IO driving strength can be one of 2/4/6/8/10/12/14/16 mA and default is 16 mA.

2.2.1 Constant Tie Pins

Table 2-4 Constant tied pins

Pin name	Description
TESTMODE	Test mode (tie to GND)

2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. User can configure register to specify the pin function.

2.3.1 Pin share scheme

Table 2-5 Pin Share

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4
SYS_WATCHDOG	GPIO0	SYS_WATCHDOG			
WF2G_LED	GPIO1	WF2G_LED			
WF5G_LED	GPIO2	WF5G_LED			
I2C_SCL	GPIO3	I2C_SCL	SGMII1_PHY_I2C_SCL	U3_PHY_I2C_SCL	
I2C_SDA	GPIO4	I2C_SDA	SGMII1_PHY_I2C_SDA	U3_PHY_I2C_SDA	
GPIO_0	GPIO5	PCIE_PHY_I2C_SCL	SGMII0_PHY_I2C_SCL		
GPIO_1	GPIO6	PCIE_PHY_I2C_SDA	SGMII0_PHY_I2C_SDA		
GPIO_2	GPIO7	DRV_VBUS	CONN0_UART_TXD0	UART1_RXD	
GPIO_3	GPIO8	DRV_VBUS_1P	CONN0_UART_TXD1	UART1_TXD	
GPIO_4	GPIO9	PCIE_CLK_REQ		UART1_CTS	
GPIO_5	GPIO10	PCIE_WAKE_N		UART1_RTS	
GPIO_6	GPIO11	JTAG_JTDO	WM0_JTAG_JTDO	SPIC_CLK	
GPIO_7	GPIO12	JTAG_JTDI	WM0_JTAG_JTDI	SPIC_MOSI	
GPIO_8	GPIO13	JTAG_JTMS	WM0_JTAG_JTMS	SPIC_MISO	
GPIO_9	GPIO14	JTAG_JTCLK	WM0_JTAG_JTCLK	SPIC_CS	
GPIO_10	GPIO15	JTAG_JTRST_N	WM0_JTAG_JTRST_N		
GPIO_11	GPIO16	WO0_JTAG_JTDO	CONN_ICE0_0	WO1_JTAG_JTDO	
GPIO_12	GPIO17	WO0_JTAG_JTDI	CONN_ICE0_1	WO1_JTAG_JTDI	
GPIO_13	GPIO18	WO0_JTAG_JTMS	CONN_ICE1_0	WO1_JTAG_JTMS	
GPIO_14	GPIO19	WO0_JTAG_JTCLK	CONN_ICE1_1	WO1_JTAG_JTCLK	
GPIO_15	GPIO20	WO0_JTAG_JTRST_N	PWM1	WO1_JTAG_JTRST_N	
PWM0	GPIO21	PWM0			
PWM1	GPIO22	PWM1	EMMC_RSTB	NET_WO0_UART_TXD	NET_WO1_UART_TXD
SPI0_CLK	GPIO23	SNFI_CLK	EMMC_DATA_0	SPIC_CLK	UART1_RXD
SPI0_MOSI	GPIO24	SNFI_MOSI	EMMC_DATA_1	SPIC_MOSI	UART1_TXD
SPI0_MISO	GPIO25	SNFI_MISO	EMMC_DATA_2	SPIC_MISO	UART1_CTS
SPI0_CS	GPIO26	SNFI_CS	EMMC_DATA_3	SPIC_CS	UART1_RTS
SPI0_HOLD	GPIO27	SNFI_HOLD	EMMC_DATA_4		
SPI0_WP	GPIO28	SNFI_WP	EMMC_DATA_5		
SPI1_CLK	GPIO29	SPIC_CLK	EMMC_DATA_6	UART1_RXD	UART2_RXD
SPI1_MOSI	GPIO30	SPIC_MOSI	EMMC_DATA_7	UART1_TXD	UART2_TXD
SPI1_MISO	GPIO31	SPIC_MISO	EMMC_CMD	UART1_CTS	UART2_CTS
SPI1_CS	GPIO32	SPIC_CS	EMMC_CK	UART1_RTS	UART2_RTS
SPI2_CLK	GPIO33	SPI0_CLK		UART2_RXD	SPIC_CLK
SPI2_MOSI	GPIO34	SPI0_MOSI		UART2_TXD	SPIC_MOSI
SPI2_MISO	GPIO35	SPI0_MISO	UART1_RXD	UART2_CTS	SPIC_MISO
SPI2_CS	GPIO36	SPI0_CS	UART1_TXD	UART2_RTS	SPIC_CS

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4
SPI2_HOLD	GPIO37	SPI0_HOLD	UART1_CTS		
SPI2_WP	GPIO38	SPI0_WP	UART1_RTS		
UART0_RXD	GPIO39	UART0_RXD			
UART0_TXD	GPIO40	UART0_TXD			
PCIE_PERESET_N	GPIO41	PCIE_PERESET_N			
UART1_RXD	GPIO42	UART1_RXD	UART_PTA_RXD		
UART1_TXD	GPIO43	UART1_TXD	UART_PTA_TXD		
UART1_CTS	GPIO44	UART1_CTS	EXT_IF0_0		
UART1_RTS	GPIO45	UART1_RTS	EXT_IF0_1		
UART2_RXD	GPIO46	UART2_RXD	EXT_IF0_2		
UART2_TXD	GPIO47	UART2_TXD	EXT_IF1_0		
UART2_CTS	GPIO48	UART2_CTS	EXT_IF1_1		
UART2_RTS	GPIO49	UART2_RTS	EXT_IF1_2		
EMMC_DATA_0	GPIO50	EMMC_DATA_0			
EMMC_DATA_1	GPIO51	EMMC_DATA_1			
EMMC_DATA_2	GPIO52	EMMC_DATA_2			
EMMC_DATA_3	GPIO53	EMMC_DATA_3			
EMMC_DATA_4	GPIO54	EMMC_DATA_4			
EMMC_DATA_5	GPIO55	EMMC_DATA_5			
EMMC_DATA_6	GPIO56	EMMC_DATA_6			
EMMC_DATA_7	GPIO57	EMMC_DATA_7			
EMMC_CMD	GPIO58	EMMC_CMD			
EMMC_CK	GPIO59	EMMC_CK			
EMMC_DSL	GPIO60	EMMC_DSL			
EMMC_RSTB	GPIO61	EMMC_RSTB			
PCM_DTX	GPIO62	PCM_DTX			
PCM_DRX	GPIO63	PCM_DRX			
PCM_CLK	GPIO64	PCM_CLK			
PCM_FS	GPIO65	PCM_FS			
MT7531_INT	GPIO66	MT7531_INT			
SMI_MDC	GPIO67	SMI_MDC			
SMI_MDIO	GPIO68	SMI_MDIO			
WF0_DIG_RESETB	GPIO69	WF0_DIG_RESETB			
WF0_CBA_RESETB	GPIO70	WF0_CBA_RESETB			
WF0_XO_REQ	GPIO71	WF0_XO_REQ			
WF0_TOP_CLK	GPIO72	WF0_TOP_CLK			
WF0_TOP_DATA	GPIO73	WF0_TOP_DATA			
WF0_HB1	GPIO74	WF0_HB1	WF0_HB1	WF0_MODE_SEL_1	
WF0_HB2	GPIO75	WF0_HB2	WF0_HB2	WF0_MODE_SEL_2	
WF0_HB3	GPIO76	WF0_HB3	WF0_HB3	WF0_XTAL_SEL_0	
WF0_HB4	GPIO77	WF0_HB4	WF0_HB4	WF0_XTAL_SEL_1	
WF0_HB0	GPIO78	WF0_O_HB0	WF0_O_HB0	WF0_MODE_SEL_0	
WF0_HB0_B	GPIO79	WF0_HB0_B	WF1_O_HB0		

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4
WF0_HB5	GPIO80	WF0_HB5	WF1_HB1	WF0_XTAL_SEL_2	
WF0_HB6	GPIO81	WF0_HB6	WF1_HB2		
WF0_HB7	GPIO82	WF0_HB7	WF1_HB3		
WF0_HB8	GPIO83	WF0_HB8	WF1_HB4		
WF0_HB9	GPIO84	WF0_HB9	WF1_HB5		
WF0_HB10	GPIO85	WF0_HB10	WF1_HB6		
WF1_DIG_RESETB	GPIO86	WF1_DIG_RESETB			
WF1_CBA_RESETB	GPIO87	WF1_CBA_RESETB			
WF1_XO_REQ	GPIO88	WF1_XO_REQ			
WF1_TOP_CLK	GPIO89	WF1_TOP_CLK			
WF1_TOP_DATA	GPIO90	WF1_TOP_DATA			
WF1_HB1	GPIO91	WF1_HB1	WF1_MODE_SEL_1		
WF1_HB2	GPIO92	WF1_HB2	WF1_MODE_SEL_2		
WF1_HB3	GPIO93	WF1_HB3	WF1_XTAL_SEL_0		
WF1_HB4	GPIO94	WF1_HB4	WF1_XTAL_SEL_1		
WF1_HB0	GPIO95	WF1_O_HB0	WF1_MODE_SEL_0		
WF1_HB0_B	GPIO96	WF1_HB0_B			
WF1_HB5	GPIO97	WF1_HB5	WF1_XTAL_SEL_2		
WF1_HB6	GPIO98	WF1_HB6			
WF1_HB7	GPIO99	WF1_HB7			
WF1_HB8	GPIO100	WF1_HB8			

2.4 Strapping Options

Table 2-6 Strapping

Pin Name	Strapping Name	Description
{GPIO_1, GPIO_0}	Boot Mode	00 : SPI-NOR 01 : SPI-NAND 10 : EMMC 11 : SNAND(SNFI)
GPIO_3	A-Die Mode	0: Two A-Die
UART0_TXD	Second A-Die XTAL mode select	0 : XTAL mode 1 : Buffer mode
PWM0	A-Die Crystal	1 : 40MHz XTAL
SYS_WATCHDOG	CPU voltage select	1 : 1.023V

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD_CORE	0.85V supply voltage	-0.3	0.935	V
DVDD_PROC_L	1.023V CPU supply voltage	-0.3	1.125	V
SG0_AVDD09_SSUSB SG1_AVDD09_SSUSB U3_AVDD09_SSUSB AVDD09_PCIE	0.9V supply voltage	-0.3	0.990	V
AFE0_AVDD12_WBG AFE1_AVDD12_WBG AVDD12_CKSQ U2_0_AVDD12_USB U2_1_AVDD12_USB	1.2V supply voltage	-0.3	1.320	V
AVDDQ_EMI0 AVDDQ_EMI0_CA	1.5V/1.2V supply voltage	-0.3 -0.3	1.575 1.320	V
DVDD18IO_LB DVDD18IO_LT DVDD18IO_RB_C0 DVDD18IO_RB_C1 DVDD18IO_RT_C0 DVDD18IO_RT_C2 DVDD18IO_WF0 DVDD18IO_WF1 AFE0_AVDD18_WBG AFE1_AVDD18_WBG AVDD18_CKSQ AVDD18_POR AVDD18_AP AVDD18_PLLGP AVDD18_EMI0 SG0_AVDD18_SSUSB SG1_AVDD18_SSUSB U2_0_AVDD18_USB U2_1_AVDD18_USB U3_AVDD18_SSUSB AVDD18_PCIE VQPS	1.8V supply voltage	-0.3	1.980	V
DVDD33IO_LB DVDD33IO_LT DVDD33IO_RB_C0 DVDD33IO_RB_C1 DVDD33IO_RT_C0 U2_0_AVDD33_USB U2_1_AVDD33_USB	3.3V supply voltage	-0.3	3.630	V

3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol or Pin name	Description	Min.	Typ.	Max.	Unit
DVDD_CORE	0.85V supply voltage	0.808	0.85	0.935	V
DVDD_PROC_L	1.023V CPU supply voltage	0.972	1.023	1.125	V
SG0_AVDD09_SSUSB SG1_AVDD09_SSUSB U3_AVDD09_SSUSB AVDD09_PCIE	0.9V supply voltage	0.855	0.9	0.945	V
AFE0_AVDD12_WBG AFE1_AVDD12_WBG AVDD12_CKSQ U2_0_AVDD12_USB U2_1_AVDD12_USB	1.2V supply voltage	1.140	1.2	1.260	V
AVDDQ_EMI0 AVDDQ_EMI0_CA	1.5V/1.2V supply voltage	1.425 1.140	1.5 1.2	1.575 1.260	V
DVDD18IO_LB DVDD18IO_LT DVDD18IO_RB_C0 DVDD18IO_RB_C1 DVDD18IO_RT_C0 DVDD18IO_RT_C2 DVDD18IO_WF0 DVDD18IO_WF1 AFE0_AVDD18_WBG AFE1_AVDD18_WBG AVDD18_CKSQ AVDD18_POR AVDD18_AP AVDD18_PLLGP AVDD18_EMI0 SG0_AVDD18_SSUSB SG1_AVDD18_SSUSB U2_0_AVDD18_USB U2_1_AVDD18_USB U3_AVDD18_SSUSB AVDD18_PCIE VQPS	1.8V supply voltage	1.710	1.8	1.890	V
DVDD33IO_LB DVDD33IO_LT DVDD33IO_RB_C0 DVDD33IO_RB_C1 DVDD33IO_RT_C0 U2_0_AVDD33_USB U2_1_AVDD33_USB	3.3V supply voltage	2.970	3.3	3.630	V
$T_{AMBIENT}$	Ambient temperature	-10	-	70	°C

3.3 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

Table 3-3 Thermal Characteristics

Symbol	Description	Performance	
		Typ	Unit
TJ	Maximum Junction Temperature (Plastic Package)	125	°C
θJA	Junction to ambient temperature thermal resistance[1] for JEDEC 4L PCB	10.6	°C/W
θJC	Junction to case temperature thermal resistance	3.4	°C/W
θJB	Junction to case temperature thermal resistance	4.57	°C/W
ψJt	Junction to the package thermal resistance for JEDEC 4L PCB	0.45	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5 x 114.5 mm (4”x4.5”)

3.4 Current Consumption

Please reference to Application note.

3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 5 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.6 AC Electrical Characteristics

3.6.1 UART Interface

MT7986A utilizes the Universal Asynchronous Receiver Transmitter (UART) interface as its host control interface. The electrical timing characteristic for the UART interface is illustrated below.

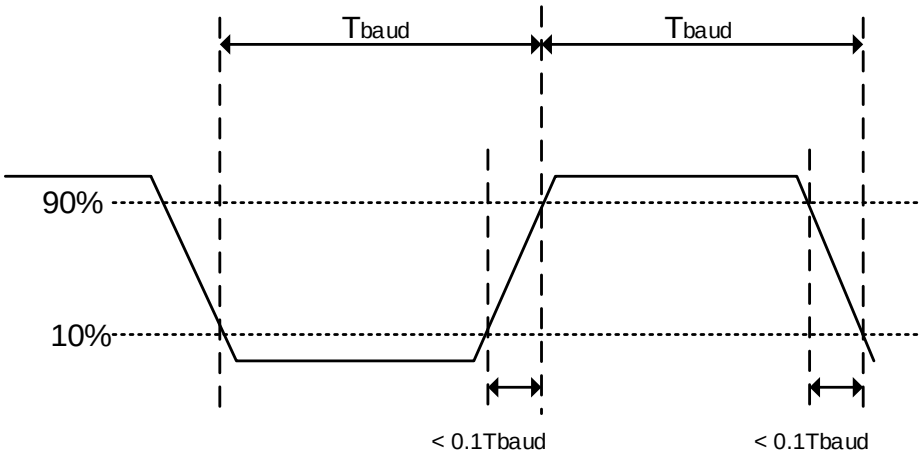


Figure 3-1 UART Timing

3.6.2 SPI Interface

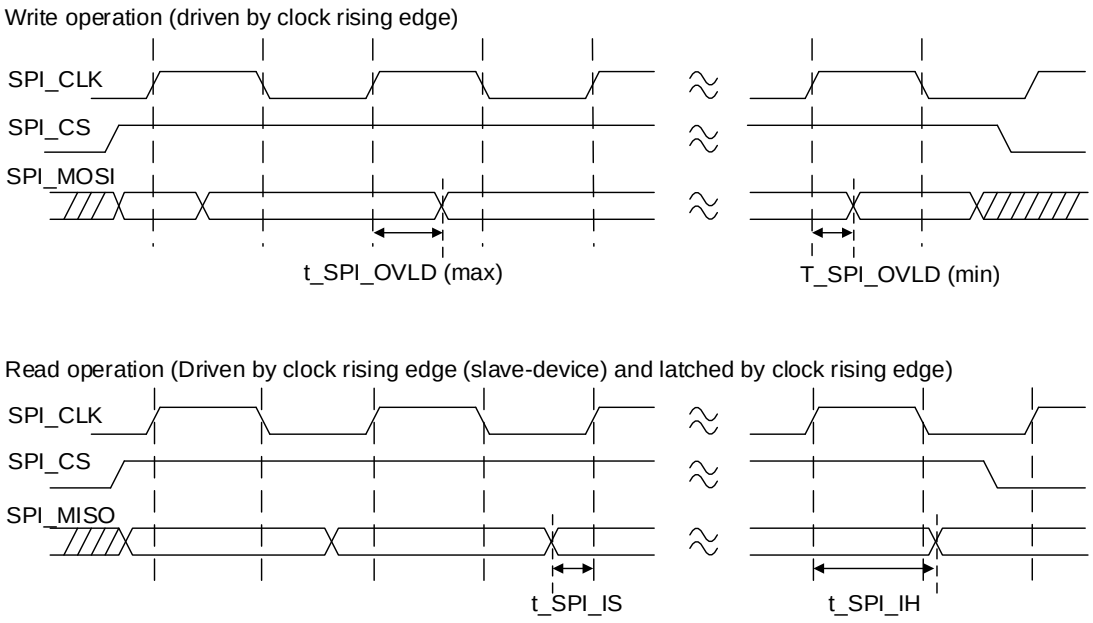


Figure 3-2 SPI Timing

Table 3-4 SPI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_SPI_IS	Setup time for SPI input	6.0	-	ns	
t_SPI_IH	Hold time for SPI input	-1.0	-	ns	
t_SPI_OVLD	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5 pF

3.6.3 SPI NOR Flash Interface

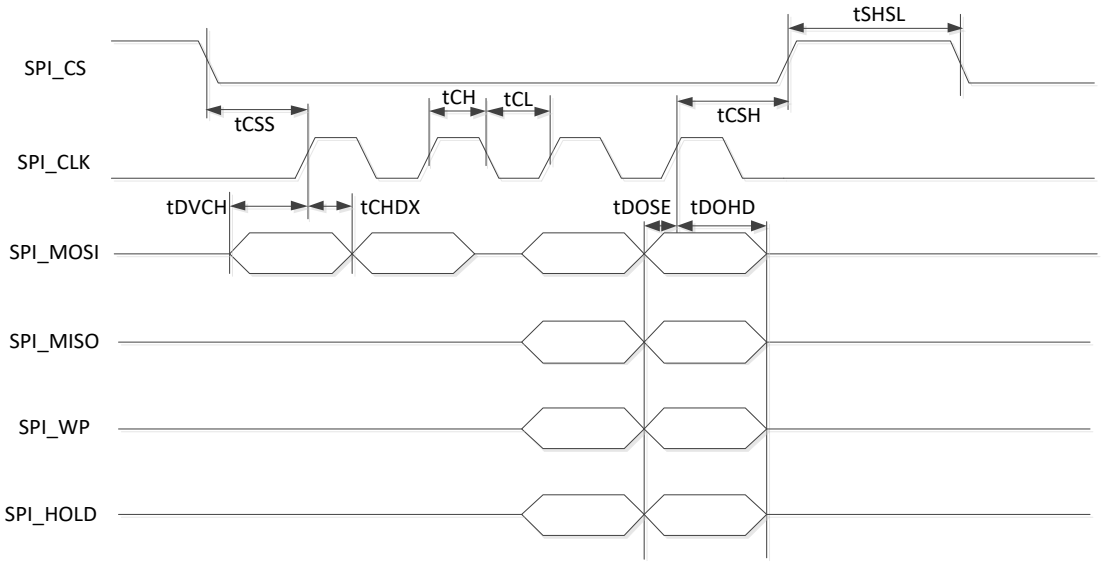


Figure 3-3 SPI NOR interface timing

Table 3-5 SPI NOR Interface Diagram Key

Symbol	Description	Min	Max	Unit
fC	Clock frequency	-	52	MHz
tCH	Clock High Time (relative to CK)	6.1	6.8	ns
tCL	Clock Low Time (relative to CK)	6.3	6.9	ns
tSHSL	CS deselect time	88	-	ns
tCSS	CS active Setup time	42	-	ns
tCSH	CS active Hold time	67	-	ns
tDVCH	DI setup time	5.7	-	ns
tCHDX	DI hold time	6.3	-	ns
tDOSE	DO setup time	0	-	ns
tDOHD	DO hold time	3	-	ns

3.6.4 SPI NAND Flash Interface

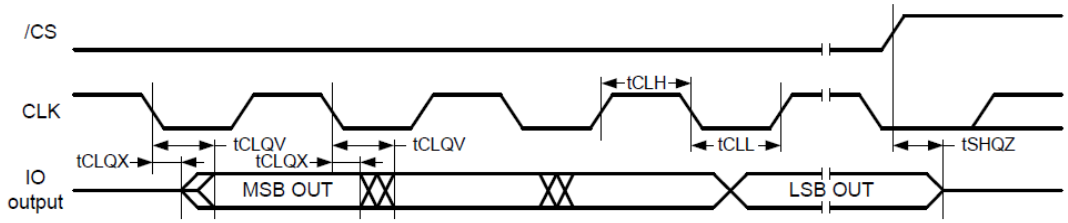


Figure 3-4 SPI NAND Serial Output Timing

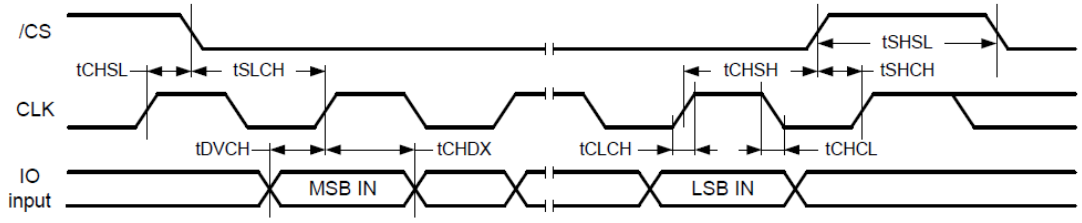


Figure 3-5 SPI NAND Serial Input Timing

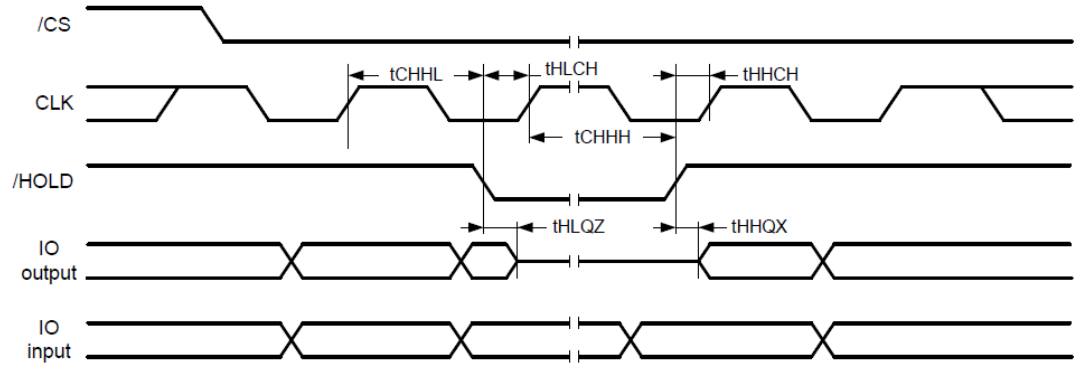


Figure 3-6 SPI NAND /HOLD Timing

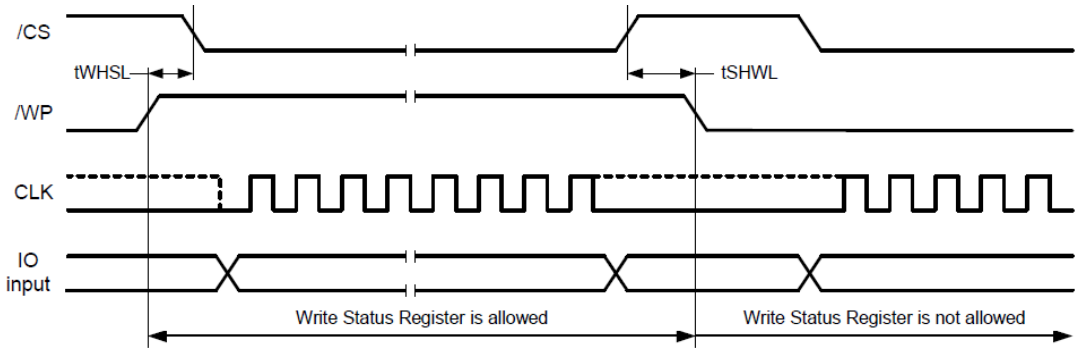


Figure 3-7 SPI NAND /WP Timing

Table 3-6 SPI NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit
tCLH, tCLL,	Clock High, Low Time for all instructions	4	-	ns
tCLCH	Clock Rise Time peak to peak	0.1		V/ns
tCHCL	Clock Fall Time peak to peak	0.1		V/ns
tSLCH	/CS Active Setup Time relative to CLK	5		ns
tCLCH	/CS Not Active Hold Time relative to CLK	5		ns
tDVCH	Data in Setup Time	2		ns
tCHDX	Data in Hold Time	3		ns
tCHSH	/CS Active Hold Time relative to CLK	3		ns
tSHCH	/CS Not Active Setup Time relative to CLK	3		ns
tSHSL1	/CS Deselect Time(for Array Read → Array Read)	10		ns
tSHSL2	/CS Deselect Time(for Erase, Program or Read Status Registers → Read Status Registers)	50		ns
tSHQZ	Output Disable Time		7	ns
tCLQV	Clock Low to Output Valid		7	ns
tCLQX	Output Hold Time	2		ns
tHLCH	/HOLD Active Setup Time relative to CLK	5		ns
tCHHH	/HOLD Active Hold Time relative to CLK	5		ns
tHHCH	/HOLD Not Active Setup Time relative to CLK	5		ns
tCHHL	/HOLD Not Active Hold Time relative to CLK	5		ns
tHHQX	/HOLD to Output Low-Z		7	ns
tHLQZ	/HOLD to Output High-Z		12	ns
tWHSL	Write Protect Setup Time Before /CS Low	20		ns
tSHWL	Write Protect Hold Time After /CS High	100		ns
tW	Status Register Write Time		50	ns
tRST	/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase		5/10/500	ns
tRD1	Read Page Data Time (ECC disabled)		25	us
tRD2	Read Page Data Time (ECC enabled)		60	us

3.6.5 SMI Interface

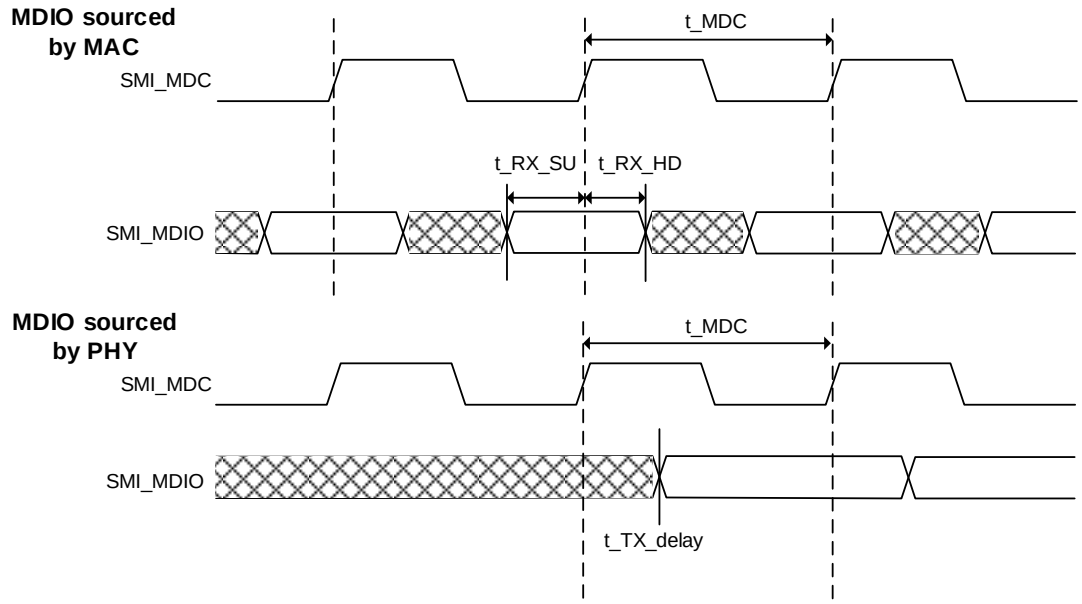


Figure 3-8 SMI MDIO Timing

Table 3-7 SMI Interface Diagram Key

Symbol	Description	Min	Max	Unit
t_TX_delay	Clock to output delay from the PHY	0	300	ns
t_RX_SU	Setup time referenced to the rising edge of SMI_MDC	10	-	ns
t_RX_HD	Hold time referenced to the rising edge of SMI_MDC	10	-	ns

Note: For 2.5 MHz SMI_MDC

3.6.6 WRI Interface

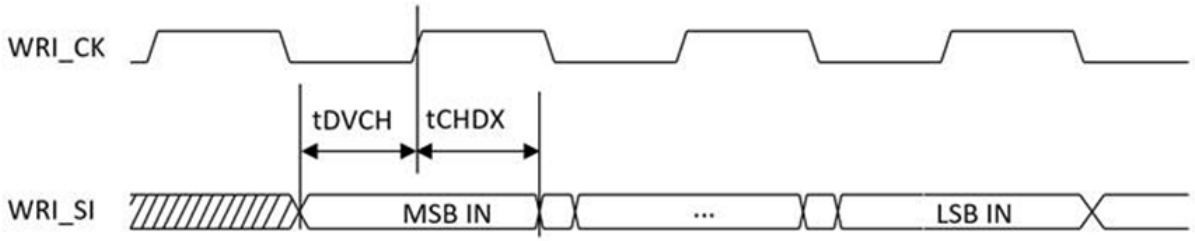


Figure 3-9 WRI Timing

Table 3-8 WRI Interface Diagram Key

Symbol	Description	Min	Max	Unit
tDVCH	Data in Setup Time	2	-	ns
tCHDX	Data In Hold Time	2	-	ns

3.6.7 I2C Interface

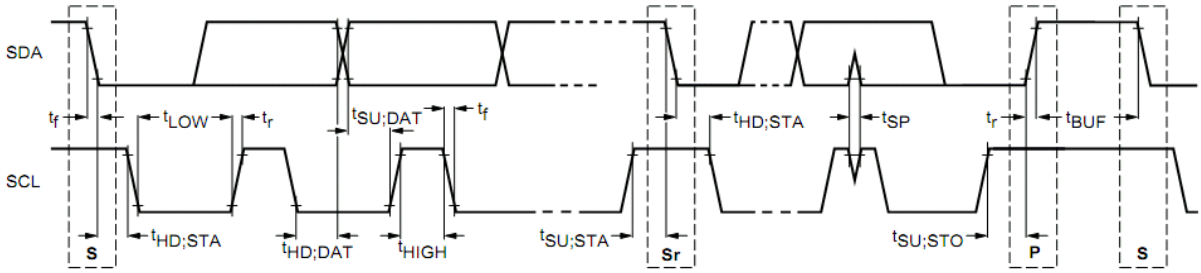


Figure 3-10 I2C Timing

Table 3-9 I2C Interface Diagram Key

Symbol	Description	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
fSCL	SCL clock frequency	0	100	0	400	kHz
tBUF	Bus free time between a STOP and START	4.7	-	1.3	-	us
tHD	condition	-	-	-	-	us
tLOW	Hold time (repeated) START condition.	4.7	-	1.3	-	us
tHIGH	After this period, the first clock pulse is generated	4.0		0.6		us
tSU:STA	LOW period of the SCL clock	4.7	-	0.6	-	us
THD:DAT	HIGH period of the SCL clock	-	-	-	-	us
tSU:DAT	Setup time for a repeated START condition	250	-	100	-	ns
tr	Data hold time:	-	1000	20	300	ns
tf	Data setup time	-	300	20	300	ns
tSU:STO	Rise time of both SDA and SCL signals	4.0	-	0.6	-	us

3.7 DC Electrical Characteristics

3.7.1 3.3V IO

Table 3-10 3.3V IO Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	-0.30	-	0.83	V
V_{IH}	Input high voltage	2.06	-	3.63	V
V_{OL}	Output low voltage	-0.30	-	0.41	V
V_{OH}	Output high voltage	2.48	-	3.63	V
R_{PU}	Input pull-up resistance	10	50	100	KΩ
R_{PD}	Input pull-down resistance	5	7.5	10	KΩ

3.7.2 1.8V IO

Table 3-11 1.8V IO Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	-0.30	-	0.63	V
V_{IH}	Input high voltage	1.17	-	2.10	V
V_{OL}	Output low voltage	-	-	0.45	V
V_{OH}	Output high voltage	1.35	-	-	V
R_{PU}	Input pull-up resistance	40	75	190	KΩ
R_{PD}	Input pull-down resistance	40	75	190	KΩ

3.8 Power on Sequence

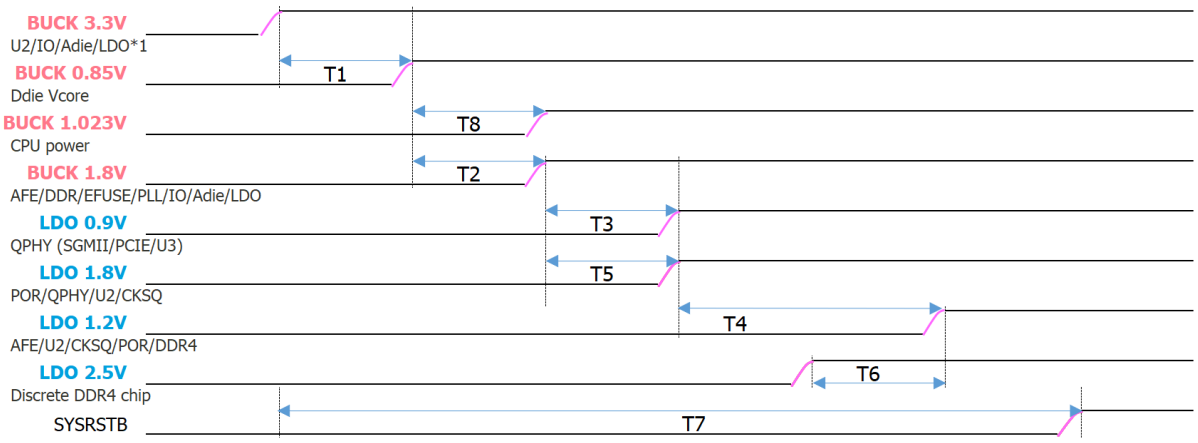


Figure 3-11 Power ON Sequence

Table 3-12 Power on sequence parameters

Symbol	Description	Min	Max	Unit
T1	BUCK_3.3V to BUCK_0.85V	0.5	5	ms
T2	BUCK_0.85V to BUCK_1.8V	0.5	5	ms
T8	BUCK_0.85V to BUCK_1.023V	0.5	5	ms
T3	BUCK_1.8V to LDO_0.9V	2	6	ms
T4	LDO_1.8V to LDO_1.2V	3	8	ms
T5	BUCK_1.8V to LDO_1.8V	2	6	ms
T6	LDO_2.5V to LDO_1.2V	1	-	ms
T7	BUCK_3.3V to SYSRSTB release	35	-	ms

4 Package Information

4.1 Dimensions – MFC VFBGA (16.85 x 16.85 x 0.9 mm)

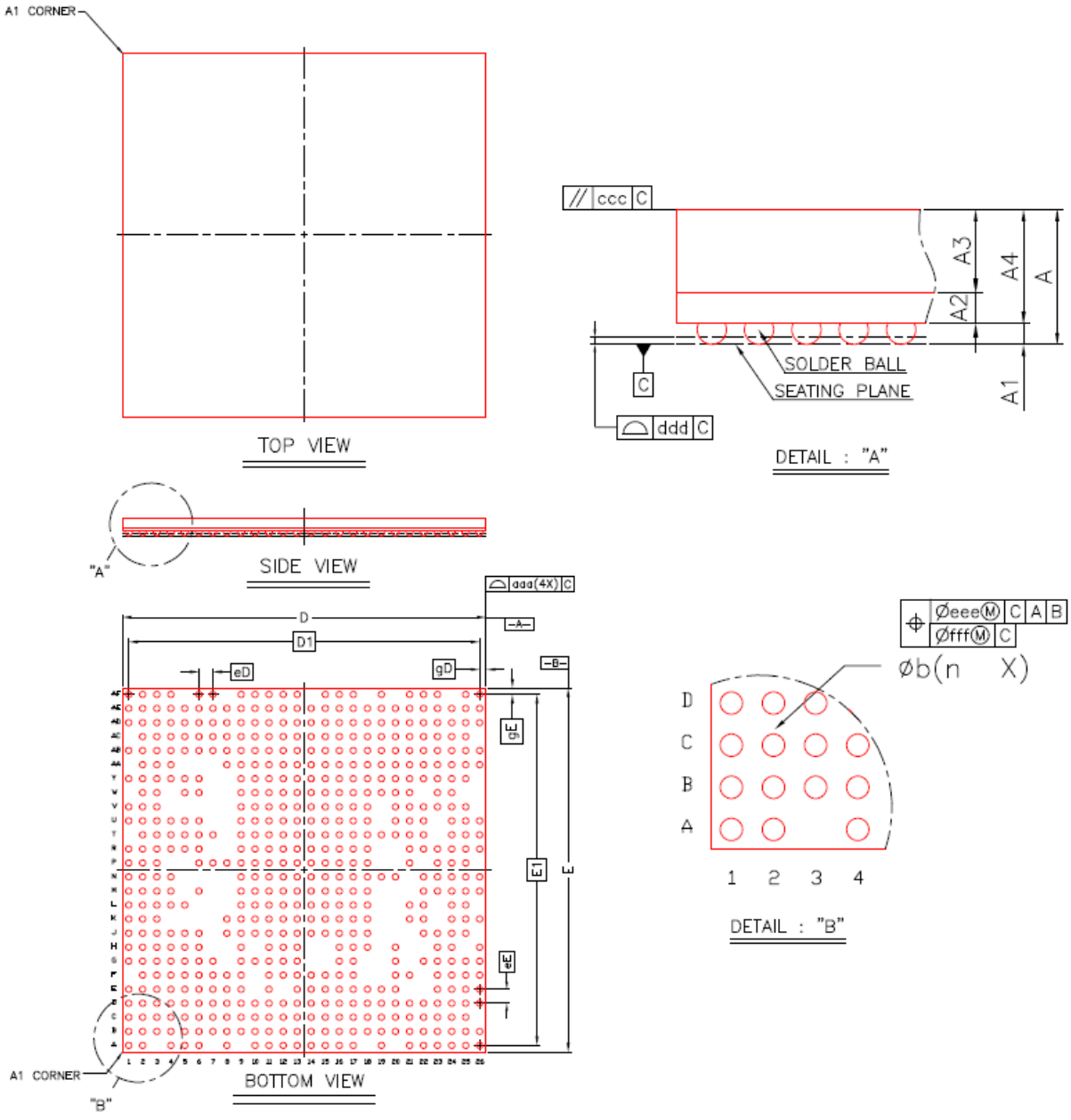


Figure 4-1 Package Dimension

NOTE:

1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. The pattern of pin 1 fiducial is for reference only.

4.1.1 Diagram Key

Table 4-1 Package Diagram Key

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	16.800	16.850	16.900
	Y	E	16.800	16.850	16.900
Ball Pitch	X	eD	0.650		
	Y	eE	0.650		
Mold Thickness		A3	0.450 Ref.		
Substrate Thickness		A2	0.145 Ref.		
Substrate+Mold Thickness		A4	0.545	0.595	0.645
Total Thickness		A	–	–	0.900
Ball Diameter			0.300		
Ball Stand Off		A1	0.160	0.210	0.260
Ball Width		b	0.250	0.300	0.350
Package Edge Tolerance		aaa	0.050		
Mold Flatness		ccc	0.150		
Coplanarity		ddd	0.120		
Ball Offset (Package)		eee	0.150		
Ball Offset (Ball)		fff	0.050		
Ball Count		n	570		
Edge Ball Center to Center	X	D1	16.250		
	Y	E1	16.250		
Edge Ball Center to Package Edge	X	gD	0.300		
	Y	gE	0.300		

4.2 Reflow Profile Guideline

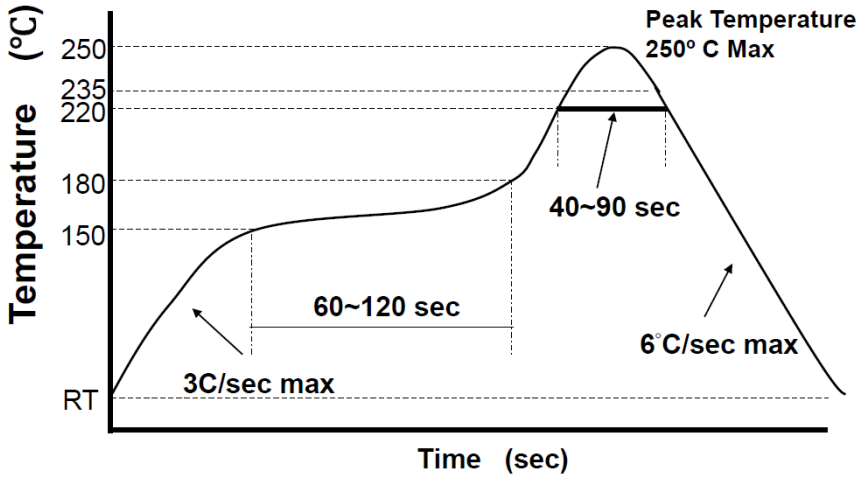
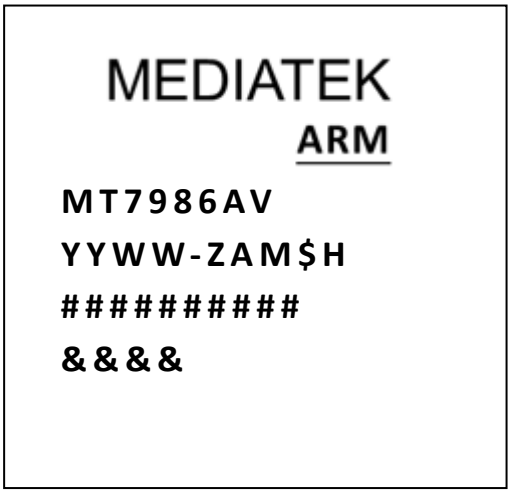


Figure 4-2 Reflow profile

Notes;
1.Reflow profile guideline is designed for SnAgCulead-free solder paste.
2.Reflow temperature is defined at the solder ball of package.
3.MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4.Appropriate N_2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

.

4.3 Top Marking



Description:

YYWW: Date code

#: LOT NO.

$/&: Internal control code

Figure 4-3 MT7986A Top marking

4.4 Ordering Information

Part Number	Package (Green/RoHS Compliant)
MT7986AV	16.85 x 16.85 mm, 570B-MFC VFBGA

Note: a heat sink is required in max ambient temperature.

MediaTek Inc. No. 1, Dusing 1st Rd., Hsinchu Science Park, Hsinchu City, Taiwan, R.O.C
Tel: +886-3-567-0766
Fax: +886-3-568-7610
www.mediatek.com