Mt7623 core module

Pupfish-MT7623A Spec

Specification Version 1.0.0

Author：RIVER

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Revision	Date	Contents of Revision Change	Remark
1.0.0	2017-08-03	First release	

1 INTRODUTION

The Pupfish-MT7623A module use the MT7623A chipset. MT7623A is a highly integrated network router system-on-chip used for high wireless performance, home entertainment, home automation and so on .

MT7623 is fabricated with advanced silicon process and integrates a Quad-core ARM® Cortex-A7 MPCoreTM operating up to 1.3GHz and more DRAM bandwidth. This SoC also includes a variety of peripherals, including MIPI, RGMII, PCIe2.0, USB2.0 OTG ,USB3.0 ports, and 5-port GbE switch. To support popular network applications, MT7623A also implements 10/100/1000 Ethernet RGMII interface, embedded a 5-ports Giga switch and supports 802.11ac/n WLAN connection thru its PCIe port.

MT7623A includes two wireless connectivity functions, WLAN, Bluetooth. The RF parts of those two blocks are put in the MT6625L chip. With two advanced radio technologies integrated into one single chip, MT7623A/MT6625L provides the best and most convenient connectivity solution among the industry. MT7623A/MT6625L implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms.

Besides the connectivity features, the hardware-based NAT engine with QoS embedded in MT7623A transporting the audio/video streams in higher priority than other non-timely services also enriches the home entertainment application. The SFQ separating P2P sessions from audio/video ones so that MT7623A guarantees the streaming service.

With the advanced technology and abundant features, MT7623A is well positioned to be the core of nextgeneration Smart WiFi AP router, and home gateway systems.

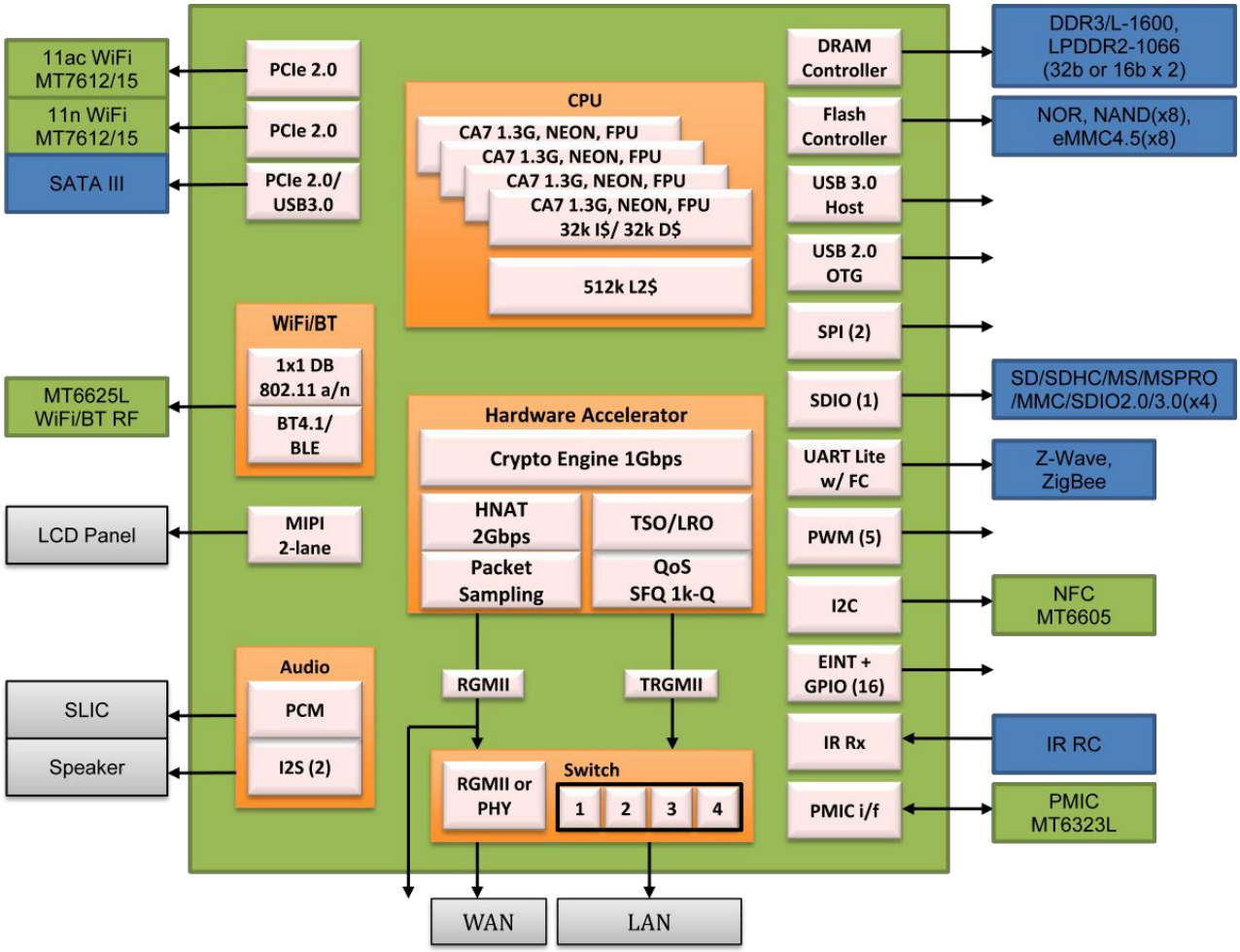
The Pupfish-MT7623A module include all the function from MT7623A chipset, it has two DDR3, a fast SPI flash. it will make the module runs faster.

Features

- Embedded Quad-core ARM® Cortex-A7 MPCore operating at 1.3GHz
- 2 x 512MB DDR3, 1 x 64Mbit SPI FLASH
- Use MT6323. It is a ideal for power management of 2G, 3G, smart phones and other portable systems.
- 1 x USB3.0, 2 x usb2.0, 5-ports Giga switch, 1 x JTAG, 1 x rgmii, 1 x aux, 2 x I2S, 2 x SPI, 1 x PCIE, 1 x I2C, 1 x PCM.

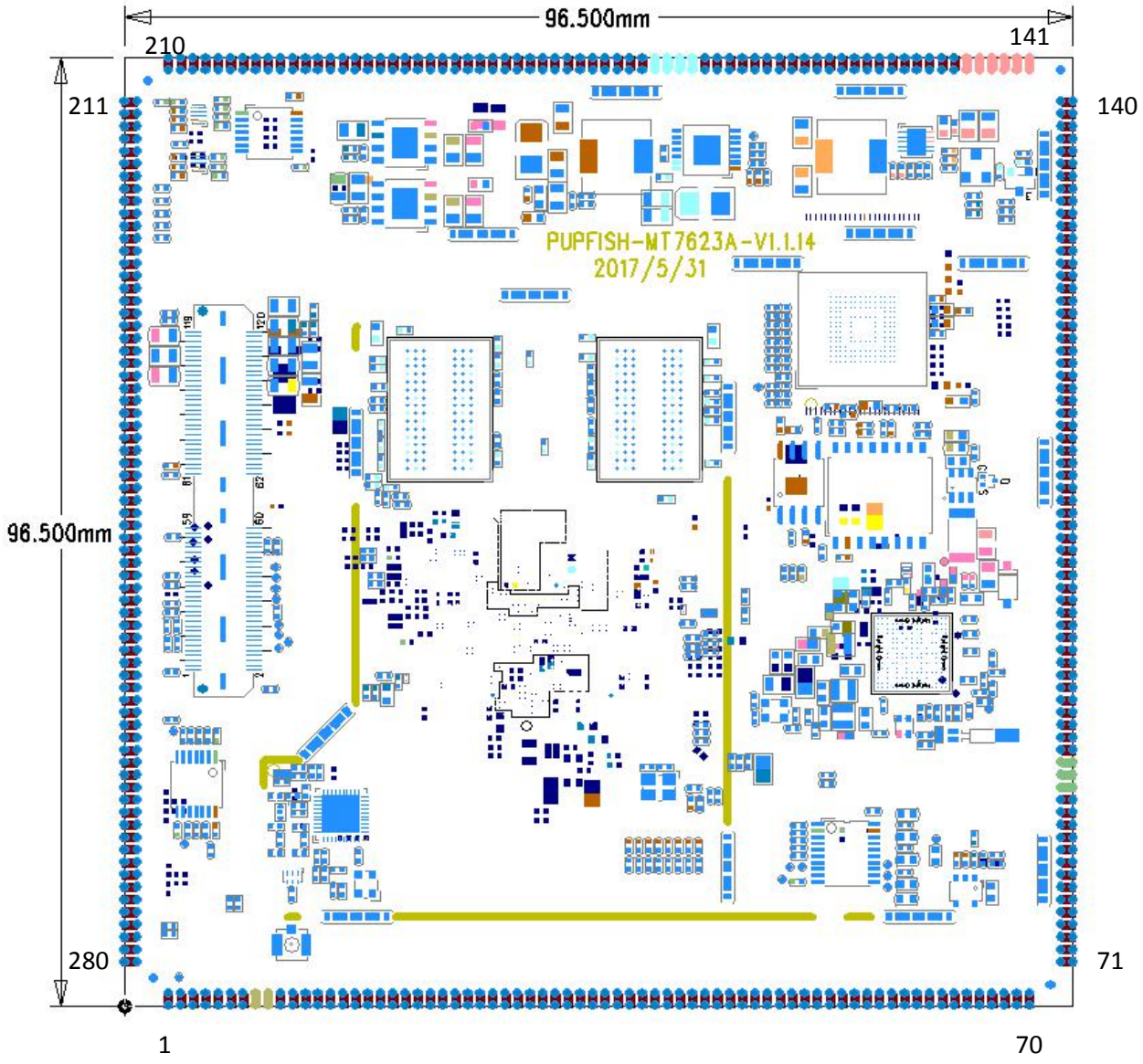
  1 x UART, 1 x MSDC, 2x PCIE, 1 x PCIE2.0/USB3.0
- VoIP support (I2S, PCM)
- Audio interface (I2S, PCM)

2 FUNCTIONAL BLOCK DIAGRAM



3 MECHANICAL

Dimensions (mm)	Length	Width	Height
	96.50 (Tolerance:±0.2mm)	96.50 (Tolerance:±0.2mm)	6.00 (Tolerance:±0.2mm)



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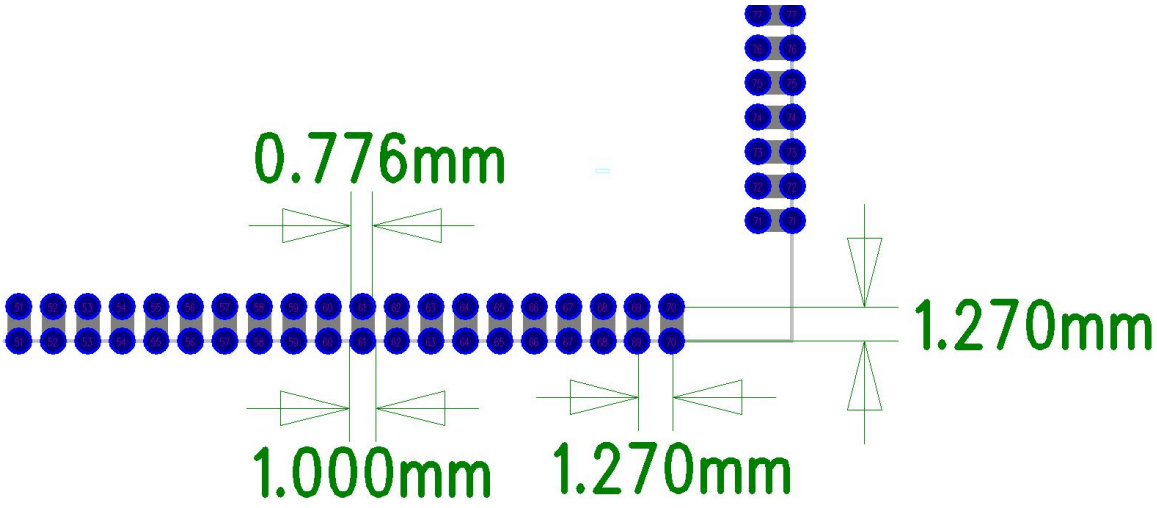
Pin describe:



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PIN NO.	FUNCTION	DESCRIPTION	
1	GND	GROUND	
2	NCEB1	NAND flash chip select1	
3	USB_DM_P2	USB port2 data pin Data- (USB2.0 OTG)	USB2.0
4	USB_DP_P2	USB port2 data pin Data+ (USB2.0 OTG)	
5	GPIO45	NAND flash chip select0	
6	GPIO237	Serial flash data bit #0	
7	USB_OCO#	External interrupt input3	
8	+5V_VBUS_OTG	+5V POWER IN	
9	+5V_VBUS_OTG	+5V POWER IN	USB3.0
10	USB_DM_1	USB port1 data pin Data- (USB3.0)	
11	USB_DP_1	USB port1 data pin Data+ (USB3.0)	
12	USB_TX_P1_1	USB port1 SS data pin TX+ (USB3.0)	
13	USB_TX_N1_1	USB port1 SS data pin TX- (USB3.0)	
14	USB_RX_P1	USB port1 SS data pin RX+ (USB3.0)	
15	USB_RX_N1	USB port1 SS data pin RX- (USB3.0)	
16	GND	GROUND	
17	GND	GROUND	Gigabit Ethernet
18	ESW_TXVP_A_P0	Port #0 MDI Transceivers	
19	ESW_TXVN_A_P0	Port #0 MDI Transceivers	
20	GND	GROUND	
21	ESW_TXVP_B_P0	Port #0 MDI Transceivers	
22	ESW_TXVN_B_P0	Port #0 MDI Transceivers	
23	GND	GROUND	
24	ESW_TXVP_C_P0	Port #0 MDI Transceivers	
25	ESW_TXVN_C_P0	Port #0 MDI Transceivers	
26	GND	GROUND	
27	ESW_TXVP_D_P0	Port #0 MDI Transceivers	
28	ESW_TXVN_D_P0	Port #0 MDI Transceivers	
29	GND	GROUND	
30	ESW_TXVP_A_P1	Port #1 MDI Transceivers	
31	ESW_TXVN_A_P1	Port #1 MDI Transceivers	
32	GND	GROUND	
33	ESW_TXVP_B_P1	Port #1 MDI Transceivers	
34	ESW_TXVN_B_P1	Port #1 MDI Transceivers	
35	GND	GROUND	
36	ESW_TXVP_C_P1	Port #1 MDI Transceivers	
37	ESW_TXVN_C_P1	Port #1 MDI Transceivers	
38	GND	GROUND	
39	ESW_TXVP_D_P1	Port #1 MDI Transceivers	
40	ESW_TXVN_D_P1	Port #1 MDI Transceivers	

41	GND	GROUND	Gigabit Ethernet
42	ESW_TXVP_A_P2	Port #2 MDI Transceivers	
43	ESW_TXVN_A_P2	Port #2 MDI Transceivers	
44	GND	GROUND	
45	ESW_TXVP_B_P2	Port #2 MDI Transceivers	
46	ESW_TXVN_B_P2	Port #2 MDI Transceivers	
47	GND	GROUND	
48	ESW_TXVP_C_P2	Port #2 MDI Transceivers	
49	ESW_TXVN_C_P2	Port #2 MDI Transceivers	
50	GND	GROUND	
51	ESW_TXVP_D_P2	Port #2 MDI Transceivers	
52	ESW_TXVN_D_P2	Port #2 MDI Transceivers	
53	GND	GROUND	
54	ESW_TXVP_A_P3	Port #3 MDI Transceivers	
55	ESW_TXVN_A_P3	Port #3 MDI Transceivers	
56	GND	GROUND	
57	ESW_TXVP_B_P3	Port #3 MDI Transceivers	
58	ESW_TXVN_B_P3	Port #3 MDI Transceivers	
59	GND	GROUND	
60	ESW_TXVP_C_P3	Port #3 MDI Transceivers	
61	ESW_TXVN_C_P3	Port #3 MDI Transceivers	
62	GND	GROUND	
63	ESW_TXVP_D_P3	Port #3 MDI Transceivers	
64	ESW_TXVN_D_P3	Port #3 MDI Transceivers	
65	GND	GROUND	
66	ESW_TXVP_A_P4	Port #4 MDI Transceivers	
67	ESW_TXVN_A_P4	Port #4 MDI Transceivers	
68	GND	GROUND	
69	ESW_TXVP_B_P4	Port #4 MDI Transceivers	
70	ESW_TXVN_B_P4	Port #4 MDI Transceivers	
71	ESW_TXVP_C_P4	Port #4 MDI Transceivers	
72	ESW_TXVN_C_P4	Port #4 MDI Transceivers	
73	GND	GROUND	
74	ESW_TXVP_D_P4	Port #4 MDI Transceivers	
75	ESW_TXVN_D_P4	Port #4 MDI Transceivers	
76	GND	GROUND	
77	TRST	JTAG reset	JTAG
78	TDO	JTAG data input	
79	TMS	JTAG mode select	
80	TCK	JTAG clock	
81	RTCK	return signal test clock	

82	TDI	JTAG data output	JTAG
83	NRST	Power on reset	
84	JTAG_RESET	JTAG target reset	
85	+1.8V	1.8V	
86	+1.8V	1.8V	
87	+1.8V	1.8V	
88	GND	GROUND	
89	GPIO255	GPIO255	
90	GPIO253	GPIO253	
91	GE_RST_N	Gigabit Ethernet RESET	RGMII
92	G2_TXD3_R	RGMII2 TX data bit #3	
93	G2_TXD2_R	RGMII2 TX data bit #2	
94	G2_TXD1_R	RGMII2 TX data bit #1	
95	G2_TXD0_R	RGMII2 TX data bit #0	
96	G2_TXEN_P	RGMII2 TX data valid	
97	G2_TXCLK_R	RGMII2 TX clock	
98	GND	GROUND	
99	G2_RXD0	RGMII2 RX data bit #0	
100	G2_RXD1	RGMII2 RX data bit #1	
101	G2_RXD2	RGMII2 RX data bit #2	
102	G2_RXD3	RGMII2 RX data bit #3	
103	G2_RXDV	RGMII2 RX data valid	
104	G2_RXCLK	RGMII2 RX clock	
105	MDC_1	PHY management clock	
106	MDIO_1	PHY management data	
107	GPIO15	GPIO15	
108	GPIO14	GPIO14	
109	SPIO_CSN2	GPIO	
110	SPIO_CK2	GPIO	
111	SRCLKENI	26MHz co-clock enable input	
112	GPIO124	GPIO124	
113	GPIO125	GPIO125	
114	AUX_IN0	AuxADC external input channel 0	AUX
115	AUX_IN1	AuxADC external input channel 1	
116	AUX_IN2	AuxADC external input channel 2	
117	AUX_IN3	AuxADC external input channel 3	
118	AUX_IN4	AuxADC external input channel 4	
119	AUX_IN5	AuxADC external input channel 5	
120	GND	GROUND	
121	GPIO37	I2S master clock for CODEC	I2S
122	GPIO36	I2S word select	

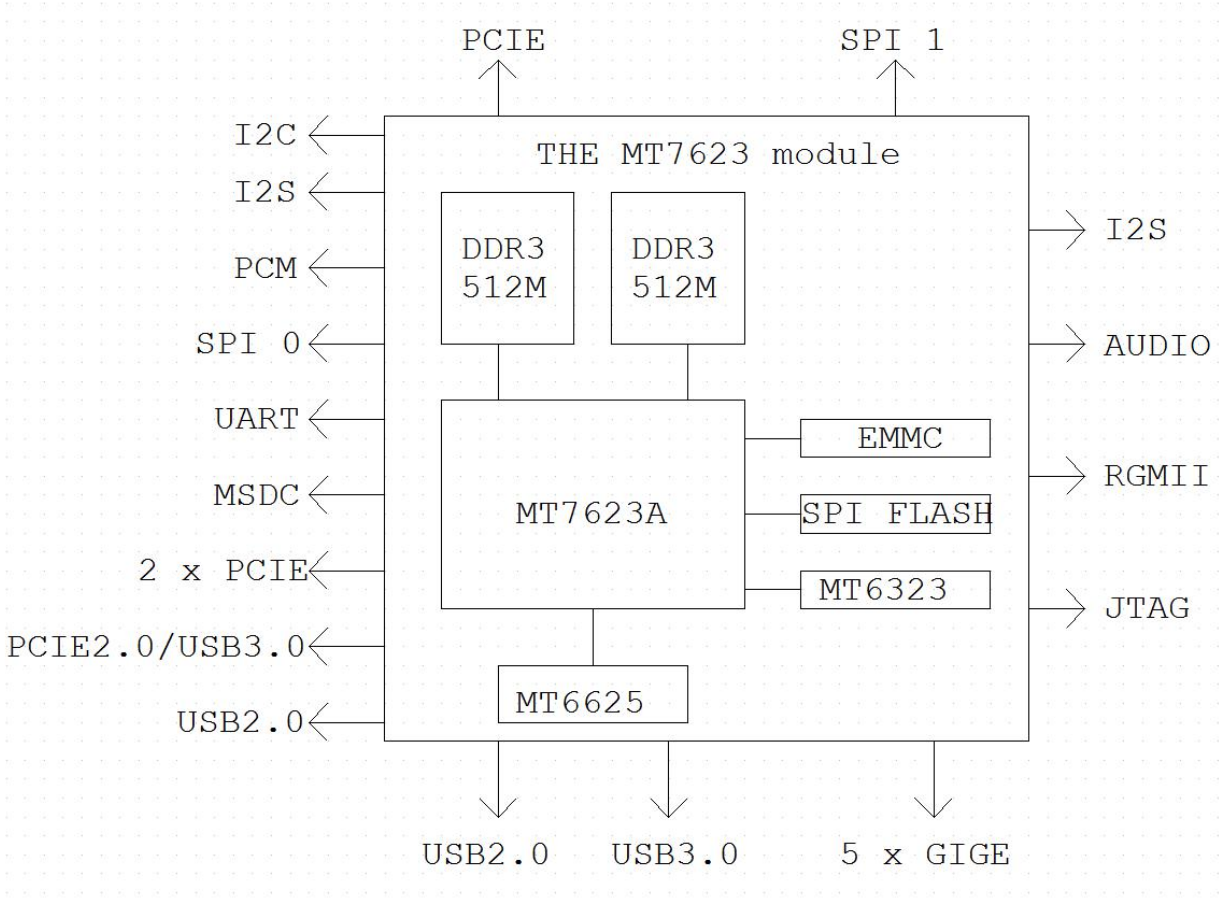
123	GPIO34	I2S data input	I2S
124	GPIO35	I2S bit clock	
125	GPIO33	I2S data output	
126	GND	GROUND	
127	GND	GROUND	
128	GND	GROUND	
129	GND	GROUND	
130	GND	GROUND	
131	GND	GROUND	
132	GND	GROUND	
133	GND	GROUND	
134	GND	GROUND	
135	GND	GROUND	
136	GND	GROUND	
137	GND	GROUND	
138	GND	GROUND	
139	GND	GROUND	
140	GND	GROUND	
141	VBAT_F	POWER IN	
142	VBAT_F	POWER IN	
143	VBAT_F	POWER IN	
144	VBAT_F	POWER IN	
145	VBAT_F	POWER IN	
146	VBAT_F	POWER IN	
147	GND	GROUND	
148	GND	GROUND	
149	GND	GROUND	
150	GND	GROUND	
151	GND	GROUND	
152	GND	GROUND	
153	GND	GROUND	
154	GND	GROUND	
155	GND	GROUND	
156	GND	GROUND	
157	GND	GROUND	
158	GND	GROUND	
159	GND	GROUND	
160	GND	GROUND	
161	GND	GROUND	
162	GND	GROUND	
163	GND	GROUND	

164	GND	GROUND	
165	GND	GROUND	
166	GND	GROUND	
167	GND	GROUND	
168	+ 12VD	+ 12V	
169	+ 12VD	+ 12V	
170	+ 12VD	+ 12V	
171	+ 12VD	+ 12V	
172	GND	GROUND	
173	GND	GROUND	
174	GND	GROUND	
175	GND	GROUND	
176	+ 5V_PCIE	PCIE POWER + 5V	
177	+ 5V_PCIE	PCIE POWER + 6V	
178	+ 5V_PCIE	PCIE POWER + 7V	
179	+ 5V_PCIE	PCIE POWER + 8V	
180	+ 5V_PCIE	PCIE POWER + 9V	
181	GND	GROUND	
182	GND	GROUND	
183	GND	GROUND	
184	GND	GROUND	
185	GND	GROUND	
186	GND	GROUND	
187	GND	GROUND	
188	GND	GROUND	
189	GND	GROUND	
190	GND	GROUND	
191	GND	GROUND	
192	GND	GROUND	
193	GND	GROUND	
194	EN_3V3	ENABLE 3.3V	SPI 1
195	GPIO7	SPI port1 chip select	
196	GPIO199	SPI port1 clock	
197	GPIO8	SPI port1 data in	
198	GPIO9	SPI port1 data out	
199	GND	GROUND	
200	GND	GROUND	
201	GND	GROUND	
202	GND	GROUND	
203	GPIO207	Pulse width modulator	
204	GND	GROUND	

205	GND	GROUND	
206	GND	GROUND	
207	I2C_SDA2	GPIO122	
208	I2C_SCL2	GPIO123	
209	GND	GROUND	
210	GPIO257	GPIO257	
211	GPIO256	GPIO256	
212	GPIO204	Pulse width modulator	
213	GPIO205	Pulse width modulator	
214	GPIO206	Pulse width modulator	
215	I2C_SCL0	I2C clock	I2C
216	I2C_SDA0	I2C data	
217	GND	GROUND	
218	I2S0_MCLK_CODEC	I2S master clock for CODEC	I2S
219	I2S0_DATA_CODEC	I2S data output	
220	I2S0_BCK_CODEC	I2S bit clock	
221	I2S0_LRCK_CODEC	I2S word select	
222	I2S0_DATA_IN_CODEC	I2S data input	
223	GND	GROUND	
224	GND	GROUND	
225	GND	GROUND	
226	PCM_HW_RST_N	PCM RESET	PCM
227	PCM_RST_N	External interrupt input0	
228	PCM_SYNC	PCM frame sync	
229	PCM_RX	PCM RX data	
230	PCM_TX	PCM TX data	
231	PCM_CLK	PCM clock	
232	SPI0_MO	SPI port0 data out	SPI 0
233	SPI0_CK	SPI port0 clock	
234	SPI0_CSN	SPI port0 chip select	
235	SPI0_MI	SPI port0 data in	
236	URTS2	UART request to send	UART
237	UCTS2	UART clear to send	
238	UTXD2	UART TX data	
239	URXD2	UART RX data	
240	GND	GROUND	
241	MSDC1_WP	MSDC External interrupt input7	MSDC
242	MSDC1_DATA1	MSDC port1 data bit #1	
243	MSDC1_DAT2	MSDC port1 data bit #2	
244	MSDC1_INS	MSDC port1 card insert	
245	MSDC1_CMD	MSDC port1 command	

246	MSDC1_CLK	MSDC port1 clock	MSDC
247	MSDC1_DAT0	MSDC port1 data bit #0	
248	MSDC1_DAT3	MSDC port1 data bit #3	
249	GND	GROUND	
250	PCIE_WAKE_N	PCIE External interrupt input6	PCIE0
251	PCIE0_PERST_N	Audio clock in1	
252	PCIE0_CLKREO_N_IO33	GPIO250	
253	PCIE_CK_NO	PCIe port0 reference clock (negative)	
254	PCIE_CK_PO	PCIe port0 reference clock (positive)	
255	PCIE_TX_PO	PCIe port0 differential transmit TX+	
256	PCIE_TX_NO	PCIe port0 differential transmit TX-	
257	PCIE_RXPO	PCIe port0 differential receive RX +	
258	PCIE_RXNO	PCIe port0 differential receive RX-	
259	GND	GROUND	
260	PCIE1_WAKE_N	External interrupt input5	PCIE1
261	PCIE1_PERST_N	Audio clock in2	
262	PCIE1_CLKREQ_N_IO33	GPIO252	
263	PCIE_TX_P1	PCIe port1 differential transmit TX+	
264	PCIE_TX_N1	PCIe port1 differential transmit TX -	
265	PCIE_RXP1	PCIe port1 differential receive RX +	
266	PCIE_RXN1	PCIe port1 differential receive RX -	
267	PCIE_CK_P1	PCIe port1 reference clock (positive)	
268	PCIE_CK_N1	PCIe port1 reference clock (negative)	
269	GND	GROUND	
270	PCIE2_WAKE_N	External interrupt input4	PCIE2
271	PCIE2_PERST_N	External interrupt input2	
272	PCIE2_CLKREQ_N_IO33	GPIO254	
273	PCIE_CK_P2	PCIe port2 reference clock (positive)	
274	PCIE_CK_N2	PCIe port2 reference clock (negative)	
275	PCIE_RXN2	PCIe port2 differential receive RX-	
276	PCIE_RXP2	PCIe port2 differential receive RX +	
277	PCOE_TX_N2	PCIe port2 differential transmit TX -	
278	PCIE_TX_P2	PCIe port2 differential transmit TX+	
279	USB_DMO	USB port0 data pin Data-	USB 2.0
280	USB_DPO	USB port0 data pin Data+	

4 BLOCK DIAGRAM OF SCHEMATIC



5 REFLOW SOLDERING TEMPERATURE CURVE

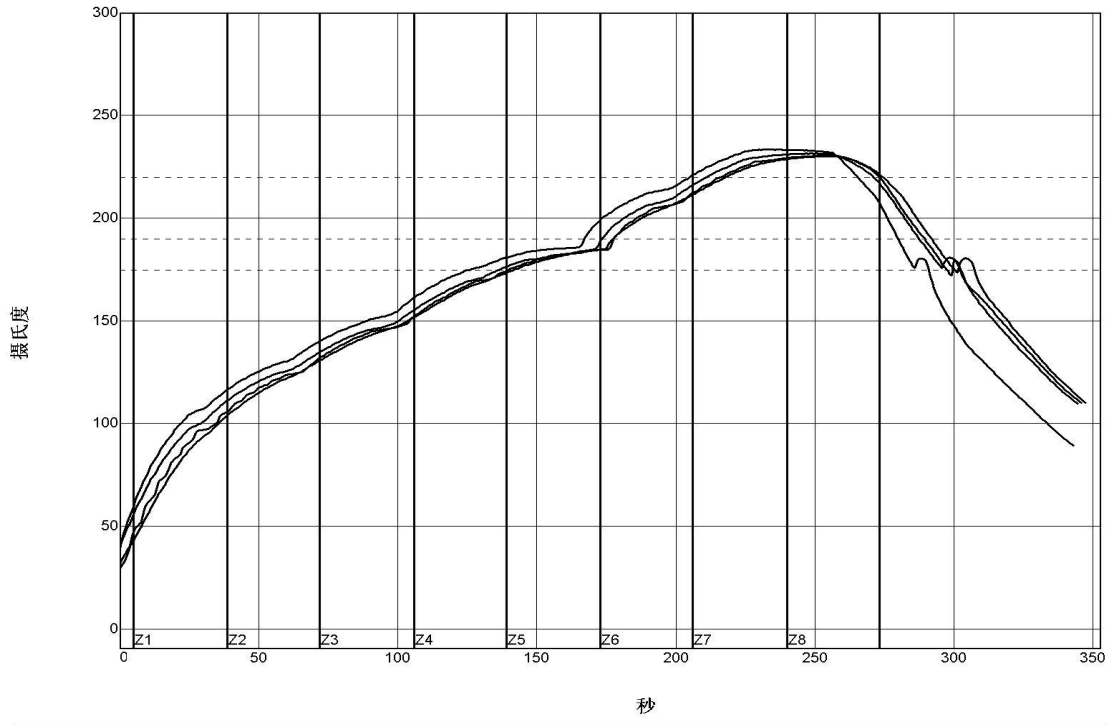
My First Product 周一 **2014年04月07日, 15:27:55**

炉子名称：**JTR-800** 制程界限名称：**System Default for Reflow**

温度设置 (摄氏度)

温区	1	2	3	4	5	6	7	8
上温区	125	135	155	185	195	225	240	230
下温区	125	135	155	185	195	225	240	230

传送带速度 (公分/分): 70.0



PWI= 94%	恒温时间175至190C		回流时间 /220C		最高温度	
<TC2>	35.53	-82%	55.58	-72%	230.28	-94%
<TC3>	37.66	-74%	58.66	-57%	230.56	-89%
<TC4>	41.52	-62%	60.63	-47%	233.62	-28%
<TC5>	37.07	-76%	60.44	-48%	231.67	-67%
温差	5.99		5.05		3.34	

制程界限:

锡膏: System Default for Reflow

统计数名称	最低界限	最高界限	单位
恒温时间175-190摄氏度	30	90	秒
回流以上时间 - 220摄氏度	50	90	秒
最高温度	230	240	度 摄氏度

描述:

KIC
San Diego, CA USA

温度曲线是由 KIC 科技所得
电话: +1-858-673-6050
传真: +1-858-673-0085

www.kicthermal.com
tech@kicmail.com

6 MODULE OPERATING ENVIRONMENT

Working temperature: 0 ℃ to 40 ℃;

Storage temperature: -40 ℃ to 70 ℃;

Humidity: 10% to 90% RH no condensation;

Storage humidity: 5% to 90% RH no condensation.