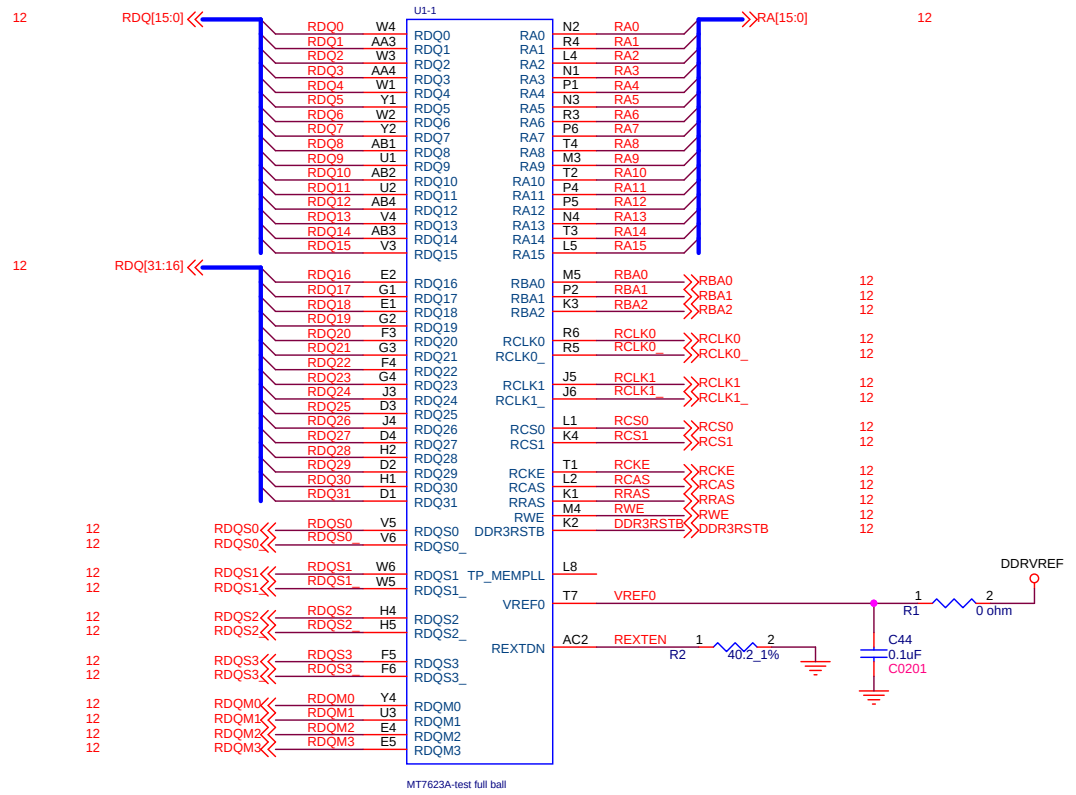
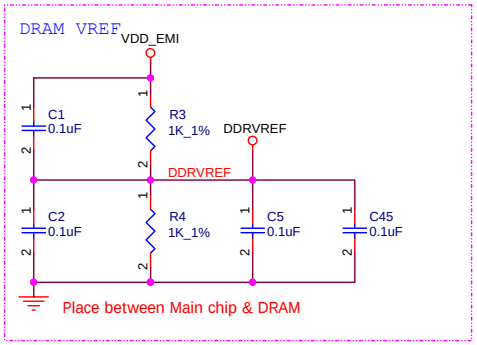
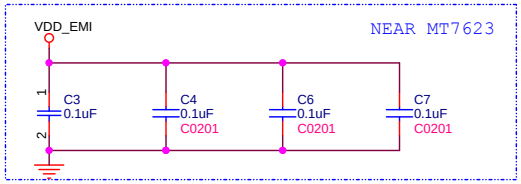
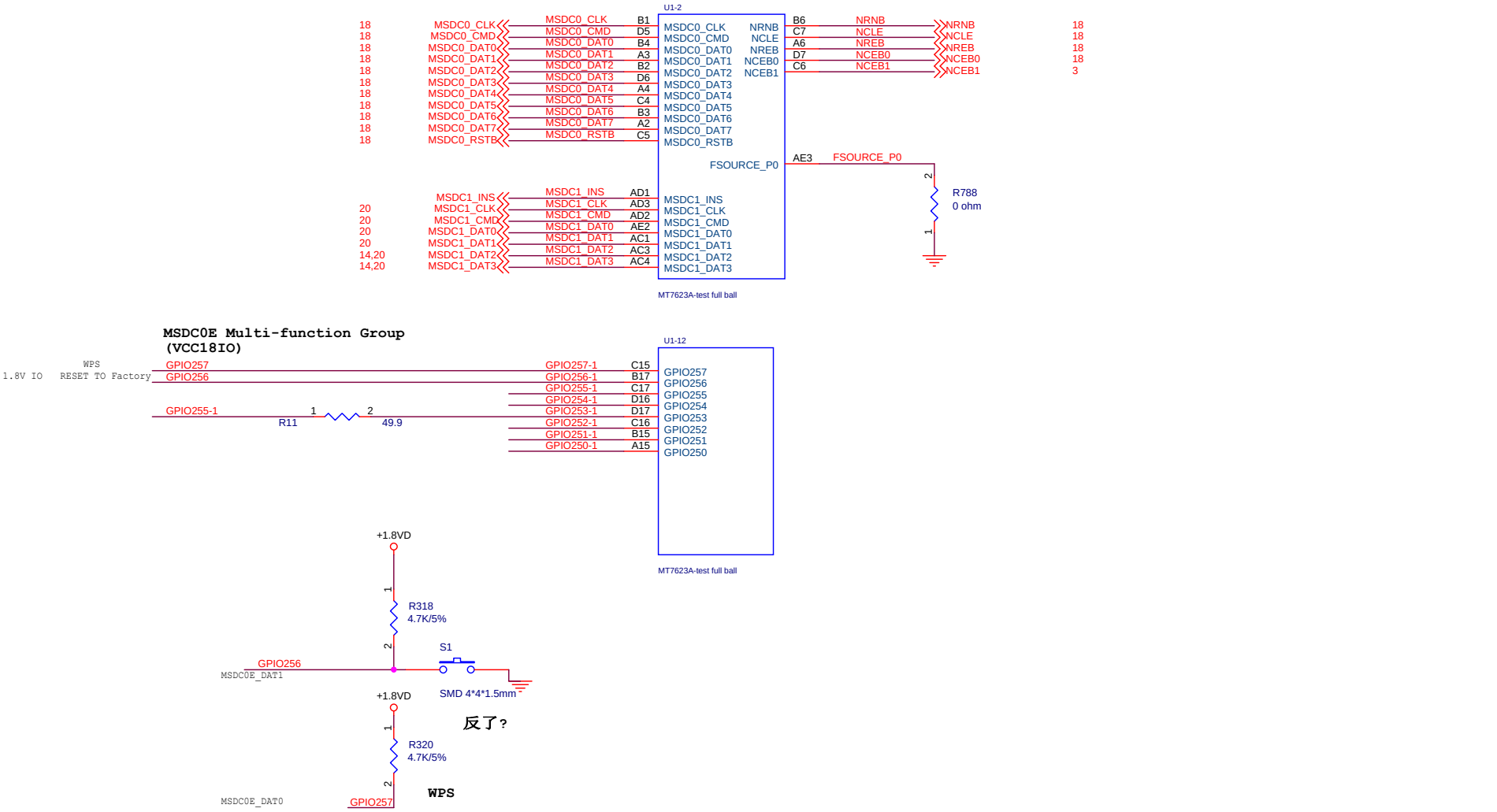


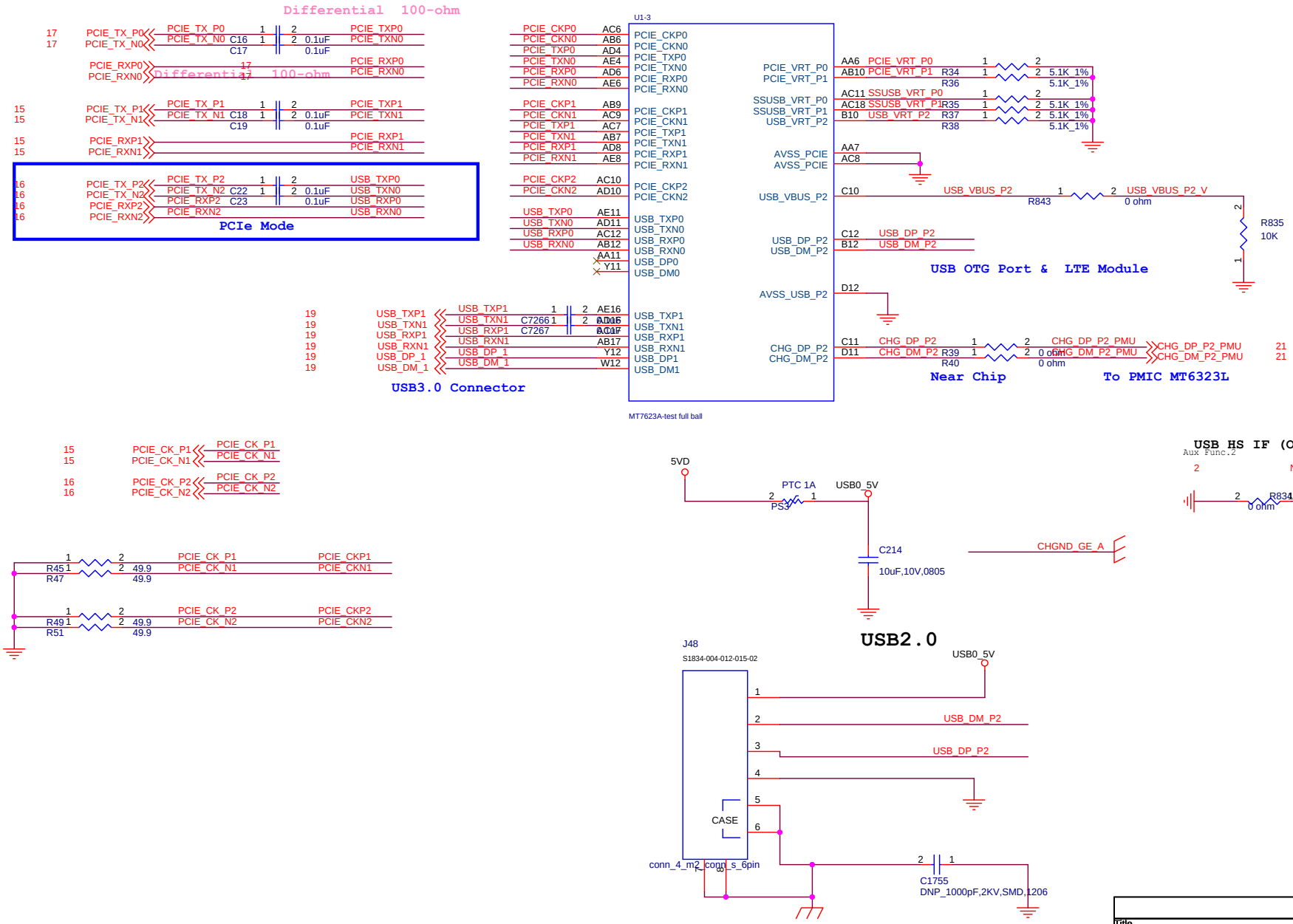




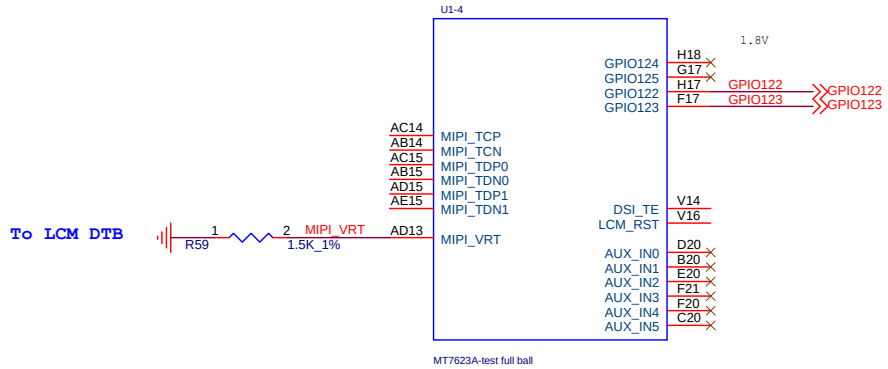
Title: MT7623_DRAM		
Size: B	Document Number: U7623-10	Rev: 1.0
Date: Tuesday, August 04, 2020	Sheet 1 of 25	

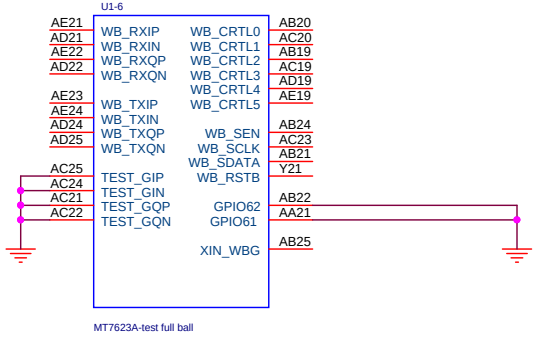


Title	MT7623_MSDC	
Size: B	Document Number: U7623-10	Rev: 1.0
Date: Tuesday, August 04, 2020	Sheet 2 of 25	

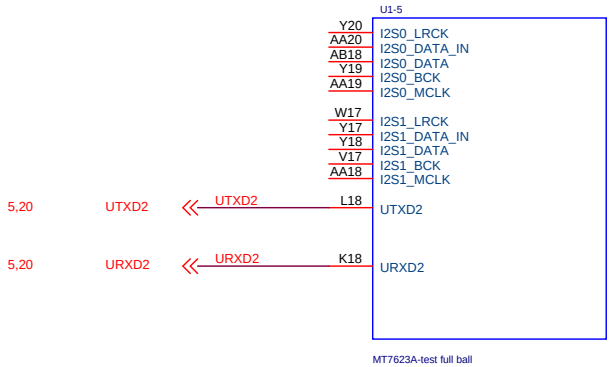


Title	MT7623_HIF_PCIe_USB3	
Size: B	Document Number: U7623-10	Rev: 1.0
Date: Friday, August 07, 2020	Sheet 3 of 25	

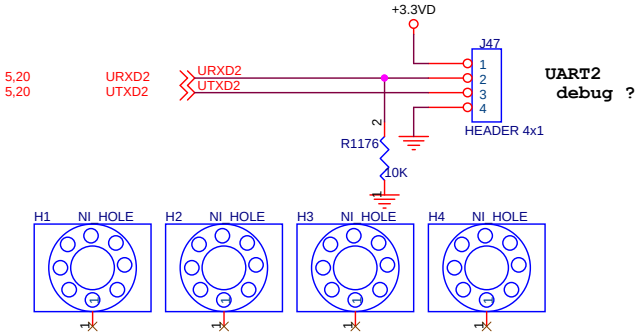




Title: MT7623_MIPI_WB			
Size: B	Document Number: U7623-10		Rev: 1.0
Date: Tuesday, August 04, 2020	Sheet 4 of 25		

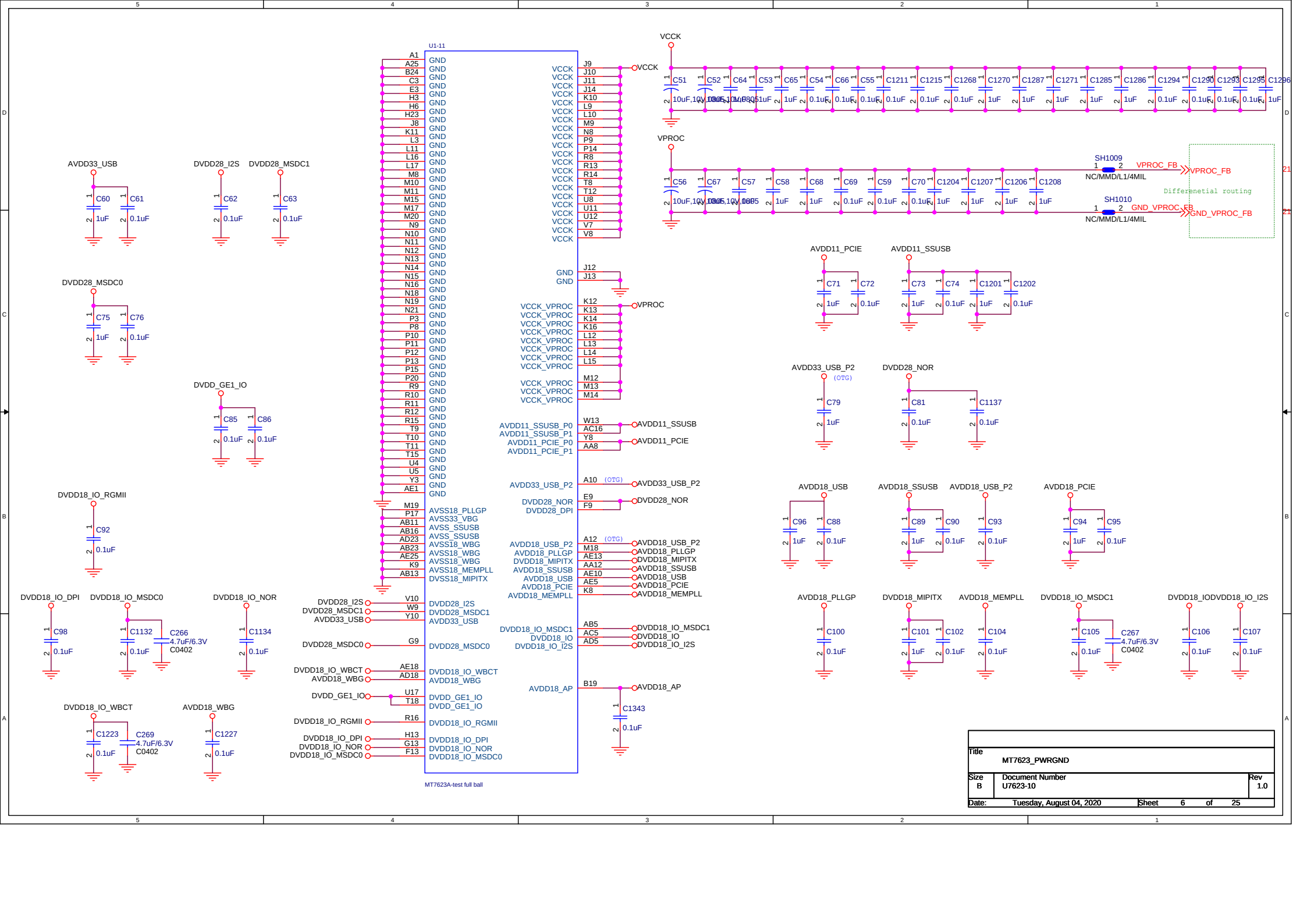


MT7623	UART-0	I2C-2
GPIO123	UTX0	SCL2
GPIO122	URX0	SDA2



I2S0 Audio Codec

Title: MT7623_I2S_WM8960			
Size: B	Document Number: U7623-10		Rev: 1.0
Date: Tuesday, August 04, 2020		Sheet 5 of 25	


U1-11
MT7623A-test full ball
VCCK
VPROC
AVDD33_USB
DVDD28_I2S
DVDD28_MSDC1
DVDD28_MSDC0
DVDD_GE1_IO
DVDD18_IO_RGMII
DVDD18_IO_DPI
DVDD18_IO_MSDC0
DVDD18_IO_NOR
DVDD18_IO_WBCT
AVDD18_WBG
AVDD11_PCIE
AVDD11_SSUSB
AVDD33_USB_P2
DVDD28_NOR
AVDD18_USB
AVDD18_SSUSB
AVDD18_USB_P2
AVDD18_PCIE
AVDD18_PLLGP
DVDD18_MIPITX
AVDD18_MEMPLL
DVDD18_IO_MSDC1
DVDD18_IODVDD18_IO_I2S
SH1009
SH1010
VPROC_FB
GND_VPROC_FB
NC/MMD/L1/4MIL
Differenetial routing
Title
MT7623_PWRGND
Size
B
Document Number
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1.0
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6
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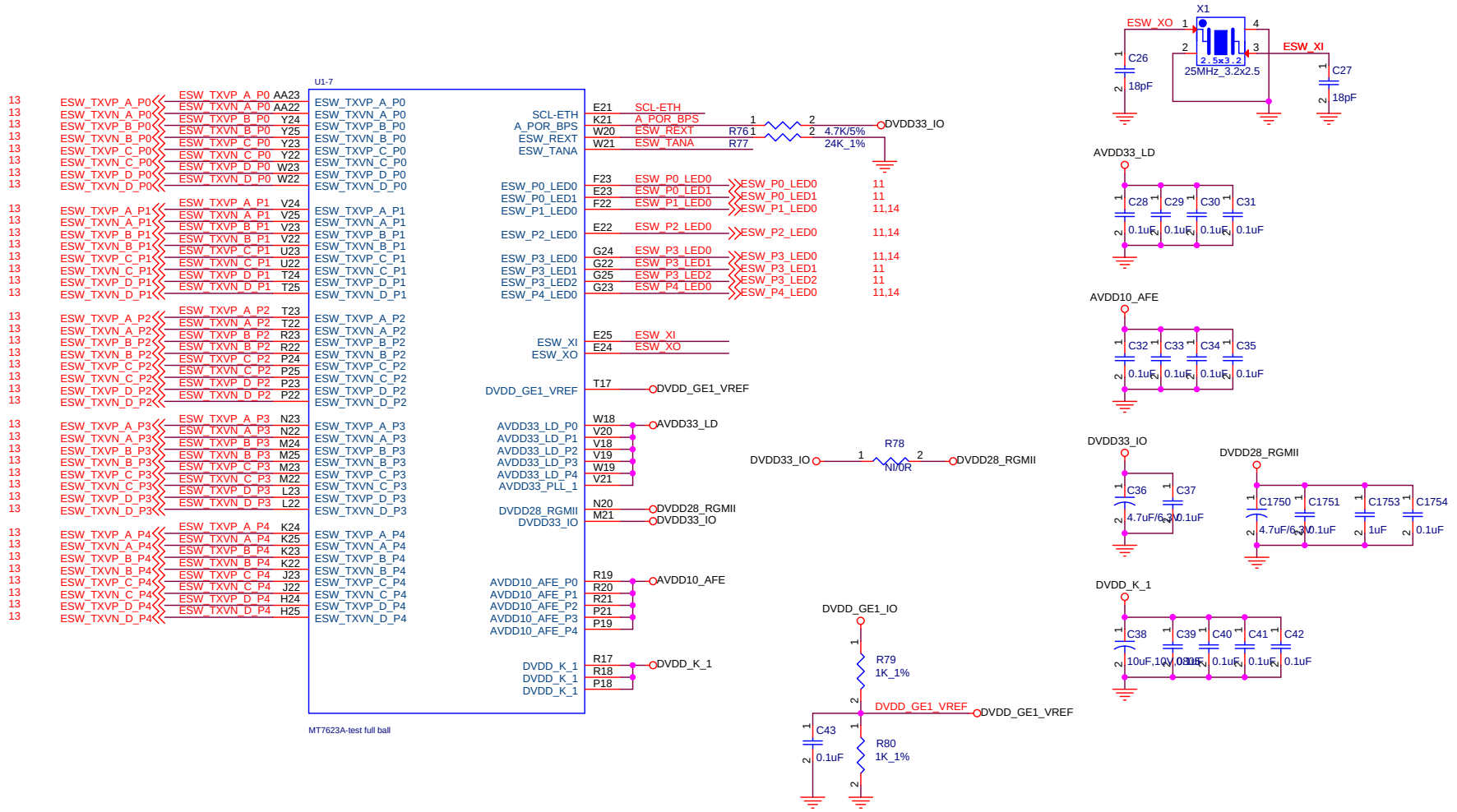
25



Title	MT7623_ETH	
Size B	Document Number U7623-10	Rev 1.0
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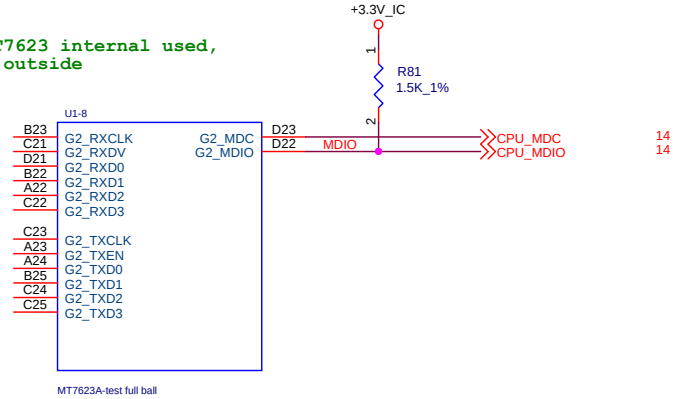
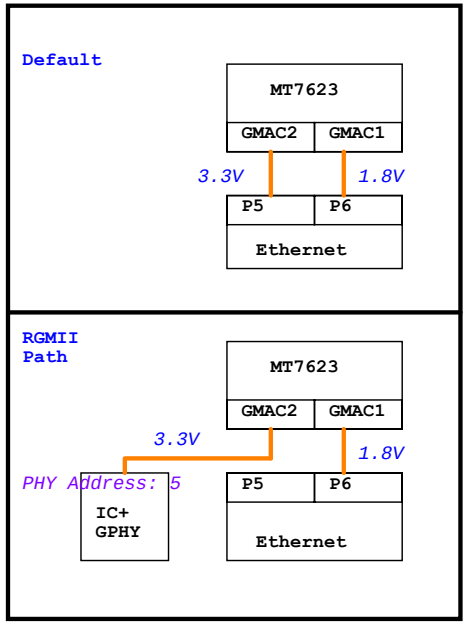
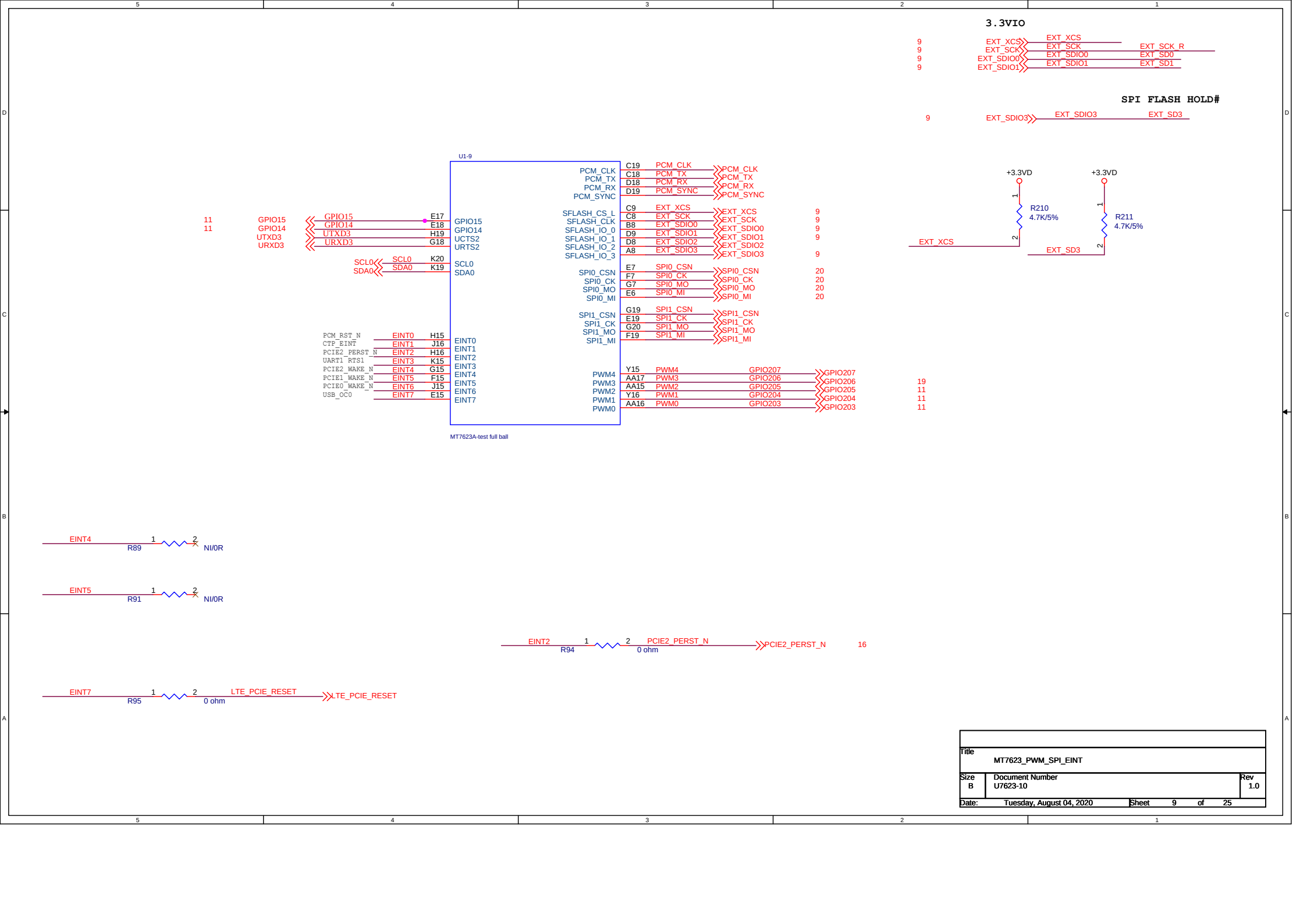
When GE2 Group for MT7623 internal used,
please keep floating outside

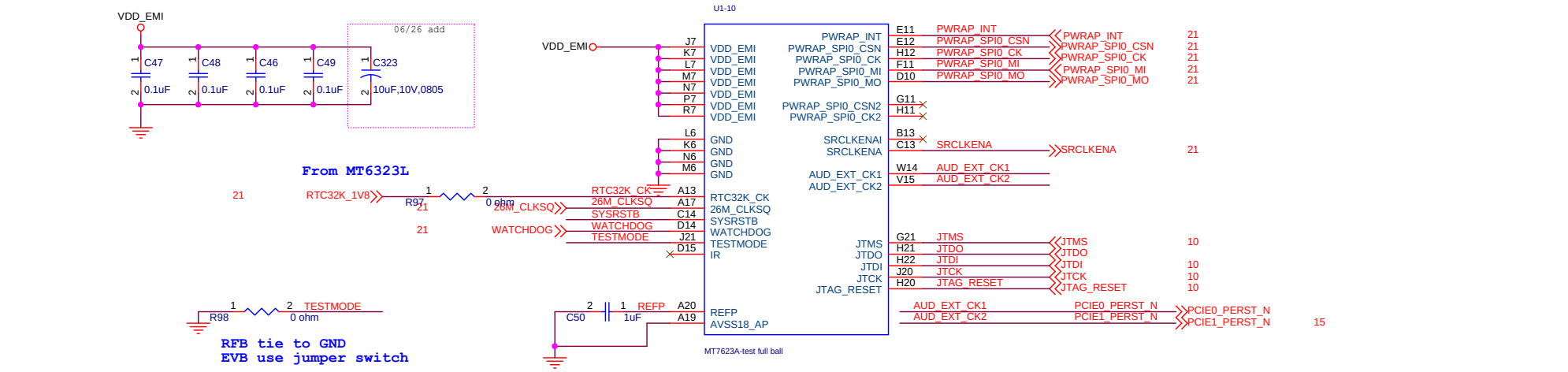


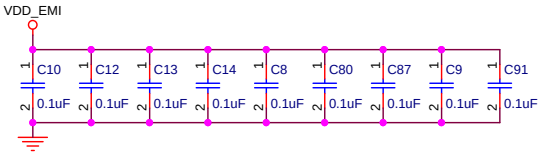


Title: MT7623_RGMII		
Size: B	Document Number: U7623-10	Rev: 1.0
Date: Tuesday, August 04, 2020	Sheet 8 of 25	

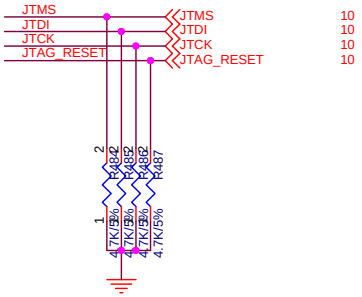


Title	MT7623_PWM_SPI_EINT	
Size B	Document Number U7623-10	Rev 1.0
Date: Tuesday, August 04, 2020	Sheet 9 of 25	





C50 Close to MT7623
AVSS18_AP should connect to C50.2 first,
than connect to GND by via



Chip Reset Source
One is from PMIC, the other is from RESET IC

Title	MT7623_PMIC_JTAG		
Size B	Document Number U7623-10		Rev 1.0
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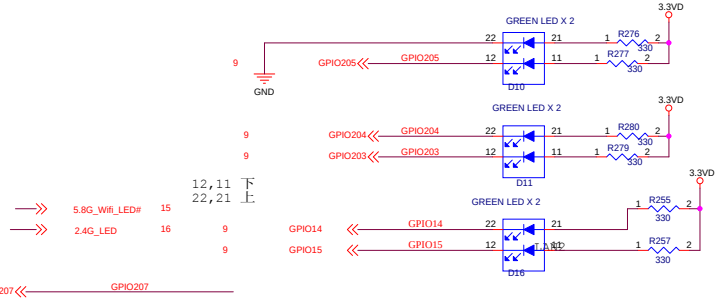
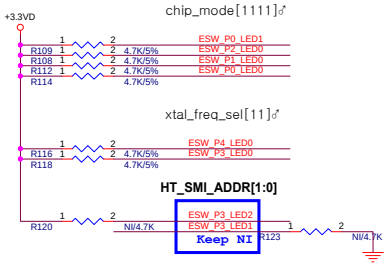
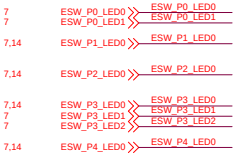
GigaSwitch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P0_LED_2	HWTRAP[4]	HT_EEPROM_EN	1'b0: disable external EEPROM 1'b1: External EEPROM used	1'b1
P1_LED_1	HWTRAP[5]	HT_C_MDIO_BPS_N	1'b0: Directly access PHY registers via C_MDC/C_MDIO 1'b1: Indirectly access PHY registers	1'b1
P1_LED_2	HWTRAP[6]	HT_P5_INTF_DIS	1'b0: enable 1'b1: disable	1'b1
P2_LED_1	HWTRAP[7]	HT_P5_INTF_MODE	1'b0: GMII/MII 1'b1: RGMII	1'b1
P2_LED_2	HWTRAP[8]	HT_P6_INTF_DIS	1'b0: enable 1'b1: disable	1'b1
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b11: 25MHz	2'b11
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		
P3_LED_2	HWTRAP[12]	HT_SMI_ADDR[1:0]	chip_smi_addr[4:3] Bits 4 and 3 of the chip SMI address chip_smi_addr[2:0] = 3'b111	2'b11
P3_LED_1	HWTRAP[11]			
P4_LED_1	HWTRAP[13]	HT_P5_INTF_SEL	1'b0: connect to GPHY4 1'b1:connect to GMAC5	1'b1
P4_LED_2	HWTRAP[14]	HT_LOOPDET_DIS	1'b0: loop detection enable 1'b1: loop detection disable	1'b1



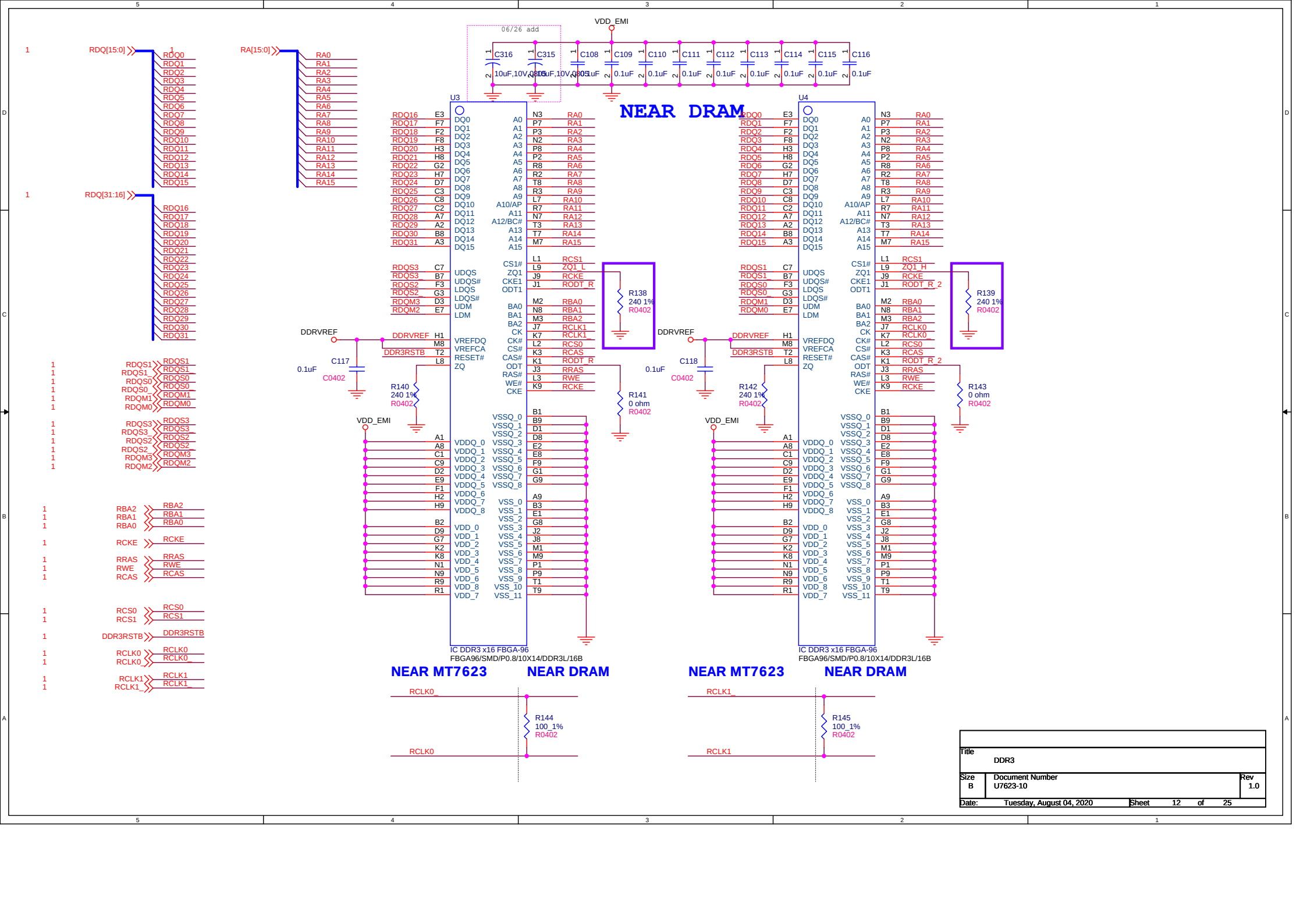




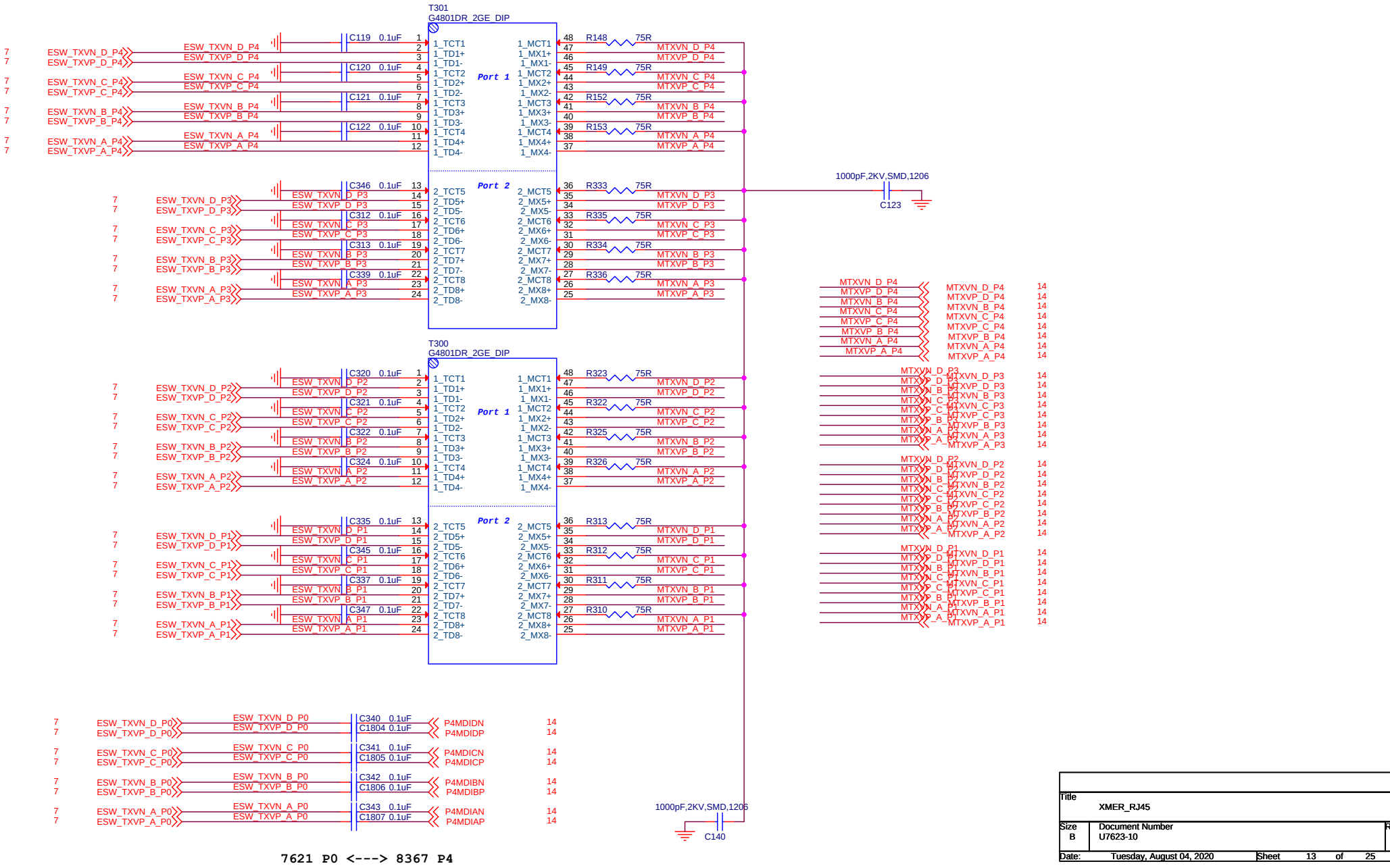
Ethernet HW Trapping

4b'1111 Normal Mode
2b'11 25MHz

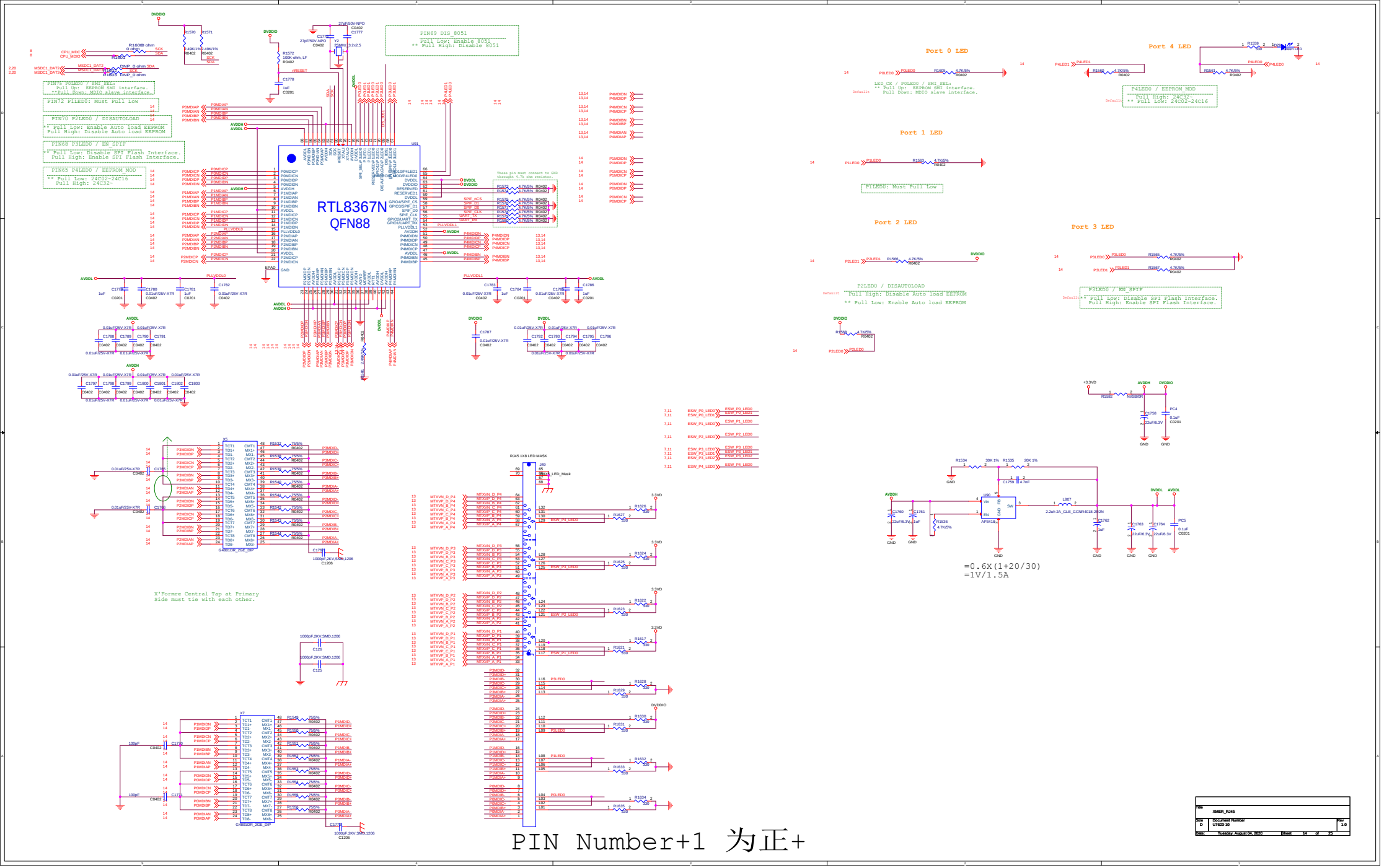
Title	Boot Strapping_Ethernet_LED	
Size: C	Document Number: U7623-10	Rev: 1.0
Date: Tuesday, August 04, 2020	Sheet 11 of 25	



Title	DDR3		
Size B	Document Number U7623-10		Rev 1.0
Date: Tuesday, August 04, 2020		Sheet 12 of 25	



Title	XMER_RJ45	
Size B	Document Number U7623-10	Rev 1.0
Date: Tuesday, August 04, 2020	Sheet 13 of 25	


RTL8367N
QFN88
PIN69 DIS_8051
Pull Low: Enable 8051
** Pull High: Disable 8051
PIN74 P0LED0 / SMI SEL:
Pull Up: EEPROM SMI interface.
Pull Down: MDIO slave interface.
PIN73 P1LED0: Must Pull Low
PIN70 P2LED0 / DISAUTOLOAD
** Pull Low: Enable Auto load EEPROM
Pull High: Disable Auto load EEPROM
PIN68 P3LED0 / EN_SPIF
** Pull Low: Disable SPI Flash Interface.
Pull High: Enable SPI Flash Interface.
PIN65 P4LED0 / EEPROM_MOD
** Pull Low: 24C02~24C16
Pull High: 24C32~
Port 0 LED
Port 1 LED
Port 2 LED
Port 3 LED
Port 4 LED
P4LED0 / EEPROM_MOD
Pull High: 24C32~
** Pull Low: 24C02~24C16
P3LED0 / EN_SPIF
** Pull Low: Disable SPI Flash Interface.
Pull High: Enable SPI Flash Interface.
P2LED0 / DISAUTOLOAD
Pull High: Disable Auto load EEPROM
** Pull Low: Enable Auto load EEPROM
P1LED0: Must Pull Low
LED_CK / P0LED0 / SMI_SEL:
** Pull Up: EEPROM SMI interface.
Pull Down: MDIO slave interface.
X'Formre Central Tap at Primary
Side must tie with each other.
RJ45 1X8 LED MASK
LED_Mask
=0.6X(1+20/30)
=1V/1.5A
PIN Number+1 为正+
XMER_RJ45
Document Number
U7623-30
Rev 1.0
Tuesday, August 04, 2020
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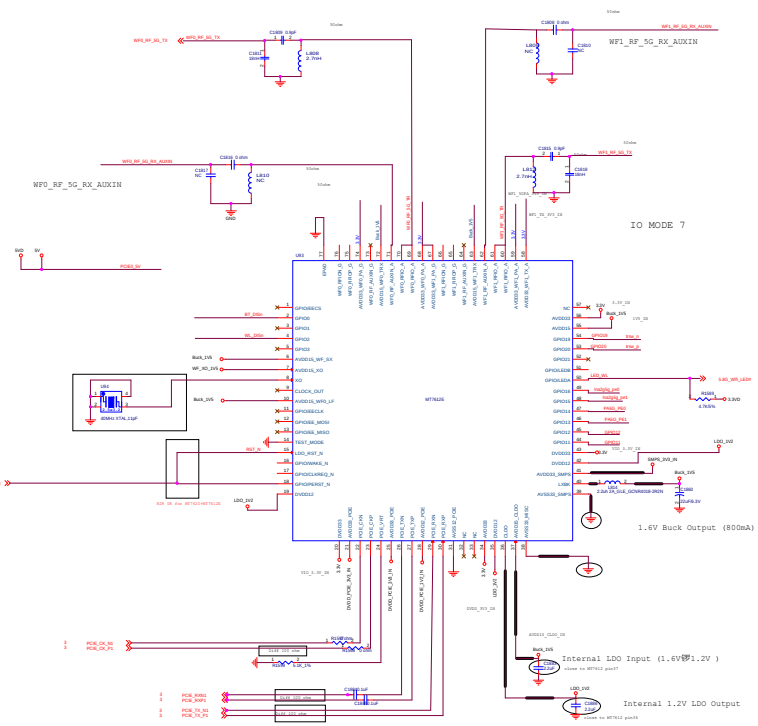
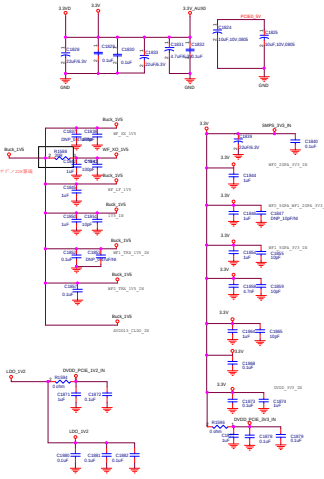
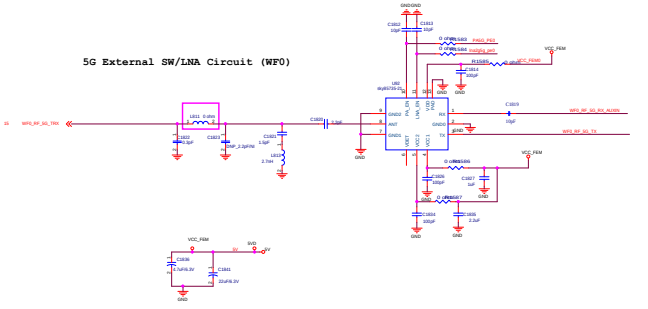
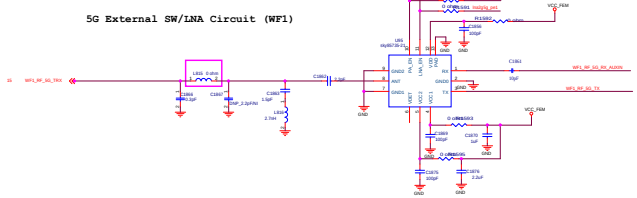
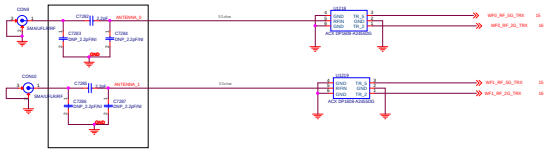

WF0_RF_5G_RX_AUXIN
WF1_RF_5G_RX_AUXIN
IO MODE 7
MT7622
1.6V Buck Output (800mA)
Internal LDO Input (1.6V or 1.2V)
Internal 1.2V LDO Output




5G External SW/LNA Circuit (WF0)


5G External SW/LNA Circuit (WF1)



0 : Normal Mode 1 : Test Mode	TEST_MODE R1606 1K

Normal Mode	Test Mode
0: EFUSE 1: EEPROM	ANTSEL6 R1607 1K
00 : 20MHz SMD 01 : 20MHz DIP 10 : 25MHz DIP 11 : 40MHz SMD	XTAL_SEL0 3V3 R1609 1K ANTSEL4 XTAL_SEL1 3V3 R1610 1K ANTSEL5
Co-clock mode 0 :Current mode 1 :Voltage mode	GPIO0 R1611 1K

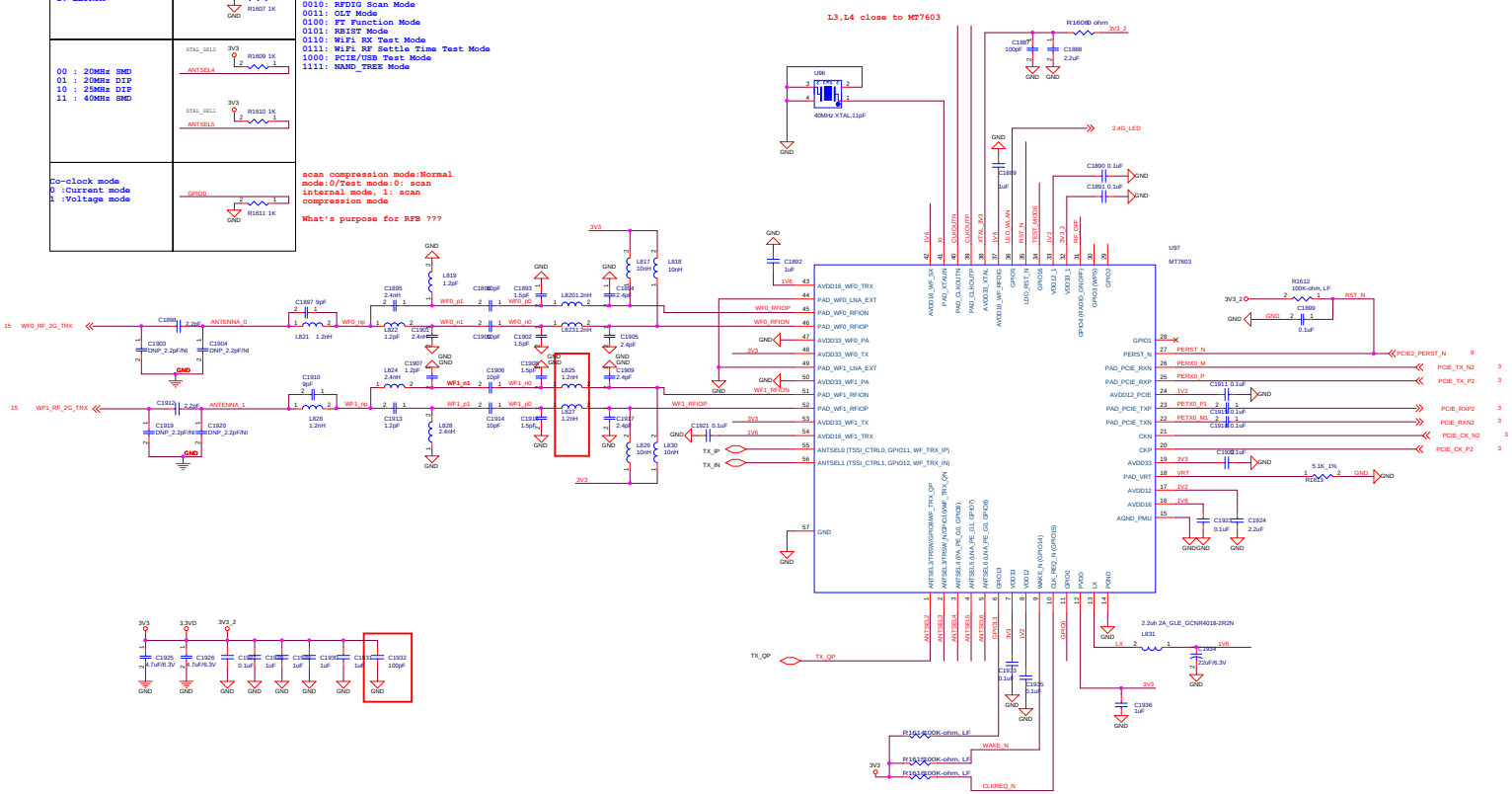
[ANTSE4, ANTSE5, ANTSE6, GPIO0]

0000: Power on Debug
0001: ATPG Mode
0010: RFDIG Scan Mode
0011: CLT Mode
0100: FT Function Mode
0101: RBIST Mode
0110: WiFi RX Test Mode
0111: WiFi RF Settle Time Test Mode
1000: PCIE/USB Test Mode
1111: NAND_TREE Mode

scan compression mode:Normal
mode:0/Test mode:0: scan
internal mode, 1: scan
compression mode

What's purpose for RFB ???

L3,L4 close to MT7603



Title	PCIE2 7603
Size: D	Document Number: U7625-10
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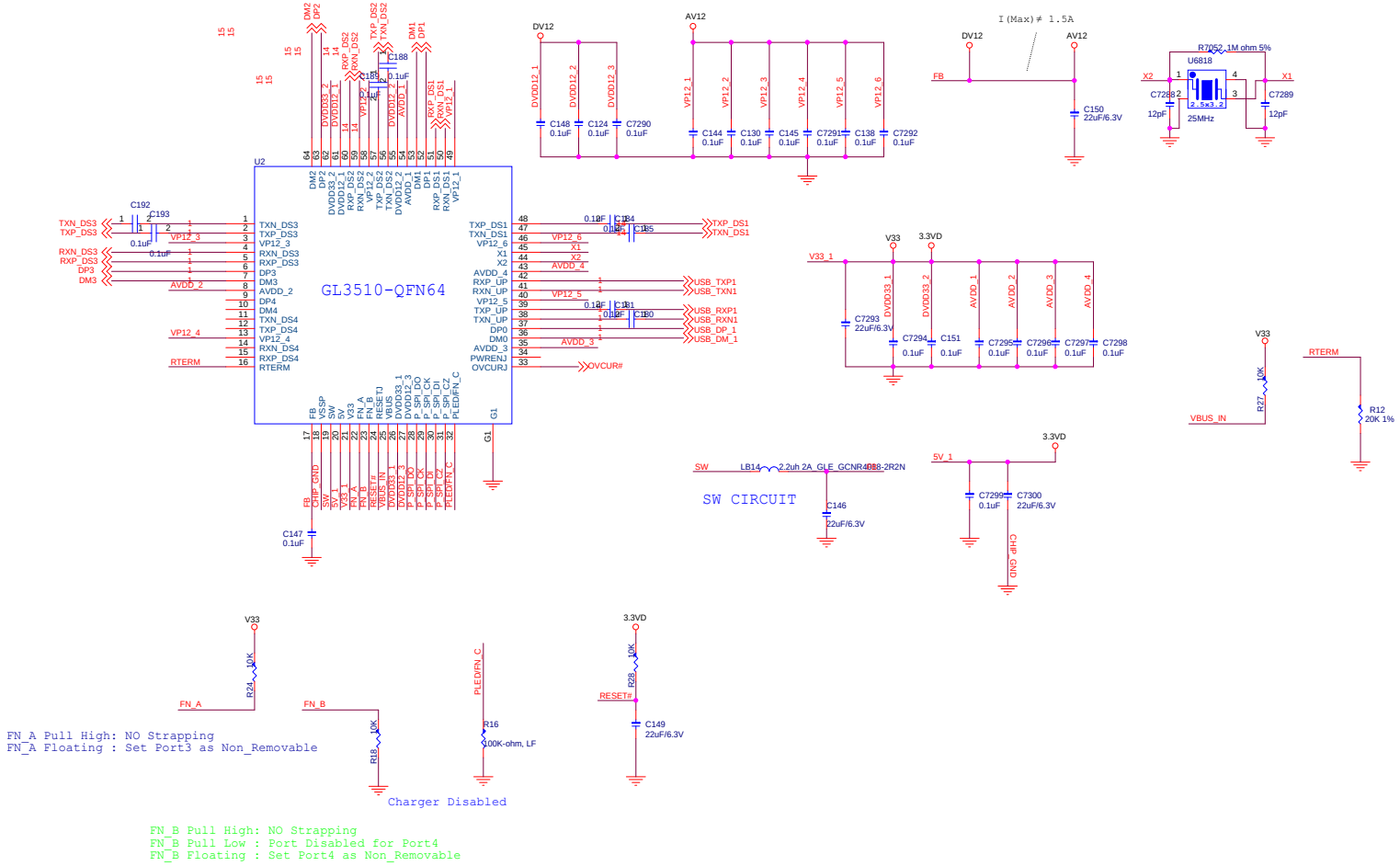
Date: Tuesday, August 04, 2020	Sheet 16 of 25



Title	PCIe HOST2_SATA3	
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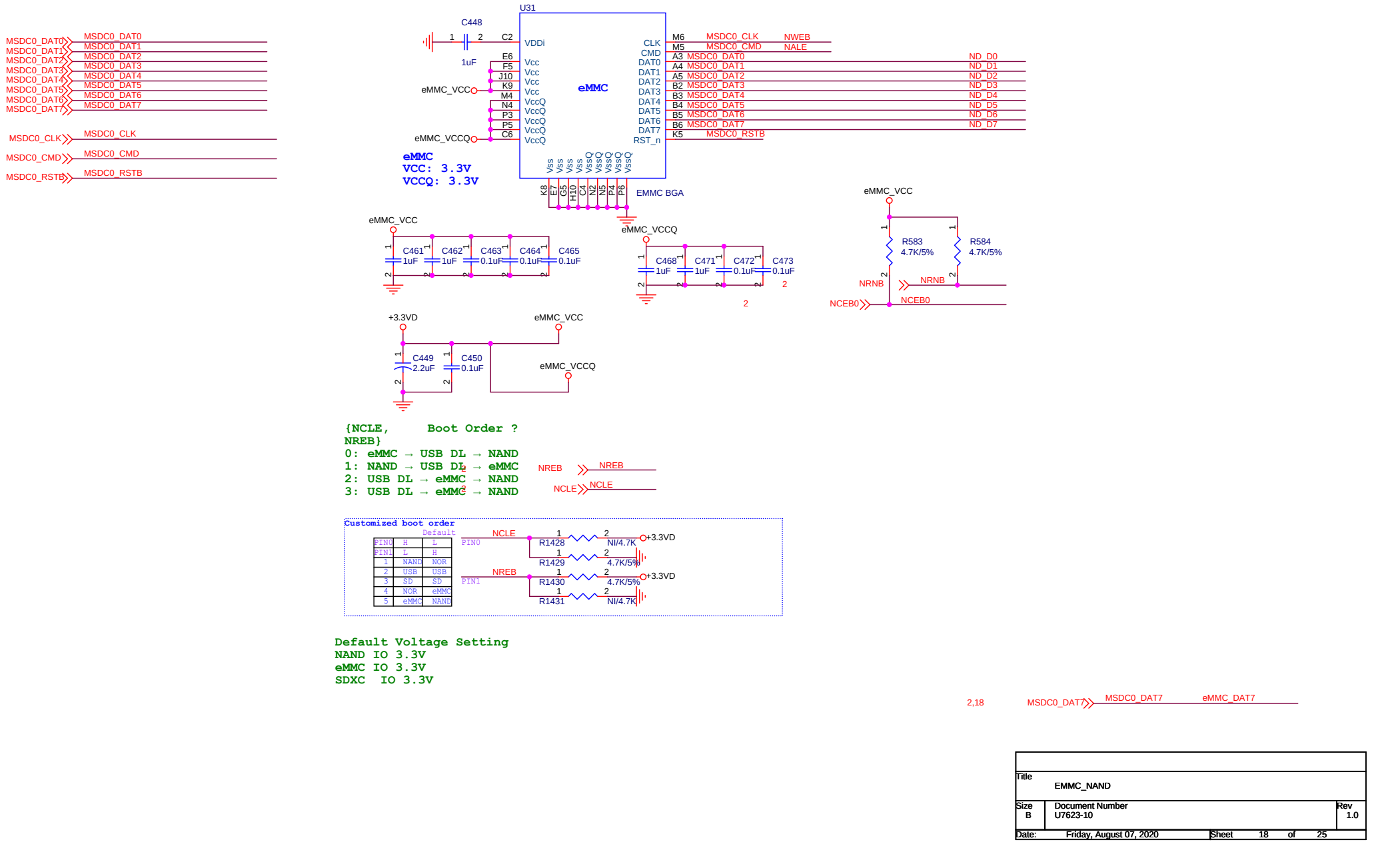
MSDC0 for SLC NAND or eMMC (Default eMMC)



PIN0	H	L
PIN1	L	H
1	NAND	NOR
2	USB	USB
3	SD	SD
4	NOR	eMMC
5	eMMC	NAND

Title	EMMC_NAND	
Size B	Document Number U7623-10	Rev 1.0
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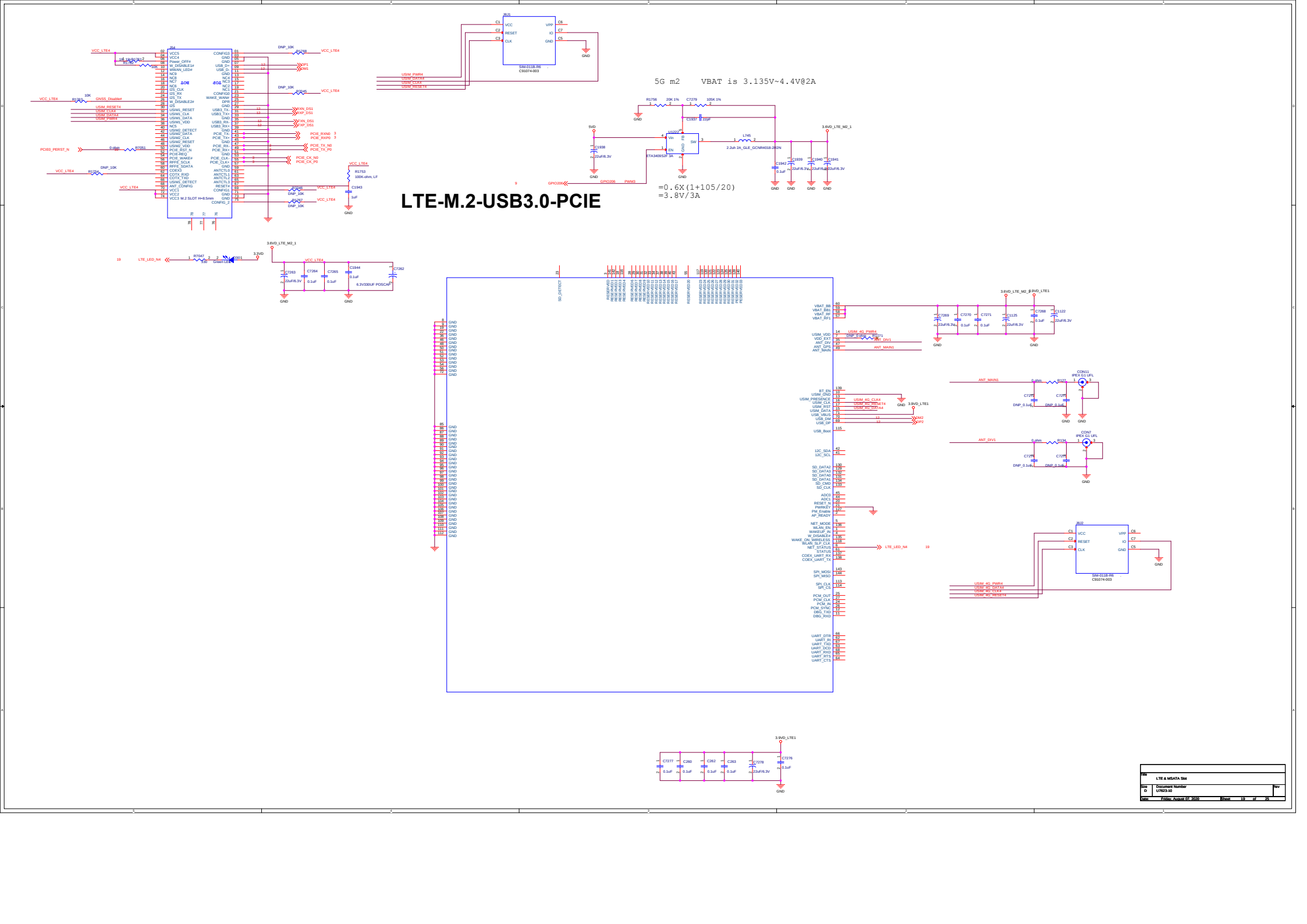
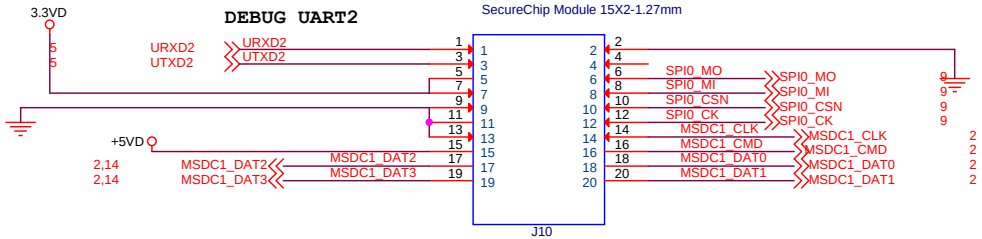
LTE-M.2-USB3.0-PCIE





I2C OR UART1 OR UART0

Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
MIPI_TDN0	N/A	GPI99	**O:TDN0**					
MIPI_TDP0	N/A	GPI100	**O:TDP0**					
MSDC1_CMD	78	GPIO105	**B0:MSDC1_CMD**		B1:SDA1			O:I2SOUT_BCK
MSDC1_CLK	79	GPIO106	**O:MSDC1_CLK**		B1:SCL1			O:I2SOUT_LRCK
MSDC1_DAT0	80	GPIO107	**B0:MSDC1_DAT0**				O:UTXD0	O:I2SOUT_DATA_OUT
MSDC1_DAT1	81	GPIO108	**B0:MSDC1_DAT1**		O:PWM0		I1:URXD0	O:PWM1
MSDC1_DAT2	82	GPIO109	**B0:MSDC1_DAT2**		B1:SDA2		O:UTXD1	O:PWM2
MSDC1_DAT3	83	GPIO110	**B0:MSDC1_DAT3**		B1:SCL2		I1:URXD1	O:PWM3

Title: MIPI_LCD		
Size: B	Document Number: U7623-10	Rev: 1.0
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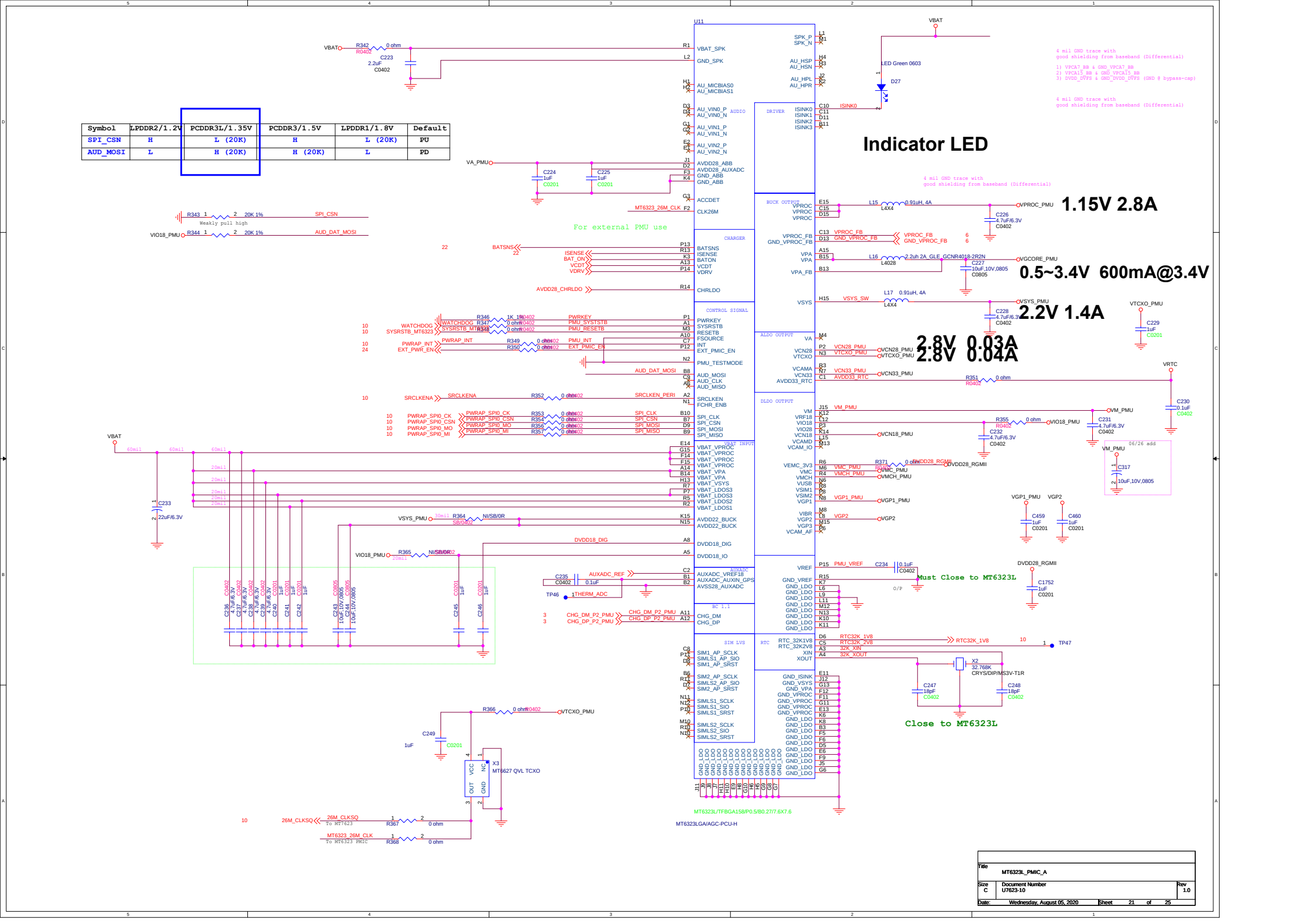
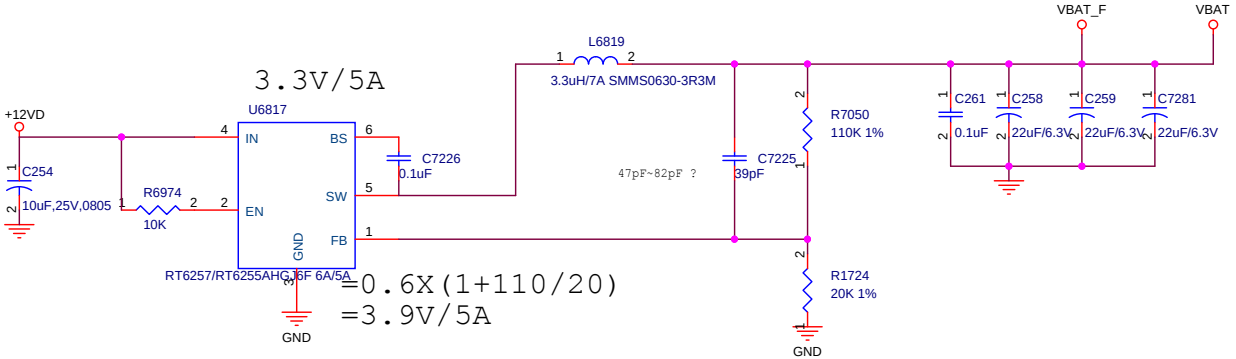
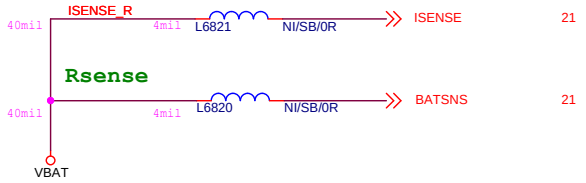


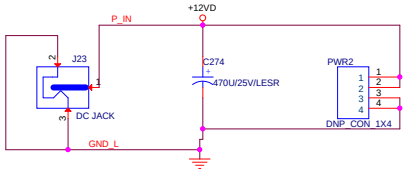
Symbol	LPDDR2/1.2V	PCDDR3L/1.35V	PCDDR3/1.5V	LPDDR1/1.8V	Default
SPI_CSN	H	L (20K)	H	L (20K)	PU
AUD_MOSI	L	H (20K)	H (20K)	L	PD

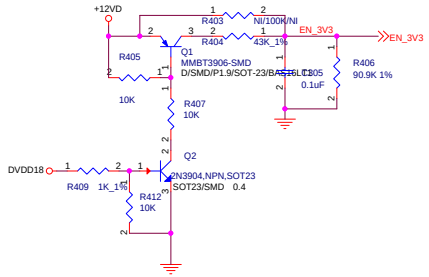


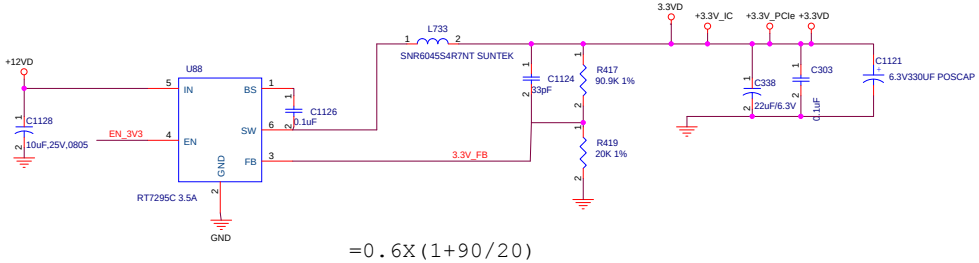
VBAT is battery voltage when DC remove.



Title: MT6323L_VBAT_IN_A		
Size: B	Document Number: U7623-10	Rev: 1.0
Date: Wednesday, August 05, 2020	Sheet 22 of 25	

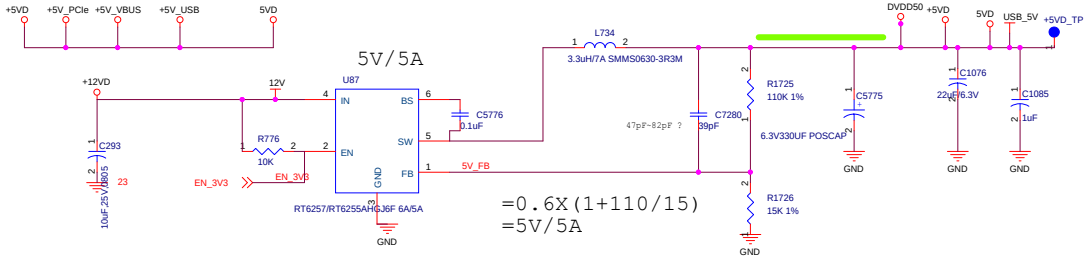






=0.6X(1+90/20)
=3.3V/3.5A

5A



=0.6X(1+110/15)
=5V/5A

Title	Power_3.3V_5V		
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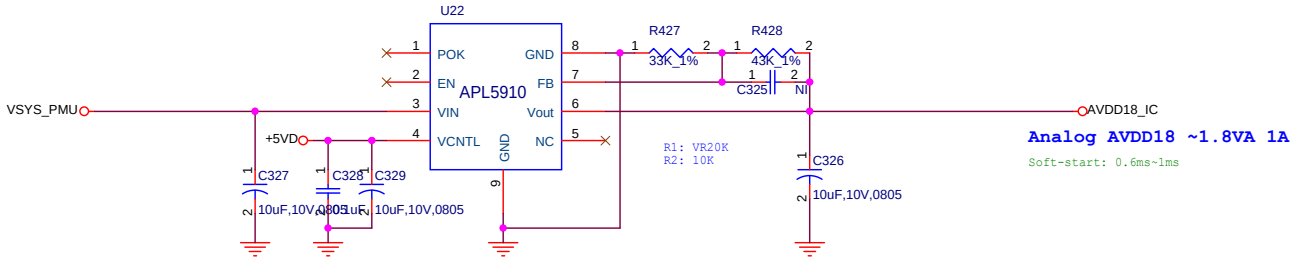
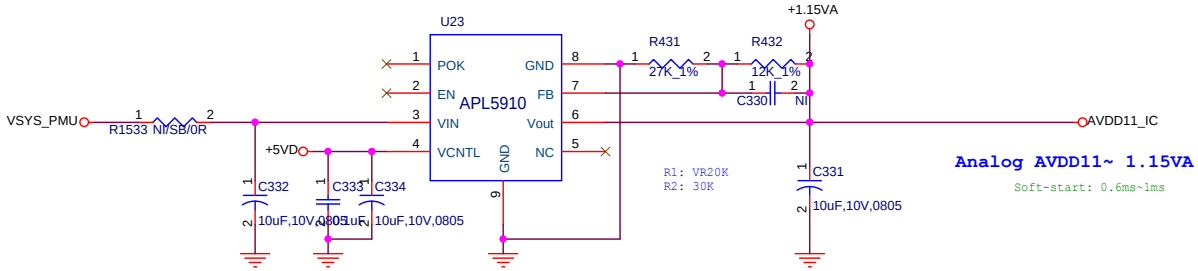
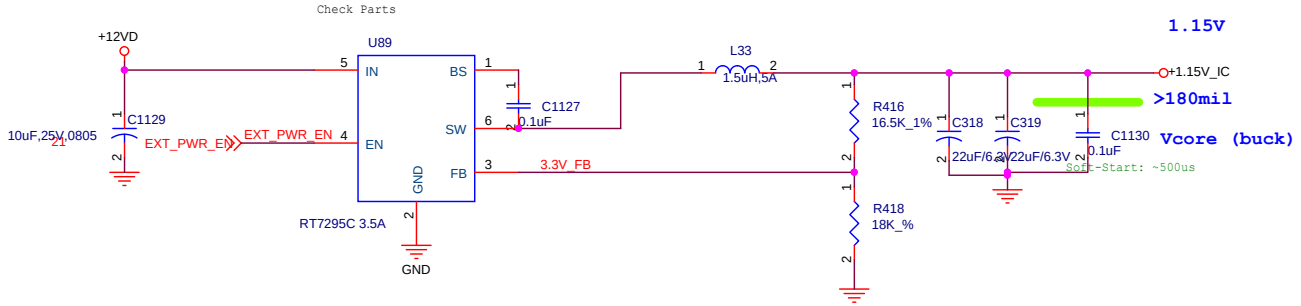




Vout=0.8(1+R1/R2)
1.15V R2:27K R1:12K
1.09V R2:33K R1:12K
1.20V R2:24K R1:12K



Vout=0.6*(1+R416/R418)
1.15V: 16.5K / 18K

Title: PWR_1.15VD_1.15VA_1.8VA		
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1.15V VPROC (CPU)

Always ON

120mil

BUCK VPROC_PMU — VPROC — VPROC

VPROC_PMUB G2156

C1390 10uF,10V,0805

3.3V Giga PHY

Always ON

+3.3V_IC — AVDD33_LD — AVDD33_LD

DVDD33_IO — DVDD33_IO

Reserved CAP

1.35V For DDR3L (DRAM+Controller)

Always ON

LDO

BUCK

VM_PMU — VDD_EMI — VDD_EMI

VEMI_PMUB G2156

default +3.3V_PCIe +3.3VD and +3.3VIC is megre

+3.3V_PCIe — DVDD28_MSDC1 — DVDD28_MSDC1

DVDD28_I2S — DVDD28_I2S

+3.3VD — L54 NI/SB/0R — AVDD33_USB — AVDD33_USB

L55 NI/SB/0R — AVDD33_USB_P2 — AVDD33_USB_P2

DVDD28_NOR — DVDD28_NOR (share w/ DVDD28_DPI)

R457 680 ohm

R457 is for AVDD33_USB and AVDD33_USB_P2 pin

PMIC MT6323L Power Management

VCN18_PMU — R1502 NI/SB/0R — AVDD18_WBG — AVDD18_WBG

VIO18_PMUB G2156

VIO18_PMU — R1506 NI/SB/0R — DVDD18

DVDD18_IO_DPI — DVDD18_IO_DPI

DVDD18_IO — DVDD18_IO

DVDD18_IO_MSDC0 — DVDD18_IO_MSDC0

DVDD18_IO_MSDC1 — DVDD18_IO_MSDC1

DVDD18_IO_NOR — DVDD18_IO_NOR

DVDD18

L50 NI/SB/0R — DVDD18_IO_RGMII — DVDD18_IO_RGMII

L52 NI/SB/0R — DVDD_GE1_IO — DVDD_GE1_IO

RGMII繁方継ミ

C264 4.7uF/6.3V C0402

C250 4.7uF/6.3V C0402

DVDD18_IO_I2S — DVDD18_IO_I2S

DVDD18_IO_WBCT — DVDD18_IO_WBCT

1.8V/3.3V

VMC_PMU — R1512 NI/0R — R0402 — DVDD28_MSDC0 — DVDD28_MSDC0

+3.3V_IC — R1514 0 ohm

Fix 3.3V

1.0V Giga Core

Always ON

VGCORE_PMU — L57 NI/SB/0R — DVDD_K_1 — DVDD_K_1

L58 NI/SB/0R — AVDD10_AFE — AVDD10_AFE

VGCORE_PMUB G2156

1.15V VCore

Always ON

AVDD11_IC — L64 NI/SB/0R — AVDD11_PCIE — AVDD11_PCIE

L65 NI/SB/0R — AVDD11_SSUSB — AVDD11_SSUSB

BUCK

+1.15V_IC — VCCK — VCCK

AVDD18 Group

Always ON

AVDD18_IC — L61 NI/SB/0R — AVDD18_PCIE — AVDD18_PCIE

L62 NI/SB/0R — AVDD18_USB — AVDD18_USB

L63 NI/SB/0R — AVDD18_SSUSB — AVDD18_SSUSB

L66 NI/SB/0R — AVDD18_MIPITX — AVDD18_MIPITX

Reserved CAP C1672 NI/0.1uF

AVDD18_IC — R1517 NI/SB/0R

AVDD18_AP must be to add 10 ohm and close MT7623 AVDD18_AP pin

L806 10 ohm — AVDD18_AP — AVDD18_AP

L70 NI/SB/0R — AVDD18_MEMPLL — AVDD18_MEMPLL

L72 NI/SB/0R — AVDD18_PLLGP — AVDD18_PLLGP

L73 NI/SB/0R — AVDD18_USB_P2 — AVDD18_USB_P2

R456 680 ohm

R456 is for AVDD18_USB_P2 and AVDD18_USB pin

Title: Power Connection		
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