everyday genius

MT7623A Datasheet

Version: Preliminary
Release date: 2015-11-12

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Overview

MT7623A is a highly integrated network router system-on-chip used for high wireless performance, home entertainment, home automation and so on.

Applications:
- Internet service router
- Wireless router
- Home security gateway
- Home automation
- NAS devices
- iNICs
- Switch control processor

MT7623 is fabricated with advanced silicon process and integrates a Quad-core ARM® Cortex-A7 MPCoreTM operating up to 1.3GHz and more DRAM bandwidth. This SoC also includes a variety of peripherals, including MIPI, RGMII, PCIe2.0, USB2.0 OTG ,USB3.0 ports, and 5-port GbE switch. To support popular network applications, MT7623A also implements 10/100/1000 Ethernet RGMII interface, embedded a 5-ports Giga switch and supports 802.11ac/n WLAN connection thru its PCIe port.

MT7623A includes two wireless connectivity functions, WLAN, Bluetooth. The RF parts of those two blocks are put in the MT6625L chip. With two advanced radio technologies integrated into one single chip, MT7623A/MT6625L provides the best and most convenient connectivity solution among the industry. MT7623A/MT6625L implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms.

Besides the connectivity features, the hardware-based NAT engine with QoS embedded in MT7623A transporting the audio/video streams in higher priority than other non-timely services also enriches the home entertainment application. The SFQ separating P2P sessions from audio/video ones so that MT7623A guarantees the streaming service.

With the advanced technology and abundant features, MT7623A is well positioned to be the core of next-generation Smart WiFi AP router, and home gateway systems.

Key Features

- Embedded Quad-core ARM® Cortex-A7 MPCore operating at 1.3GHz
  - 32KB L1 I-Cache and 32KB L1 D-Cache
  - 512KB unified L2 Cache
  - NEON/FPU
  - DVFS technology
- 32-bit LPDDR2 and DDR3/L
- NOR(SPI), NAND Flash(SLC/MLC), MSDC(4-bits), eMMC4.5
- USB3.0 Host x 2 (2nd port share w/ PCIe2.0)
- USB2.0 OTG x 1
- PCIe2.0 Host x 3 (3rd port share w/ USB3.0)
- SPI, I2C, UART Lite, JTAG, MDC, MDIO, GPIO, PWM, ADC
- VoIP support (I2S, PCM)
- Audio interface (I2S, PCM)
- MIPI(2-lane)
- Deliver the super Samba performance via USB2.0/USB3.0/SD-XC
- One RGMII/MII interface
- Gigabit Switch
  - 5 ports with full-line rate
  - 5-port 10/100/1000Mbps MDI transceivers
- HW storage accelerator
  - HW NAT
  - 2Gbps wired speed
  - L2 bridge
  - IPv4 routing, NAT, NAPT
  - IPv6 routing, DS-Lite, 6RD, 6to4
- HW QoS
  - 16 hardware queues to guarantee the min/max bandwidth of each flow.
  - Seamlessly co-work with HW NAT engine.
  - 2Gbps wired speed.
  - SFQ w/ 1k queues.
- HW Crypto Engine
  - Deliver 1 Gbps IPSec throughput
  - AES/3DES, MD5/SHA1/SHA2
- Green
  - Intelligent Clock Scaling (exclusive)
  - DDR: ODT off, Self-refresh mode
- Software: Linux 3.10.20 SDK, OpenWRT

Functional Block Diagram

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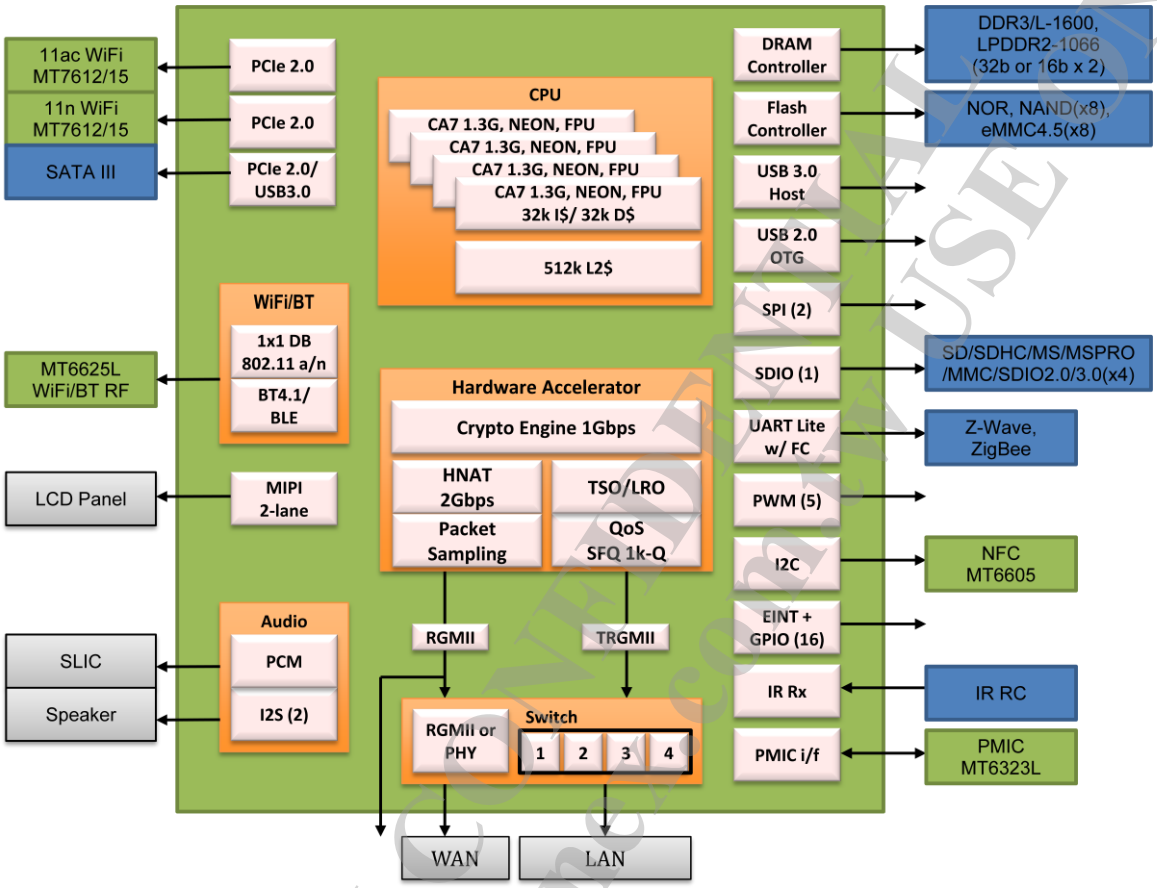

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Document Revision History

Revision	Date	Author	Description
Preliminary	2014-12-26	Ken Wu	Initial Release
	2015-5-15	Leon Chung	Change pin name of Serial Flash Interface
	2015-6-15	Leon Chung	1. Section 2.2, add Reset Aux and Pull columns into pin description table 2. Section 2.3.1, add EINT(External INT) column into pin share scheme table 3. Add new sections 2.3.2 and 2.3.3
	2015-6-22	Leon Chung	1. Section 2.2, add IO reset state.
	2015-7-6	Leon Chung	1. Section 3.6, add amplitude value.
	2015-8-27	Yushu Xiao	1. Section 3.8, update power on sequence
	2015-9-15	Ken Wu Chungfa	1. Section 3.2, revised VCCK voltage range 2. Section 3.3, add case temperature
	2015-10-28	Yushu Xiao	1. Section 2.4, revised boot download mode value
	2015-11-12	Leon Chung	1. Section 4.3, add “ARM” word in top marking.

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Table of Contents

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Lists of Tables and Figures

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1 General Features

1.1 Platform Features

- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A7 MPCoreTM operating at 1.3 GHz
  - NEON processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 1.05V to 1.31V
- **CONN MCU subsystem**
  - Andes N9 processor with 32KB I-cache, 16KB D-cache
- **External memory interface**
  - Supports LPDDR2, DDR3/L
  - 32-bit data bus width
  - Memory clock up to 533MHz(LPDDR2) and 800MHz(DDR3/L)
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
- **Security**
  - ARM® TrustZone® Security
  - Security boot
  - Crypto engine(IPSEC/ DES/ 3DES/ AES/ ARC4/ MD5/ SHA1/ SHA2/ GHASH/ CRC32/ PRNG)
- **Connectivity**
  - 3 PCIe2.0 (3rd port is shared w/ USB3.0)
  - 2 USB3.0 (2nd port is shared w/ PCI2.0)
  - USB2.0 high-speed dual mode supporting 8 Tx and 8 Rx endpoints
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - UART for external devices and debugging interfaces
  - SPI master for external devices
  - I2C to control peripheral devices,
  - I2S master output and master/slave input for connection with optional external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controller supporting(SD/ SDHC/ MS/ MSPRO/ MMC and SDIO2.0/3.0 protocols)
  - IR Rx
- **Operating conditions**
  - Core voltage: 1.15V
  - Processor DVFS+SRAM voltage : 1.05V~1.31V (Typ. 1.15V; Sleep mode 0.85V)
  - I/O voltage: 1.8V/3.3V
  - Memory: 1.2V/1.35V/1.5V
  - NAND: 1.8V/3.3V
  - Clock source: 25MHz, 26MHz, 32.768kHz
- **Package**
  - FBGA 21x21mm 486 balls
  - Ball pitch: 0.8mm

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1.2 BT/WLAN with MT6625L Features

- **Common**
  - Self calibration
  - Single TCXO and TSX for BT and WLAN
  - Best-in-class current consumption performance
  - OS supported: Android
  - Intelligent BT/WLAN coexistence scheme
  - Single antenna support for WLAN/Bluetooth

- **WLAN**
  - Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w Protected Managed Frames
  - Supports WiFi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated PA with max 21dBm output power
  - Typical -77.5 dBm 2.4GHz receiver sensitivity at 11g 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 10dBm (class 1) transmit power and Balun
  - Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet loss concealment (PLC) function for better voice quality
  - Low-power scan function to reduce the power consumption in scan modes

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, WBT diplexer.
  - Fully integrated in one IPD die
  - Supports single and dual antenna operation.

1.3 Switch Features

MT7623A switch is a highly integrated Ethernet switch with high performance and non-blocking transmission. It includes a 5-port Gigabit Ethernet MAC and a 5-port Gigabit Ethernet PHY for Dumb and Smart Switch applications. MT7623A enables an advanced power-saving feature to meet the market requirement. It complies with IEEE803.3az for Energy Efficient Ethernet and cable-length/link-down power saving mode. MediaTek's industry-leading techniques provide customers with the most cost-competitive and lowest power consumption Ethernet product in the industry.

- 5-port 10/100/1000Mbps MDI transceivers
- Accessible MAC address table with 2048 entries and auto aging and learning capabilities

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- Programmable aging timer for MAC address table
- Supports programmable 1518/1536/1552 and 9K Jumbo frame length (Jumbo frame can't working with HNAT and HQoS)
- Supports SVL and IVL with 8 filtering database
- Supports RSTP and MSTP
- Supports 802.1X
- Supports 4K VLAN entries
- Supports VLAN ID tag and un-tag options for each port
- Supports double tagging VLAN
- Supports hardware port isolation
- Supports 8 priority queues per port
- Supports SP, WFQ, and SP+WFQ latency scheduler
- Supports Max-Min bandwidth scheduler
- Supports ingress and egress rate control
- Supports 64 sets of ACL rules
- Supports IPv4 and IPv6 multicast frames hardware forwarding
- Supports 40 MIB counters per port
- Supports Loop detection indicator
- Supports Broadcast/Multicast/Unknown frames storm suppression
- 10Base-T, 10Base-Te, 100Base-TX, and 1000Base-T compliant Transceivers
- Compliant with IEEE 802.3 Auto-Negotiation
- Supports 1 LED per GEPHY port
- Supports short-cable power saving
- Integrated MDI resistors
- Supports IEEE 802.3az Energy Efficient Ethernet

1.4 Main Features Summary

The following table covers the main features offered by MT7623A. Overall, the MT7623A supports the requirements of a high-level AP/router, and a number of interfaces together with a large maximum RAM capacity.

Table 1-1 Main Features

Features	MT7623A
CPU	ARM CA7 (1.3GHz, Quad-core), NEON
I-Cache, D-Cache	32kB, 32kB per core
L2 Cache	512KB
HNAT/HQoS	HQoS 16 queues, SFQ 1k queues HNAT 2Gbps forwarding (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4)
DRAM data	32bit

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Features	MT7623A
LPDDR2	1066 Mbps (max 8Gb)
DDR3/L	1600 Mbps (max 16Gb)
SD eMMC	SD-XC class 10 (4bits, max 128GByte) eMMC4.5 (max 128GByte)
NAND (SLC type)	ONFI2.0 (8bits, max 60b ECC) Small page 512-Byte (max 512Mbit) Large page 2k-Byte (max 2GB) Note that pin sharing w/ eMMC4.5.
SPI Flash (NOR)	1 (max 50MHz) 3B addr mode (max 128Mbit) 4B add. mode (max 512Mbit) The 2nd chip select is by pin sharing.
MIPI	2-Lane
PCIe	PCIe2.0 x 3 (3rd port pin sharing w/ USB3.0)
USB	USB2.0 OTG x 1 (w/ BC 1.2) USB3.0 x 2 (2nd port pin sharing w/ PCIe2.0)
Ethernet	5-port GSW + RGMII x 1
I2S	2 (max 192k sample rate, 24bits)
PCM	1 (4 ch)
I2C	1 (Max 400kHz) The other two I2C are by pin sharing.
SPI	2
UART Lite	1 The other three UART Lite are by pin sharing
IR RX	1
JTAG	1
Package	FBGA 21 x 21 mm

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2 Pins

2.1 Ball Map (Top View)

Table 2-1 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	MSDC0_DAT7	MSDC0_DAT1	MSDC0_DAT4		NREB		SFLASH_IO_3		AVDD33_USB_P2		AVDD18_USB_P2
B	MSDC0_CLK	MSDC0_DAT2	MSDC0_DAT6	MSDC0_DAT0		NRNB		SFLASH_IO_0		USB_VRT_P2		USB_DM_P2
C			GND	MSDC0_DAT5	MSDC0_RSTB	NCEB1	NCLE	SFLASH_CLK	SFLASH_CS_L	USB_VBUS_P2	CHG_DP_P2	USB_DP_P2
D	RDQ31	RDQ29	RDQ25	RDQ27	MSDC0_CMD	MSDC0_DAT3	NCEB0	SFLASH_IO_2	SFLASH_IO_1	PWRAP_SPI0_MO	CHG_DM_P2	AVSS_USB_P2
E	RDQ18	RDQ16	GND	RDQM2	RDQM3	SPI0_MI	SPI0_CSN		DVDD28_NOR		PWRAP_INT	PWRAP_SPI0_CSN
F			RDQ20	RDQ22	RDQS3	RDQS3_	SPI0_CK		DVDD28_DPI		PWRAP_SPI0_MI	
G	RDQ17	RDQ19	RDQ21	RDQ23			SPI0_MO		DVDD28_MSDC0		PWRAP_SPI0_CSN2	
H	RDQ30	RDQ28	GND	RDQS2	RDQS2_	GND					PWRAP_SPI0_CK2	PWRAP_SPI0_CK
J			RDQ24	RDQ26	RCLK1	RCLK1_	VDD_EMI	GND	VCCK	VCCK	VCCK	GND
K	RRAS	DDR3RSTB	RBA2	RCS1		GND	VDD_EMI	AVDD18_MEMPLL	AVSS18_MEMPLL	VCCK	GND	VCCK_VPROC
L	RCS0	RCAS	GND	RA2	RA15	GND	VDD_EMI	TP_MEMPLL	VCCK	VCCK	GND	VCCK_VPROC
M			RA9	RWE	RBA0	GND	VDD_EMI	GND	VCCK	GND	GND	VCCK_VPROC
N	RA3	RA0	RA5	RA13		GND	VDD_EMI	VCCK	GND	GND	GND	GND
P	RA4	RBA1	GND	RA11	RA12	RA7	VDD_EMI	GND	VCCK	GND	GND	GND
R			RA6	RA1	RCLK0_	RCLK0	VDD_EMI	VCCK	GND	GND	GND	GND
T	RCKE	RA10	RA14	RA8			VREF0	VCCK	GND	GND	GND	VCCK
U	RDQ9	RDQ11	RDQM1	GND	GND			VCCK			VCCK	VCCK
V			RDQ15	RDQ13	RDQS0	RDQS0_	VCCK	VCCK		DVDD28_I2S		
W	RDQ4	RDQ6	RDQ2	RDQ0	RDQS1_	RDQS1			DVDD28_MSDC1			USB_DM1
Y	RDQ5	RDQ7	GND	RDQM0				AVDD11_PCIE_P0		AVDD33_USB	USB_DM0	USB_DP1
AA			RDQ1	RDQ3		PCIE_VRT_P0	AVSS_PCIE	AVDD11_PCIE_P1			USB_DP0	AVDD18_SSUSB
AB	RDQ8	RDQ10	RDQ14	RDQ12	DVDD18_IO_MSDC1	PCIE_CKN0	PCIE_TXN1		PCIE_CKP1	PCIE_VRT_P1	AVSS_SSUSB	USB_RXN0
AC	MSDC1_DAT1	REXTDN	MSDC1_DAT2	MSDC1_DAT3	DVDD18_IO	PCIE_CKP0	PCIE_TXP1	AVSS_PCIE	PCIE_CKN1	PCIE_CKP2	SSUSB_VRT_P0	USB_RXP0
AD	MSDC1_INS	MSDC1_CMD	MSDC1_CLK	PCIE_TXP0	DVDD18_IO_I2S	PCIE_RXP0		PCIE_RXP1		PCIE_CKN2	USB_TXN0	
AE	GND	MSDC1_DAT0	FSOURCE_P0	PCIE_TXN0	AVDD18_PCIE	PCIE_RXN0		PCIE_RXN1		AVDD18_USB	USB_TXP0	
	1	2	3	4	5	6	7	8	9	10	11	12

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13	14	15	16	17	18	19	20	21	22	23	24	25	
RTC32K_CK		GPIO250		26M_CLKSQ		AVSS18_AP	REFP		G2_RXD2	G2_TXEN	G2_TXD0	GND	A
SRCLKENAI		GPIO251		GPIO256		AVDD18_AP	AUX_IN1		G2_RXD1	G2_RXCLK	GND	G2_TXD1	B
SRCLKENA	SYSRSTB	GPIO257	GPIO252	GPIO255	PCM_TX	PCM_CLK	AUX_IN5	G2_RXDV	G2_RXD3	G2_TXCLK	G2_TXD2	G2_TXD3	C
	WATCHDOG	IR	GPIO254	GPIO253	PCM_RX	PCM_SYNC	AUX_IN0	G2_RXD0	G2_MDIO	G2_MDC			D
		EINT7		GPIO15	GPIO14	SPI1_CK	AUX_IN2	SCL-ETH	ESW_P2_LED0	ESW_P0_LED1	ESW_XO	ESW_XI	E
DVDD18_IO_MSDC0		EINT5		GPIO123		SPI1_MI	AUX_IN4	AUX_IN3	ESW_P1_LED0	ESW_P0_LED0			F
DVDD18_IO_NOR		EINT4		GPIO125	URTS2	SPI1_CSN	SPI1_MO	JTMS	ESW_P3_LED1	ESW_P4_LED0	ESW_P3_LED0	ESW_P3_LED2	G
DVDD18_IO_DPI		EINT0	EINT2	GPIO122	GPIO124	UCTS2	JTAG_RESET	JTDO	JTDI	GND	ESW_TXVP_D_P4	ESW_TXVN_D_P4	H
GND	VCCK	EINT6	EINT1				JTCK	TESTMODE	ESW_TXVN_C_P4	ESW_TXVP_C_P4			J
VCCK_VPROC	VCCK_VPROC	EINT3	VCCK_VPROC		URXD2	SDA0	SCL0	A_POR_BPS	ESW_TXVN_B_P4	ESW_TXVP_B_P4	ESW_TXVP_A_P4	ESW_TXVN_A_P4	K
VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	GND	GND	UTXD2				ESW_TXVN_D_P3	ESW_TXVP_D_P3			L
VCCK_VPROC	VCCK_VPROC	GND		GND	AVDD18_PLLGP	AVSS18_PLLGP	GND	DVDD33_IO	ESW_TXVN_C_P3	ESW_TXVP_C_P3	ESW_TXVP_B_P3	ESW_TXVN_B_P3	M
GND	GND	GND	GND		GND	GND	DVDD33_IO	GND	ESW_TXVN_A_P3	ESW_TXVP_A_P3			N
GND	VCCK	GND		AVSS33_VBG	DVDD_K_1	AVDD10_AFE_P4	GND	AVDD10_AFE_P3	ESW_TXVN_D_P2	ESW_TXVP_D_P2	ESW_TXVP_C_P2	ESW_TXVN_C_P2	P
VCCK	VCCK	GND	DVDD18_IO_RGMII	DVDD_K_1	DVDD_K_1	AVDD10_AFE_P0	AVDD10_AFE_P1	AVDD10_AFE_P2	ESW_TXVN_B_P2	ESW_TXVP_B_P2			R
		GND		DVDD_GE1_VREF	DVDD_GE1_IO				ESW_TXVN_A_P2	ESW_TXVP_A_P2	ESW_TXVP_D_P1	ESW_TXVN_D_P1	T
				DVDD_GE1_IO					ESW_TXVN_C_P1	ESW_TXVP_C_P1			U
	DSI_TE	AUD_EXT_CK2	LCM_RST	I2S1_BCK	AVDD33_LD_P2	AVDD33_LD_P3	AVDD33_LD_P1	AVDD33_PLL_1	ESW_TXVN_B_P1	ESW_TXVP_B_P1	ESW_TXVP_A_P1	ESW_TXVN_A_P1	V
AVDD11_SSUSBP0	AUD_EXT_CK1			I2S1_LRCK	AVDD33_LD_P0	AVDD33_LD_P4	ESW_REXT	ESW_TANA	ESW_TXVN_D_P0	ESW_TXVP_D_P0			W
		PWM4	PWM1	I2S1_DATA_IN	I2S1_DATA	I2S0_BCK	I2S0_LRCK	WB_RSTB	ESW_TXVN_C_P0	ESW_TXVP_C_P0	ESW_TXVP_B_P0	ESW_TXVN_B_P0	Y
		PWM2	PWM0	PWM3	I2S1_MCLK	I2S0_MCLK	I2S0_DATA_IN	GPIO61	ESW_TXVN_A_P0	ESW_TXVP_A_P0			AA
DVSS18_MIPITX	MIPI_TCN	MIPI_TDN0	AVSS_SSUSB	USB_RXN1	I2S0_DATA	WB_CRTL2	WB_CRTL0	WB_SDATA	GPIO62	AVSS18_WBG	WB_SEN	XIN_WBG	AB
	MIPI_TCP	MIPI_TDP0	AVDD11_SSUSB_P1	USB_RXP1	SSUSB_VRT_P1	WB_CRTL3	WB_CRTL1	TEST_GQP	TEST_GQN	WB_SCLK	TEST_GIN	TEST_GIP	AC
MIPI_VRT		MIPI_TDP1	USB_TXN1		AVDD18_WBG	WB_CRTL4		WB_RXIN	WB_RXQN	AVSS18_WBG	WB_TXQP	WB_TXQN	AD
DVDD18_MIPITX		MIPI_TDN1	USB_TXP1		DVDD18_IO_WBCT	WB_CRTL5		WB_RXIP	WB_RXQP	WB_TXIP	WB_TXIN	AVSS18_WBG	AE
13	14	15	16	17	18	19	20	21	22	23	24	25	

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2.2 Pin Descriptions

Table 2-2 Pin Description

Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
GPIO								
E18	GPIO14	I	0	PD	PU/PD	3.3	4/8/12/16	GPIO14
E17	GPIO15	I	0	PD	PU/PD	3.3	4/8/12/16	GPIO15
H17	GPIO122	I	1	-	PD	1.8	5v open-drain	GPIO122
F17	GPIO123	I	1	-	PD	1.8	5v open-drain	GPIO123
H18	GPIO124	I	1	-	PD	1.8	5v open-drain	GPIO124
G17	GPIO125	I	1	-	PD	1.8	5v open-drain	GPIO125
C15	GPIO257	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO257
B17	GPIO256	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO256
C17	GPIO255	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO255
D16	GPIO254	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO254
D17	GPIO253	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO253
C16	GPIO252	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO252
B15	GPIO251	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO251
A15	GPIO250	I	1	PU	PU/PD	1.8	2/4/6/8/10/12/14/16	GPIO250
AB22	GPIO62	I	1	PD	PU/PD	1.8	2/4/6/8	GPIO62
AA21	GPIO61	I	1	PD	PU/PD	1.8	2/4/6/8	GPIO61
EINT								
H15	EINT0	OL	2	PD	PU/PD	3.3	4/8/12/16	External interrupt input0
J16	EINT1	OL	2	PD	PU/PD	3.3	4/8/12/16	External interrupt input1
H16	EINT2	OL	2	PD	PU/PD	3.3	4/8/12/16	External interrupt input2
K15	EINT3	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input3
G15	EINT4	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input4
F15	EINT5	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input5
J15	EINT6	I	0	PD	PU/PD	3.3	4/8/12/16	External interrupt input6
E15	EINT7	OL	6	PD	PU/PD	3.3	4/8/12/16	External interrupt input7
UART								
L18	UTXD2	I	0	PD	PU/PD	3.3	4/8/12/16	UART TX data
K18	URXD2	I	0	PD	PU/PD	3.3	4/8/12/16	UART RX data
H19	UCTS2	I	0	PD	PU/PD	3.3	4/8/12/16	UART clear to send
G18	URTS2	I	0	PD	PU/PD	3.3	4/8/12/16	UART request to send
JTAG								
H21	JTDO	OL	1	PU	PU/PD	1.8	2/4/6/8	JTAG data output
H22	JTDI	I	1	PU	PU/PD	1.8	2/4/6/8	JTAG data input
G21	JTMS	I	1	PU	PU/PD	1.8	2/4/6/8	JTAG mode select

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		State *1	Aux *2	Pull				
J20	JTCK	I	1	PU	PU/PD	1.8	2/4/6/8	JTAG clock
H20	JTAG_RESET	I	0	PU	PU/PD	1.8	2/4/6/8	JTAG target reset
I2C								
K20	SCL0	I	1	-	PD	1.8	5v open-drain	I2C clock
K19	SDA0	I	1	-	PD	1.8	5v open-drain	I2C data
SPI								
F7	SPI0_CK	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 clock
E7	SPI0_CSN	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 chip select
E6	SPI0_MI	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 data in
G7	SPI0_MO	I	0	PD	PU/PD	3.3	4/8/12/16	SPI port0 data out
E19	SPI1_CK	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 clock
G19	SPI1_CSN	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 chip select
F19	SPI1_MI	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 data in
G20	SPI1_MO	I	0	PD	PU/PD	1.8	2/4/6/8	SPI port1 data out
PWM								
AA16	PWM0	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
Y16	PWM1	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
AA15	PWM2	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
AA17	PWM3	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
Y15	PWM4	I	0	PD	PU/PD	3.3	4/8/12/16	Pulse width modulator
SFlash								
C8	SFLASH_CLK	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash clock
C9	SFLASH_CS_L	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash chip select
B8	SFLASH_IO_0	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #0
D9	SFLASH_IO_1	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #1
D8	SFLASH_IO_2	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #2
A8	SFLASH_IO_3	I	0	PD	PU/PD	3.3	4/8/12/16	Serial flash data bit #3
NAND								
D7	NCEB0	I	0	PU	PU/PD	3.3	4/8/12/16	NAND flash chip select0
C6	NCEB1	I	0	PU	PU/PD	3.3	4/8/12/16	NAND flash chip select1
A6	NREB	I	0	PD	PU/PD	3.3	4/8/12/16	NAND flash read enable
C7	NCLE	I	0	PD	PU/PD	3.3	4/8/12/16	NAND flash command latch enable
B6	NRNB	I	0	PU	PU/PD	3.3	4/8/12/16	NAND flash ready/busy
MSDC								
B1	MSDC0_CLK	OL	1	PD	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 clock (eMMC4.5)
D5	MSDC0_CMD	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 command (eMMC4.5)
B4	MSDC0_DAT0	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #0 (eMMC4.5)
A3	MSDC0_DAT1	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #1 (eMMC4.5)

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		State *1	Aux *2	Pull				
B2	MSDC0_DAT2	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #2 (eMMC4.5)
D6	MSDC0_DAT3	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #3 (eMMC4.5)
A4	MSDC0_DAT4	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #4 (eMMC4.5)
C4	MSDC0_DAT5	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #5 (eMMC4.5)
B3	MSDC0_DAT6	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #6 (eMMC4.5)
A2	MSDC0_DAT7	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 data bit #7 (eMMC4.5)
C5	MSDC0_RSTB	OH	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port0 reset output (eMMC4.5)
AD3	MSDC1_CLK	OL	1	PD	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 clock
AD2	MSDC1_CMD	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 command
AD1	MSDC1_INS	I	0	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 card insert
AE2	MSDC1_DAT0	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #0
AC1	MSDC1_DAT1	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #1
AC3	MSDC1_DAT2	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #2
AC4	MSDC1_DAT3	I	1	PU	PU/PD	3.3	2/4/6/8/10/12/14/16	MSDC port1 data bit #3
RGMII								
B23	G2_RXCLK	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX clock
C21	G2_RXDV	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data valid
D21	G2_RXD0	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #0
B22	G2_RXD1	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #1
A22	G2_RXD2	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #2
C22	G2_RXD3	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 RX data bit #3
C23	G2_TXCLK	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX clock
A23	G2_TXEN	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data valid
A24	G2_TXD0	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #0
B25	G2_TXD1	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #1
C24	G2_TXD2	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #2
C25	GE2_TXD3	I	0	PD	PU/PD	3.3	4/8/12/16	RGMII2 TX data bit #3
PHY Mgn.								
D23	G2_MDC	I	0	PD	PU/PD	3.3	4/8/12/16	PHY management clock
D22	G2_MDIO	I	0	PD	PU/PD	3.3	4/8/12/16	PHY management data
GSW								
F23	ESW_P0_LED0	O				3.3		Port #0 PHY LED indicators
E23	ESW_P0_LED1	O				3.3		Port #0 PHY LED indicators
F22	ESW_P1_LED0	O				3.3		Port #1 PHY LED indicators
E22	ESW_P2_LED0	O				3.3		Port #2 PHY LED indicators
G24	ESW_P3_LED0	O				3.3		Port #3 PHY LED indicators
G22	ESW_P3_LED1	O				3.3		Port #3 PHY LED indicators
G25	ESW_P3_LED2	O				3.3		Port #3 PHY LED indicators

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
G23	ESW_P4_LED0	O				3.3		Port #4 PHY LED indicators
W20	ESW_REXT	A				3.3		Band gap resistor which is connected to AVSS33_BG through a 24kΩ (±1%) resistor
W21	ESW_TANA	A				3.3		Analog test
AA22	ESW_TXVN_A_P0	A				3.3		Port #0 MDI Transceivers
Y25	ESW_TXVN_B_P0	A				3.3		Port #0 MDI Transceivers
Y22	ESW_TXVN_C_P0	A				3.3		Port #0 MDI Transceivers
W22	ESW_TXVN_D_P0	A				3.3		Port #0 MDI Transceivers
AA23	ESW_TXVP_A_P0	A				3.3		Port #0 MDI Transceivers
Y24	ESW_TXVP_B_P0	A				3.3		Port #0 MDI Transceivers
Y23	ESW_TXVP_C_P0	A				3.3		Port #0 MDI Transceivers
W23	ESW_TXVP_D_P0	A				3.3		Port #0 MDI Transceivers
V25	ESW_TXVN_A_P1	A				3.3		Port #1 MDI Transceivers
V22	ESW_TXVN_B_P1	A				3.3		Port #1 MDI Transceivers
U22	ESW_TXVN_C_P1	A				3.3		Port #1 MDI Transceivers
T25	ESW_TXVN_D_P1	A				3.3		Port #1 MDI Transceivers
V24	ESW_TXVP_A_P1	A				3.3		Port #1 MDI Transceivers
V23	ESW_TXVP_B_P1	A				3.3		Port #1 MDI Transceivers
U23	ESW_TXVP_C_P1	A				3.3		Port #1 MDI Transceivers
T24	ESW_TXVP_D_P1	A				3.3		Port #1 MDI Transceivers
T22	ESW_TXVN_A_P2	A				3.3		Port #2 MDI Transceivers
R22	ESW_TXVN_B_P2	A				3.3		Port #2 MDI Transceivers
P25	ESW_TXVN_C_P2	A				3.3		Port #2 MDI Transceivers
P22	ESW_TXVN_D_P2	A				3.3		Port #2 MDI Transceivers
T23	ESW_TXVP_A_P2	A				3.3		Port #2 MDI Transceivers
R23	ESW_TXVP_B_P2	A				3.3		Port #2 MDI Transceivers
P24	ESW_TXVP_C_P2	A				3.3		Port #2 MDI Transceivers
P23	ESW_TXVP_D_P2	A				3.3		Port #2 MDI Transceivers
N22	ESW_TXVN_A_P3	A				3.3		Port #3 MDI Transceivers
M25	ESW_TXVN_B_P3	A				3.3		Port #3 MDI Transceivers
M22	ESW_TXVN_C_P3	A				3.3		Port #3 MDI Transceivers
L22	ESW_TXVN_D_P3	A				3.3		Port #3 MDI Transceivers
N23	ESW_TXVP_A_P3	A				3.3		Port #3 MDI Transceivers
M24	ESW_TXVP_B_P3	A				3.3		Port #3 MDI Transceivers
M23	ESW_TXVP_C_P3	A				3.3		Port #3 MDI Transceivers
L23	ESW_TXVP_D_P3	A				3.3		Port #3 MDI Transceivers
K25	ESW_TXVN_A_P4	A				3.3		Port #4 MDI Transceivers
K22	ESW_TXVN_B_P4	A				3.3		Port #4 MDI Transceivers

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
J22	ESW_TXVN_C_P4	A				3.3		Port #4 MDI Transceivers
H25	ESW_TXVN_D_P4	A				3.3		Port #4 MDI Transceivers
K24	ESW_TXVP_A_P4	A				3.3		Port #4 MDI Transceivers
K23	ESW_TXVP_B_P4	A				3.3		Port #4 MDI Transceivers
J23	ESW_TXVP_C_P4	A				3.3		Port #4 MDI Transceivers
H24	ESW_TXVP_D_P4	A				3.3		Port #4 MDI Transceivers
E21	SCL-ETH	I				3.3		ESW test pin
K21	A_POR_BPS	I				3.3		ESW bypass reset
E24	ESW_XO	A				3.3		25MHz XTAL output
E25	ESW_XI	A				3.3		25MHz XTAL input
PCIe								
AA6	PCIE_VRT_P0	A				3.3		PCIe port0 reference pin
AB6	PCIE_CKN0	A				3.3		PCIe port0 reference clock (negative)
AC6	PCIE_CKP0	A				3.3		PCIe port0 reference clock (positive)
AE4	PCIE_TXN0	A				3.3		PCIe port0 differential transmit TX -
AD4	PCIE_TXP0	A				3.3		PCIe port0 differential transmit TX+
AE6	PCIE_RXN0	A				3.3		PCIe port0 differential receive RX -
AD6	PCIE_RXP0	A				3.3		PCIe port0 differential receive RX +
AB10	PCIE_VRT_P1	A				3.3		PCIe port1 reference pin
AC9	PCIE_CKN1	A				3.3		PCIe port1 reference clock (negative)
AB9	PCIE_CKP1	A				3.3		PCIe port1 reference clock (positive)
AB7	PCIE_TXN1	A				3.3		PCIe port1 differential transmit TX -
AC7	PCIE_TXP1	A				3.3		PCIe port1 differential transmit TX+
AE8	PCIE_RXN1	A				3.3		PCIe port1 differential receive RX -
AD8	PCIE_RXP1	A				3.3		PCIe port1 differential receive RX +
AD10	PCIE_CKN2	A				3.3		PCIe port2 reference clock (negative)
AC10	PCIE_CKP2	A				3.3		PCIe port2 reference clock (positive)
USB								
AC11	SSUSB_VRT_P0	A				3.3		USB port0 reference pin (USB3.0) PCIe port2 reference pin
Y11	USB_DM0	A				3.3		USB port0 HS/FS/LS data pin Data- (USB3.0)
AA11	USB_DP0	A				3.3		USB port0 HS/FS/LS data pin Data+ (USB3.0)
AB12	USB_RXN0	A				3.3		USB port0 SS data pin RX- (USB3.0) PCIe port2 differential receive RX -
AC12	USB_RXP0	A				3.3		USB port0 SS data pin RX+ (USB3.0) PCIe port2 differential receive RX +
AD11	USB_TXN0	A				3.3		USB port0 SS data pin TX- (USB3.0) PCIe port2 differential transmit TX -

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description	
		State *1	Aux *2	Pull					
AE11	USB_TXP0	A				3.3		USB port0 SS data pin TX+ (USB3.0) PCIe port2 differential transmit TX+	
AC18	SSUSB_VRT_P1	A				3.3		USB port1 reference pin (USB3.0)	
W12	USB_DM1	A				3.3		USB port1 data pin Data- (USB3.0)	
Y12	USB_DP1	A				3.3		USB port1 data pin Data+ (USB3.0)	
AB17	USB_RXN1	A				3.3		USB port1 SS data pin RX- (USB3.0)	
AC17	USB_RXP1	A				3.3		USB port1 SS data pin RX+ (USB3.0)	
AD16	USB_TXN1	A				3.3		USB port1 SS data pin TX- (USB3.0)	
AE16	USB_TXP1	A				3.3		USB port1 SS data pin TX+ (USB3.0)	
D11	CHG_DM_P2	A				3.3		USB port2 charger DM (BC1.1)	
C11	CHG_DP_P2	A				3.3		USB port2 charger DP (BC1.1)	
B12	USB_DM_P2	A				3.3		USB port2 data pin Data- (USB2.0 OTG)	
C12	USB_DP_P2	A				3.3		USB port2 data pin Data+ (USB2.0 OTG)	
C10	USB_VBUS_P2	A				3.3		USB port2 power for connected device +3.3V	
B10	USB_VRT_P2	A				3.3		USB port2 reference pin (USB2.0 OTG)	
DDR								**DDR3/L (1.5/1.35V)**	**LPDDR2 (1.2V)**
W4	RDQ0	I/O						Data bit #0	Data bit #23
AA3	RDQ1	I/O						Data bit #1	Data bit #22
W3	RDQ2	I/O						Data bit #2	Data bit #3
AA4	RDQ3	I/O						Data bit #3	Data bit #20
W1	RDQ4	I/O						Data bit #4	Data bit #4
Y1	RDQ5	I/O						Data bit #5	Data bit #2
W2	RDQ6	I/O						Data bit #6	Data bit #3
Y2	RDQ7	I/O						Data bit #7	Data bit #21
AB1	RDQ8	I/O						Data bit #8	Data bit #19
U1	RDQ9	I/O						Data bit #9	Data bit #11
AB2	RDQ10	I/O						Data bit #10	Data bit #16
U2	RDQ11	I/O						Data bit #11	Data bit #12
AB4	RDQ12	I/O						Data bit #12	Data bit #17
V4	RDQ13	I/O						Data bit #13	Data bit #9
AB3	RDQ14	I/O						Data bit #14	Data bit #18
V3	RDQ15	I/O						Data bit #15	Data bit #14
E2	RDQ16	I/O						Data bit #16	Data bit #25
G1	RDQ17	I/O						Data bit #17	Data bit #14
E1	RDQ18	I/O						Data bit #18	Data bit #26
G2	RDQ19	I/O						Data bit #19	Data bit #11

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description	
		State *1	Aux *2	Pull					
F3	RDQ20	I/O						Data bit #20	Data bit #27
G3	RDQ21	I/O						Data bit #21	Data bit #12
F4	RDQ22	I/O						Data bit #22	Data bit #30
G4	RDQ23	I/O						Data bit #23	Data bit #8
J3	RDQ24	I/O						Data bit #24	Data bit #13
D3	RDQ25	I/O						Data bit #25	Data bit #24
J4	RDQ26	I/O						Data bit #26	Data bit #10
D4	RDQ27	I/O						Data bit #27	Data bit #28
H2	RDQ28	I/O						Data bit #28	Data bit #9
D2	RDQ29	I/O						Data bit #29	Data bit #31
H1	RDQ30	I/O						Data bit #30	Data bit #15
D1	RDQ31	I/O						Data bit #31	Data bit #29
N2	RA0	O						Address bit #0	Address bit #11
R4	RA1	O						Address bit #1	Address bit #2
L4	RA2	O						Address bit #2	Address bit #5
N1	RA3	O						Address bit #3	Address bit #6
P1	RA4	O						Address bit #4	Address bit #10
N3	RA5	O						Address bit #5	Address bit #4
R3	RA6	O						Address bit #6	Address bit #3
P6	RA7	O						Address bit #7	Address bit #12
T4	RA8	O						Address bit #8	Address bit #14
M3	RA9	O						Address bit #9	Bank Address bit #2
T2	RA10	O						Address bit #10	Address bit #0
P4	RA11	O						Address bit #11	Address bit #13
P5	RA12	O						Address bit #12	Bank Address #0
N4	RA13	O						Address bit #13	Address bit #15
T3	RA14	O						Address bit #14	Address bit #1
L5	RA15	O						Address bit #15	RCAS
M5	RBA0	O						Bank Address #0	RRAS
P2	RBA1	O						Bank Address #1	Bank Address #1
K3	RBA2	O						Bank Address #2	Address bit #9
K1	RRAS	O						RAS	Address bit #8
L2	RCAS	O						CAS	Address bit #7
M4	RWE	O						RWE	RWE
R6	RCLK0	O						Clock	Clock
R5	RCLK0_	O						Clock	Clock
J5	RCLK1	O						Clock	Clock
J6	RCLK1_	O						Clock	Clock

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description	
		State *1	Aux *2	Pull					
Y4	RDQM0	O						DM#0	DM#2
U3	RDQM1	O						DM#1	DM#0
E4	RDQM2	O						DM#0	DM#3
E5	RDQM3	O						DM#1	DM#1
L1	RCS0	O						CS	CS
K4	RCS1	O						CS	CS
V5	RDQS0	I/O						DQS#0	DQS#2
V6	RDQS0_	I/O						DQS#0	DQS#2
W6	RDQS1	I/O						DQS#1	DQS#0
W5	RDQS1_	I/O						DQS#1	DQS#0
H4	RDQS2	I/O						DQS#0	DQS#3
H5	RDQS2_	I/O						DQS#0	DQS#3
F5	RDQS3	I/O						DQS#1	DQS#1
F6	RDQS3_	I/O						DQS#1	DQS#1
T1	RCKE	O						CKE	CKE
AC2	REXTDN	O						REXTDN	REXTDN
K2	DDR3RSTB	O						Reset	Reset
MIPI									
AB14	MIPI_TCN	I	1	-	NP	1.8		DSI0 CK lane N	
AC14	MIPI_TCP	I	1	-	NP	1.8		DSI0 CK lane P	
AB15	MIPI_TDN0	I	1	-	NP	1.8		DSI0 lane0 N	
AC15	MIPI_TDP0	I	1	-	NP	1.8		DSI0 lane0 P	
AE15	MIPI_TDN1	I	1	-	NP	1.8		DSI0 lane1 N	
AD15	MIPI_TDP1	I	1	-	NP	1.8		DSI0 lane1 P	
AD13	MIPI_VRT	A						External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground	
I2S									
AA19	I2S0_MCLK	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S master clock for CODEC	
Y19	I2S0_BCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S bit clock	
Y20	I2S0_LRCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S word select	
AB18	I2S0_DATA	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S data output	
AA20	I2S0_DATA_IN	I	1	PD	PU/PD	3.3	4/8/12/16	I2S data input	
AA18	I2S1_MCLK	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S master clock for CODEC	
V17	I2S1_BCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S bit clock	
W17	I2S1_LRCK	OH	1	PD	PU/PD	3.3	4/8/12/16	I2S word select	
Y18	I2S1_DATA	OL	1	PD	PU/PD	3.3	4/8/12/16	I2S data output	
Y17	I2S1_DATA_IN	I	1	PD	PU/PD	3.3	4/8/12/16	I2S data input	
PCM									

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
C19	PCM_CLK	I	0	PD	PU/PD	3.3	4/8/12/16	PCM clock
D19	PCM_SYNC	I	0	PD	PU/PD	3.3	4/8/12/16	PCM frame sync.
C18	PCM_TX	I	0	PD	PU/PD	3.3	4/8/12/16	PCM TX data
D18	PCM_RX	I	0	PD	PU/PD	3.3	4/8/12/16	PCM RX data
LCD								
V14	DSI_TE	I	0	PD	PU/PD	1.8	2/4/6/8	DSI tearing effect control
V16	LCM_RST	I	0	PD	PU/PD	1.8	2/4/6/8	LCM reset
WBG								
AB20	WB_CRTL0	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AC20	WB_CRTL1	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AB19	WB_CRTL2	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AC19	WB_CRTL3	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AD19	WB_CRTL4	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AE19	WB_CRTL5	I	1	PD	PU/PD	1.8	2/4/6/8	WB control for CONN_RF
AB24	WB_SEN	OL	1	PD	PU/PD	1.8	2/4/6/8	SPI for CONN_RF
AC23	WB_SCLK	OL	1	PD	PU/PD	1.8	2/4/6/8	SPI for CONN_RF
Y21	WB_RSTB	OL	1	PD	PU/PD	1.8	2/4/6/8	Reset for CONN_RF
AB21	WB_SDATA	I	1	PD	PU/PD	1.8	2/4/6/8	SPI for CONN_RF
AD21	WB_RXIN	A				1.8		RX_IN for WIFI/BT RX
AD22	WB_RXQN	A				1.8		RX_QN for WIFI/BT RX
AD24	WB_TXQP	A				1.8		TX_QP for WIFI/BT TX
AD25	WB_TXQN	A				1.8		TX_QN for WIFI/BT TX
AE21	WB_RXIP	A				1.8		RX_IP for WIFI/BT RX
AE22	WB_RXQP	A				1.8		RX_QP for WIFI/BT RX
AE23	WB_TXIP	A				1.8		TX_IP for WIFI/BT TX
AE24	WB_TXIN	A				1.8		TX_IN for WIFI/BT TX
AC21	TEST_GQP	A				1.8		FT test Pin
AC22	TEST_GQN	A				1.8		FT test Pin
AC24	TEST_GIN	A				1.8		FT test Pin
AC25	TEST_GIP	A				1.8		FT test Pin
AB25	XIN_WBG	A				1.8		26MHz clock input for WBG
PMIC								
E11	PWRAP_INT	I	0	PD	PU/PD	1.8	2/4/6/8	PMIC interrupt
D10	PWRAP_SPI0_MO	OL	1	PD	PU/PD	1.8	2/4/6/8	PMIC SPI data out
F11	PWRAP_SPI0_MI	OL	1	PD	PU/PD	1.8	2/4/6/8	PMIC SPI data in
H12	PWRAP_SPI0_CK	OL	1	PD	PU/PD	1.8	2/4/6/8	PMIC SPI clock
H11	PWRAP_SPI0_CK2	OL	1	PD	PU/PD	1.8	2/4/6/8	GPIO
E12	PWRAP_SPI0_CSN	OH	1	PU	PU/PD	1.8	2/4/6/8	PMIC SPI chip select

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
G11	PWRAP_SPI0_CSN2	OH	1	PU	PU/PD	1.8	2/4/6/8	GPIO
ABB								
A20	REFP	A						Positive reference port for internal circuit
A17	26M_CLKSQ	A						26MHz clock input for AP
D20	AUX_IN0	A						AuxADC external input channel 0
B20	AUX_IN1	A						AuxADC external input channel 1
E20	AUX_IN2	A						AuxADC external input channel 2
F21	AUX_IN3	A						AuxADC external input channel 3
F20	AUX_IN4	A						AuxADC external input channel 4
C20	AUX_IN5	A						AuxADC external input channel 5
MISC								
A13	RTC32K_CK	I	1	PD	PU/PD	1.8	2/4/6/8	Real time clock 32.768 kHz
B13	SRCLKENAI	I	1	PD	PU/PD	1.8	2/4/6/8	26MHz co-clock enable input
C13	SRCLKENA	OH	1	PU	PU/PD	1.8	2/4/6/8	26MHz co-clock enable output
C14	SYSRSTB	I	-	PU	PU	1.8	-	Power on reset
D14	WATCHDOG	OH	1	PD	PU/PD	1.8	2/4/6/8	Watchdog reset
J21	TESTMODE	I	-	PD	PD	1.8	-	Test mode
AE3	FSOURCE_P0	A				1.8		E-FUSE blowing power control
D15	IR	I	0	PD	PU/PD	1.8	-	Infra red receiver
L8	TP_MEMPLL	A				1.8		PLL test
W14	AUD_EXT_CK1	I	3	PD	PU/PD	3.3	4/8/12/16	Audio clock in1
V15	AUD_EXT_CK2	I	3	PD	PU/PD	3.3	4/8/12/16	Audio clock in2
POWER								
M21, N20	DVDD33_IO	P				3.3		Digital I/O power supply
J10, J11, J14, J9, K10, L10, L9, M9, N8, P14, P9, R13, R14, R8, T12, T8, U11, U12, U8, V7, V8	VCCK	P				1.15		Digital core power supply
K12, K13, K14, K16, L12, L13, L14, L15, M12, M13, M14	VCCK_VPROC	P				0.85 1.05 1.15 1.31		CPU core power supply
P18, R17, R18	DVDD_K_1	P				1.0		ESW core power supply
AC5	DVDD18_IO	P				1.8		Digital I/O power supply

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
H13	DVDD18_IO_DPI	P				1.8		Digital I/O power supply
AD5	DVDD18_IO_I2S	P				1.8		Digital I/O power supply
F13	DVDD18_IO_MSDC0	P				1.8		Digital I/O power supply
AB5	DVDD18_IO_MSDC1	P				1.8		Digital I/O power supply
G13	DVDD18_IO_NOR	P				1.8		Digital I/O power supply
R16	DVDD18_IO_RGMII	P				1.8		Digital I/O power supply
AE18	DVDD18_IO_WBCT	P				1.8		Digital I/O power supply
AE13	DVDD18_MIPITX	P				1.8		Digital I/O power supply
F9	DVDD28_DPI	P				3.3		Digital I/O power supply
V10	DVDD28_I2S	P				3.3		Digital I/O power supply
G9	DVDD28_MSDC0	P				1.8 3.3		Digital I/O power supply
W9	DVDD28_MSDC1	P				3.3		Digital I/O power supply
E9	DVDD28_NOR	P				3.3		Digital I/O power supply
T7	VREF0	P				0.75 0.675 0.6		DRAM reference voltage power supply
J7, K7, L7, M7, N7, P7, R7,	VDD_EMI	P				1.5 1.35 1.2		DRAM I/O power supply
T17	DVDD_GE1_VREF	P						GE1 reference voltage power supply
T18, U17	DVDD_GE1_IO	P				1.8		GE1 I/O power supply
R19, R20, R21, P21, P19	AVDD10_AFE_P0/1/2/3/4	P				1.0		ESW analog power supply
Y8	AVDD11_PCIE_P0	P				1.15		PCIe port0 analog power supply
AA8	AVDD11_PCIE_P1	P				1.15		PCIe port1 analog power supply
W13	AVDD11_SSUSB_P0	P				1.15		USB port0 analog power supply
AC16	AVDD11_SSUSB_P1	P				1.15		USB port1 analog power supply
B19	AVDD18_AP	P				1.8		ADC analog power supply
K8	AVDD18_MEMPLL	P				1.8		DRAM PLL power supply
AE5	AVDD18_PCIE	P				1.8		PCIe analog power supply
M18	AVDD18_PLLGP	P				1.8		PLL group analog power supply
AA12	AVDD18_SSUSB	P				1.8		SSUSB analog power supply
AE10	AVDD18_USB	P				1.8		USB analog power supply
A12	AVDD18_USB_P2	P				1.8		USB analog power supply
AD18	AVDD18_WBG	P				1.8		WiFi/BT analog power supply
W18, V20, V18, V19, W19	AVDD33_LD_P0/1/2/3/4	P				3.3		ESW analog power supply

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
V21	AVDD33_PLL_1	P				3.3		ESW PLL analog power supply
Y10	AVDD33_USB	P				3.3		USB analog power supply
A10	AVDD33_USB_P2	P				3.3		USB analog power supply
GROUND								
K9	AVSS18_MEMPLL	G						
AB23, AD23, AE25	AVSS18_WBG	G						
A19	AVSS18_AP	G						
AA7, AC8	AVSS_PCIE	G						
AB11, AB16	AVSS_SSUSB	G						
D12	AVSS_USB_P2	G						
M19	AVSS18_PLLGP	G						
P17	AVSS33_VBG	G						
AB13	DVSS18_MIPITX	G						

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Pin	Name	Reset			PU/PD *3,4	Voltage(V)	Driving (mA)	Description
		State *1	Aux *2	Pull				
A1, A25, AE1, B24, C3, E3, H23, H3, H6, J12, J13, J8, K11, K6, L11, L16, L17, L3, L6, M10, M11, M15, M17, M20, M6, M8, N10, N11, N12, N13, N14, N15, N16, N18, N19, N21, N6, N9, P10, P11, P12, P13, P15, P20, P3, P8, R10, R11, R12, R15, R9, T10, T11, T15, T9, U4, U5, Y3	GND	G						Ground

NOTE:

1. I: Input
   O: Output
   OH: Output high
   OL: Output low
   I/O: Bi-directional
   P: Power
   G: Ground
   NC: Not connected
   A: Analog
2. AUX: Aux function. (Please reference to next section for detail.)
3. The internal pull resistance value is 75kΩ.
4. PD: Internal pull-down
   PU: Internal pull-up
   NP: No pull-down/up

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2.2.1 Constant Tie Pins

Table 2-3 Constant tied pins

Pin name	Description
TESTMODE	Test mode (tie to GND)
FSOURCE_P	EFUSE blowing (tie to GND)

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2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7623A provides up to 137 GPIO pins. Users can configure registers specify the pin function. For more information, see the Programmer's Guide. The pin's default function mode is specified with **bold** type words.

2.3.1 Pin share scheme

Table 2-4 Pin Share

Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
PWRAP_SPI0_MI	148	GPIO0	**B0:PWRAP_SPIDO**	B0:PWRAP_SPIDI				
PWRAP_SPI0_MO	149	GPIO1	**B0:PWRAP_SPIDI**	B0:PWRAP_SPIDO				
PWRAP_INT	150	**GPIO2**	I0:PWRAP_INT					
PWRAP_SPI0_CK	151	GPIO3	**O:PWRAP_SPICK_I**					
PWRAP_SPI0_CSN	152	GPIO4	**O:PWRAP_SPICS_B_I**					
PWRAP_SPI0_CK2	155	GPIO5	**O:PWRAP_SPICK2_I**					
PWRAP_SPI0_CSN2	156	GPIO6	**O:PWRAP_SPICS2_B_I**					
SPI1_CSN	153	**GPIO7**	O:SPI1_CS					
SPI1_MI	154	**GPIO8**	I0:SPI1_MI	O:SPI1_MO				
SPI1_MO	157	**GPIO9**	O:SPI1_MO	I0:SPI1_MI				
RTC32K_CK	158	GPIO10	**I0:RTC32K_CK**					
WATCHDOG	159	GPIO11	**O:WATCHDOG**					
SRCLKENA	160	GPIO12	**O:SRCLKENA**					
SRCLKENAI	161	GPIO13	**I0:SRCLKENAI**					
GPIO14	162	**GPIO14**	I1:URXD2	O:UTXD2				
GPIO15	163	**GPIO15**	O:UTXD2	I1:URXD2				
PCM_CLK	166	**GPIO18**	B0:PCM_CLK0					B0:AP_PCM_CLKO
PCM_SYNC	167	**GPIO19**	B0:PCM_SYNC					B0:AP_PCM_SYNC
PCM_RX	N/A	**GPIO20**	I0:PCM_RX			O:PCM_TX		I0:AP_PCM_RX
PCM_TX	N/A	**GPIO21**	O:PCM_TX			I0:PCM_RX		O:AP_PCM_TX
EINT0	0	GPIO22	I1:UCTS0	**O: PCIE0_PERST_N**				
EINT1	1	GPIO23	O:URTS0	**O: PCIE1_PERST_N**				
EINT2	2	GPIO24	I1:UCTS1	**O: PCIE2_PERST_N**				
EINT3	3	**GPIO25**	O:URTS1					
EINT4	4	**GPIO26**	I1:UCTS3					I1: PCIE2_WAKE_N
EINT5	5	**GPIO27**	O:URTS3					I1: PCIE1_WAKE_N
EINT6	6	**GPIO28**	O:DRV_VBUS					I1: PCIE0_WAKE_N
EINT7	7	GPIO29	I0:IDDIG	I0: MSDC1_WP				**O: PCIE2_PERST_N**
I2S1_DATA	15	GPIO33	**B0:I2S1_DATA**		O:PCM_TX			O: AP_PCM_TX
I2S1_DATA_IN	16	GPIO34	**B0:I2S1_DATA_IN**		I0:PCM_RX			I0:AP_PCM_RX
I2S1_BCK	17	GPIO35	**B0:I2S1_BCK**		B0:PCM_CLK0			B0:AP_PCM_CLKO

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Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
I2S1_LRCK	18	GPIO36	**B0:I2S1_LRCK**		B0:PCM_SYNC			B0: AP_PCM_SYNC
I2S1_MCLK	19	GPIO37	**B0:I2S1_MCLK**					
JTMS	21	GPIO39	**B1:JTMS**					
JTCK	22	GPIO40	**I0:JTCK**					
JTDI	23	GPIO41	**I1:JTDI**					
JTDO	24	GPIO42	**O:JTDO**					
NCLE	25	**GPIO43**	O:NCLE	O: SFLASH_CS2_L				
NCEB1	26	**GPIO44**	O:NCEB1	I0:IDDIG				
NCEB0	27	**GPIO45**	O:NCEB0	O:DRV_VBUS				
IR	28	**GPIO46**	I0:IR					
NREB	29	**GPIO47**	O:NREB					
NRNB	30	**GPIO48**	I1:NRNB					
I2S0_DATA	31	GPIO49	**B0:I2S0_DATA**		O:PCM_TX			O: AP_I2S_DO
SPI0_CSN	35	**GPIO53**	O:SPI0_CS				O:PWM1	
SPI0_CK	36	**GPIO54**	O:SPI0_CK					
SPI0_MI	37	**GPIO55**	I0:SPI0_MI	O:SPI0_MO	I0: MSDC1_WP		O:PWM2	
SPI0_MO	38	**GPIO56**	O:SPI0_MO	I0:SPI0_MI				
WB_RSTB	41	GPIO60	**O:WB_RSTB**					
GPIO61	42	GPIO61	**I0:TEST_FD**					
GPIO62	43	GPIO62	**I0:TEST_FC**					
WB_SCLK	44	GPIO63	**O:WB_SCLK**					
WB_SDATA	45	GPIO64	**B0:WB_SDATA**					
WB_SEN	46	GPIO65	**O:WB_SEN**					
WB_CRTL0	47	GPIO66	**B0:WB_CRTL0**					
WB_CRTL1	48	GPIO67	**B0:WB_CRTL1**					
WB_CRTL2	49	GPIO68	**B0:WB_CRTL2**					
WB_CRTL3	50	GPIO69	**B0:WB_CRTL3**					
WB_CRTL4	51	GPIO70	**B0:WB_CRTL4**					
WB_CRTL5	52	GPIO71	**B0:WB_CRTL5**					
I2S0_DATA_IN	53	GPIO72	**B0:I2S0_DATA_IN**		I0:PCM_RX	O:PWM0	O:DISP_PWM	I0: AP_I2S_DI
I2S0_LRCK	54	GPIO73	**B0:I2S0_LRCK**		B0:PCM_SYNC			B0: AP_I2S_LRCK
I2S0_BCK	55	GPIO74	**B0:I2S0_BCK**		B0:PCM_CLK0			B0: AP_I2S_BCK
SDA0	56	GPIO75	**B1:SDA0**					
SCL0	57	GPIO76	**B1:SCL0**					
LCM_RST	64	**GPIO83**	O:LCM_RST					
DSI_TE	65	**GPIO84**	I0:DSI_TE					
MIPI_TCN	N/A	GPI95	**O:TCN**					
MIPI_TCP	N/A	GPI96	**O:TCP**					
MIPI_TDN1	N/A	GPI97	**O:TDN1**					
MIPI_TDP1	N/A	GPI98	**O:TDP1**					

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Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
MIPI_TDN0	N/A	GPI99	**O:TDN0**					
MIPI_TDP0	N/A	GPI100	**O:TDP0**					
MSDC1_CMD	78	GPIO105	**B0:MSDC1_CMD**		B1:SDA1			O:I2SOUT_BCK
MSDC1_CLK	79	GPIO106	**O:MSDC1_CLK**		B1:SCL1			O:I2SOUT_LRCK
MSDC1_DAT0	80	GPIO107	**B0:MSDC1_DAT0**				O:UTXD0	O:I2SOUT_DATA_OUT
MSDC1_DAT1	81	GPIO108	**B0:MSDC1_DAT1**		O:PWM0		I1:URXD0	O:PWM1
MSDC1_DAT2	82	GPIO109	**B0:MSDC1_DAT2**		B1:SDA2		O:UTXD1	O:PWM2
MSDC1_DAT3	83	GPIO110	**B0:MSDC1_DAT3**		B1:SCL2		I1:URXD1	O:PWM3
MSDC0_DAT7	84	GPIO111	**B0:MSDC0_DAT7**			B0:NLD7		
MSDC0_DAT6	85	GPIO112	**B0:MSDC0_DAT6**			B0:NLD6		
MSDC0_DAT5	86	GPIO113	**B0:MSDC0_DAT5**			B0:NLD5		
MSDC0_DAT4	87	GPIO114	**B0:MSDC0_DAT4**			B0:NLD4		
MSDC0_RSTB	88	GPIO115	**O:MSDC0_RSTB**			B0:NLD8		
MSDC0_CMD	89	GPIO116	**B0:MSDC0_CMD**			O:NALE		
MSDC0_CLK	90	GPIO117	**O:MSDC0_CLK**			O:NWEB		
MSDC0_DAT3	91	GPIO118	**B0:MSDC0_DAT3**			B0:NLD3		
MSDC0_DAT2	92	GPIO119	**B0:MSDC0_DAT2**			B0:NLD2		
MSDC0_DAT1	93	GPIO120	**B0:MSDC0_DAT1**			B0:NLD1		
MSDC0_DAT0	94	GPIO121	**B0:MSDC0_DAT0**			B0:NLD0	O:WATCHDOG	
GPIO122	95	GPIO122	**B0:TEST**			B1:SDA2	I1:URXD0	
GPIO123	96	GPIO123	**I0:TEST**			B1:SCL2	O:UTXD0	
GPIO124	97	GPIO124	**B0:TEST**			B1:SDA1	O:PWM3	
GPIO125	98	GPIO125	B0:TEST			B1:SCL1	O:PWM4	
I2S0_MCLK	99	GPIO126	**B0:I2S0_MCLK**					O: AP_I2S_MCLK
SPI1_CK	111	**GPIO199**	O:SPI1_CK					
URXD2	112	**GPIO200**						I1:URXD2
UTXD2	113	**GPIO201**						O:UTXD2
PWM0	115	**GPIO203**	O:PWM0	O:DISP_PWM				
PWM1	116	**GPIO204**	O:PWM1					
PWM2	117	**GPIO205**	O:PWM2					
PWM3	118	**GPIO206**	O:PWM3					
PWM4	119	**GPIO207**	O:PWM4					
AUD_EXT_CK1	120	GPIO208	I0:AUD_EXT_CK1	O:PWM0	**O: PCIE0_PERST_N**		O:DISP_PWM	
AUD_EXT_CK2	121	GPIO209	I0:AUD_EXT_CK2	I0: MSDC1_WP	**O: PCIE1_PERST_N**		O:PWM1	
SFLASH_IO_3	122	**GPIO236**	B0: SFLASH_IO_3	I0:IDDIG				
SFLASH_IO_2	123	**GPIO237**	B0: SFLASH_IO_2	O:DRV_VBUS				
SFLASH_IO_1	124	**GPIO238**	B0: SFLASH_IO_1					
SFLASH_IO_0	125	**GPIO239**	B0: SFLASH_IO_0					
SFLASH_CS_L	126	**GPIO240**	O:SFLASH_CS_L					
SFLASH_CLK	127	**GPIO241**	O:SFLASH_CLK					

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Pin	EINT	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6
URTS2	128	**GPIO242**	O:URTS2	O:UTXD3	I1:URXD3	B1:SCL1		
UCTS2	129	**GPIO243**	I1:UCTS2	I1:URXD3	O:UTXD3	B1:SDA1		
GPIO250	135	GPIO250	**B0:TEST_MD7**					I1: PCIE0_CLKREQ_N
GPIO251	136	GPIO251	**B0:TEST_MD6**					I1: PCIE0_WAKE_N
GPIO252	137	GPIO252	**B0:TEST_MD5**					I1: PCIE1_CLKREQ_N
GPIO253	138	GPIO253	**B0:TEST_MD4**					I1: PCIE1_WAKE_N
GPIO254	139	GPIO254	**B0:TEST_MD3**					I1: PCIE2_CLKREQ_N
GPIO255	140	GPIO255	**B0:TEST_MD2**					I1: PCIE2_WAKE_N
GPIO256	141	GPIO256	**B0:TEST_MD1**					
GPIO257	142	GPIO257	**B0:TEST_MD0**					
MSDC1_INS	146	**GPIO261**	I0:MSDC1_INS					
G2_TXEN	N/A	**GPIO262**	B0: G2_TXEN					
G2_TXD3	N/A	**GPIO263**	B0: G2_TXD3					
G2_TXD2	N/A	**GPIO264**	B0: G2_TXD2					
G2_TXD1	N/A	**GPIO265**	B0: G2_TXD1					
G2_TXD0	N/A	**GPIO266**	B0: G2_TXD0					
G2_TXCLK	N/A	**GPIO267**	B0: G2_TXC					
G2_RXCLK	N/A	**GPIO268**	B0: G2_RXC					
G2_RXD0	N/A	**GPIO269**	B0: G2_RXD0					
G2_RXD1	N/A	**GPIO270**	B0: G2_RXD1					
G2_RXD2	N/A	**GPIO271**	B0: G2_RXD2					
G2_RXD3	N/A	**GPIO272**	B0: G2_RXD3					
G2_RXDV	N/A	**GPIO274**	B0: G2_RXDV					
G2_MDC	N/A	**GPIO275**	O: MDC					
G2_MDIO	N/A	**GPIO276**	B0: MDIO					
JTAG_RESET	147	**GPIO278**	I0:JTAG_RESET					

Note:

" Bold" = Default function mode.

"O" = output function

"I0" = input function, high active

"I1" = input function, low active

"B0" = bi-direction function, high active

"B1" = bi-direction function, low active

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2.3.2 EINT Usage Tips

For the GPIOs used ad external interrupt source, there are some notes need take attention.

Pin Name	Notes
EINT0	Need Enable De-bounce Feature
EINT1	Need Enable De-bounce Feature
EINT2	Need Enable De-bounce Feature
EINT3	Need Enable De-bounce Feature
EINT4	Need Enable De-bounce Feature
EINT5	Need Enable De-bounce Feature
EINT6	Need Enable De-bounce Feature
EINT7	Need Enable De-bounce Feature

2.3.3 MIPI GPIO Usage Tips

MIPI pins are listed in below table, and they are analog and digital share pins. In GPIO mode, these MIPI pins can only be use as GPI pins, and can't be used as GPO pins. In order to get the good performance, all these pins are either in MIPI CSI mode or in GPI mode, and it is not suggested that part of these pins are in MIPI CSI mode and other pins are in GPI mode.

Pin Name	Notes
MIPI_TCN	GPI95
MIPI_TCP	GPI96
MIPI_TDN1	GPI97
MIPI_TDP1	GPI98
MIPI_TDN0	GPI99
MIPI_TDP0	GPI100

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2.3.4 xMII PHY/MAC Pin Mapping

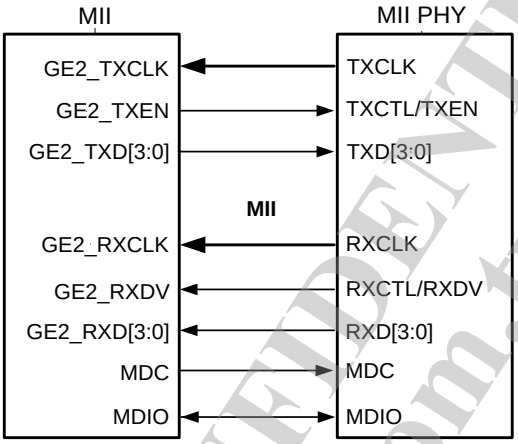

Figure 2-1 MII → MII PHY

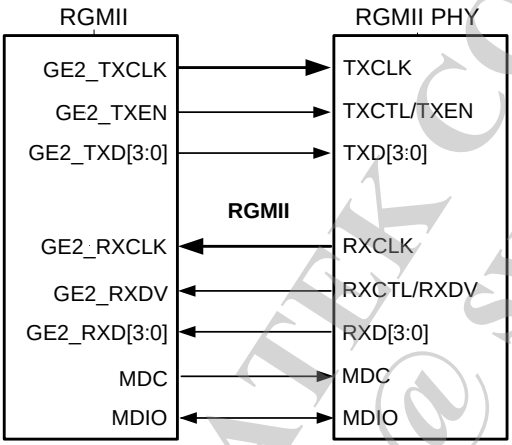

Figure 2-2 RGMII → RGMII PHY

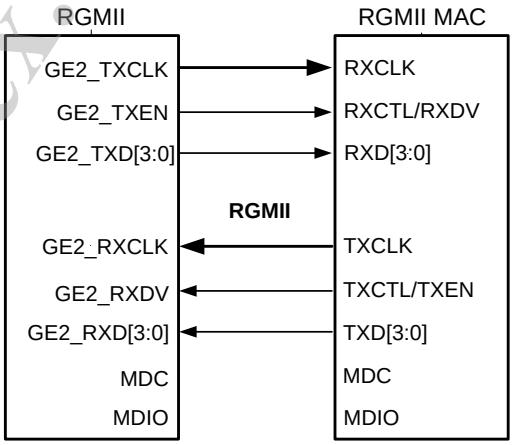

Figure 2-3 RGMII→ RGMII MAC

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2.4 Strapping Options

Table 2-5 Strapping

Pin Name	Strapping Name	Description
{NCLE, NREB}	Boot Order	0: eMMC → USB DL → NAND 1: NAND → USB DL → eMMC 2: USB DL → eMMC → NAND 3: USB DL → eMMC → NAND
JTAG_RESET	Boot Download Mode	0: Trigger USB DL directly 1: According to strapping boot order

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD28_DPI DVDD28_I2S DVDD28_MSDC0 DVDD28_MSDC1 DVDD28_NOR DVDD28_RGMII	3.3V supply voltage	-0.3	3.63	V
AVDD33_USB AVDD33_USB_P2 AVDD33_VDAC_C	3.3V supply voltage	-0.3	3.465	V
DVDD18_IO DVDD18_IO_DPI DVDD18_IO_I2S DVDD18_IO_MSDC0 DVDD18_IO_MSDC1 DVDD18_IO_NOR DVDD18_IO_RGMII DVDD18_IO_WBCT DVDD18_MIPITX DVDD28_MSDC0 DVDD_GE1_IO	1.8V supply voltage	-0.3	2.1	V
AVDD18_AP AVDD18_MEMPLL AVDD18_PCIE AVDD18_PLLGP AVDD18_SSUSB AVDD18_USB AVDD18_USB_P2 AVDD18_WBG AVDD18_DAC	1.8V supply voltage	-0.3	1.89	V
VDD_EMI	1.5V supply voltage	-0.3	1.9	V
	1.35V supply voltage	-0.3	1.9	V
	1.2V supply voltage	-0.3	1.9	V
AVDD11_PCIE_P0 AVDD11_PCIE_P1 AVDD11_SSUSB_P0 AVDD11_SSUSB_P1	1.15V supply voltage	-0.3	1.2	V

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3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD28_DPI DVDD28_I2S DVDD28_MSDC0 DVDD28_MSDC1 DVDD28_NOR DVDD28_RGMII	3.3V supply voltage	2.97	3.3	3.63	V
AVDD33_USB AVDD33_USB_P2 AVDD33_VDAC_C	3.3V supply voltage	3.135	3.3	3.465	V
DVDD18_IO DVDD18_IO_DPI DVDD18_IO_I2S DVDD18_IO_MSDC0 DVDD18_IO_MSDC1 DVDD18_IO_NOR DVDD18_IO_RGMII DVDD18_IO_WBCT DVDD18_MIPITX DVDD28_MSDC0 DVDD_GE1_IO	1.8V supply voltage	1.62	1.8	1.98	V
AVDD18_AP AVDD18_MEMPLL AVDD18_PCIE AVDD18_PLLGP AVDD18_SSUSB AVDD18_USB AVDD18_USB_P2 AVDD18_WBG AVDD18_DAC	1.8V supply voltage	1.71	1.8	1.89	V
VDD_EMI	1.5V supply voltage	1.425	1.5	1.575	V
	1.35V supply voltage	1.215	1.35	1.485	V
	1.2V supply voltage	1.14	1.2	1.3	V
AVDD11_PCIE_P0 AVDD11_PCIE_P1 AVDD11_SSUSB_P0 AVDD11_SSUSB_P1	1.15V supply voltage	1.0925	1.15	1.2075	V
VCCK	Digital core supply voltage	1.035	1.15	1.265	V
VCCK_VPROC	Digital processor supply voltage	0.85	1.15	1.31	V

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3.3 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

Table 3-3 Thermal Characteristics

Symbol	Description	Performance	
		Typ	Unit
T_J	Maximum junction temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance for JEDEC 4L system PCB	20.91	°C/W
θ_{JC}	Thermal Resistance for JEDEC system PCB	5.37	°C/W
ψ_{Jt}	Thermal Characterization parameter for JEDEC 4L system PCB	3.35	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4”x4.5”)

Symbol	Parameters	Min.	Typ.	Max.	Unit
Tc	Case Temperature	-10	-	113	C

Note: The device is mounted on a 4L PCB, 200 x 170 x 1.6mm, natural convection and without thermal solution.

3.4 Current Consumption

Please check with application note.

Table 3-4 Current Consumption

3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 0 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.6 External XTAL Specification

Table 3-5 External XTAL Specifications (AP)

Frequency	26 Mhz
Amplitude	350(min)/500(typ.)/1000(max) mV
Duty cycle	50+-5%

Table 3-6 External XTAL Specifications (ESW)

Frequency	25 Mhz

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Frequency offset	+/- 20 ppm
Duty cycle	50+-5%

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3.7 AC Electrical Characteristics

3.7.1 DDR SDRAM Interface

The LPDDR2 SDRAM interface complies with 533 MHz timing requirements for standard LPDDR2 SDRAM. The interface drivers are SSTL_12 drivers matching the EIA/JEDEC standard JESD209-2B.

Table 3-7 LPDDR2 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Average clock period	1.875	100	ns	
tCH(avg)	Average clock high pulse width	0.45	0.55	tCK(avg)	
tCL(avg)	Average clock low pulse width	0.45	0.55	tCK(avg)	
tCH(abs)	Absolute clock high pulse width	0.43	0.57	tCK(avg)	
tCL(abs)	Absolute clock low pulse width	0.43	0.57	tCK(avg)	
tCKE	CKE min. pulse width	3	-	tCK(avg)	
tIS	Command/Address setup time to CK	220	-	ps	
tIH	Command/Address hold time from CK	220	-	ps	
tDQSCK	DQS output access time from SDRAM CLK	2500	5500	ps	
tDQSQ	Data skew of DQS and associated DQ	-	200	ps	
tQHS	Data hold skew factor	-	230	ps	
tQSH	DQS Output High Pulse Width	tCH(abs) - 0.05	-	tCK(avg)	
tQSL	DQS Output Low Pulse Width	tCL (abs) - 0.05	-	tCK(avg)	
tQHP	Data Half Period	min(tQSH,tQSL)		tCK(avg)	
tQH	DQ/DQS output hold time from DQS	tQHP - tQHS	-	ns	
tRPRE	Read preamble	0.9	-	tCK(avg)	
tRPST	Read postamble	tCL(abs) - 0.05	-	tCK(avg)	
tDH	DQ and DQM input hold time	210	-	ps	
tDS	DQ and DQM input setup time	210	-	ps	
tDIPW	DQ and DM input pulse width	0.35	-	tCK(avg)	
tDQSS	Write command to 1st DQS latching transition	0.75	1.25	tCK(avg)	
tDQSH	DQS input high pulse width	0.4	-	tCK(avg)	
tDQSL	DQS input low pulse width	0.4	-	tCK(avg)	
tDSS	DQS falling edge setup time to CK	0.2	-	tCK(avg)	
tDSH	DQS falling edge hold time from CK	0.2	-	tCK(avg)	

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Symbol	Description	Min	Max	Unit	Remark
tWPRE	DQS write preamble	0.35	-	tCK(avg)	
tWPST	DQS write postamble	0.4	-	tCK(avg)	

The DDR3 SDRAM interface complies with 800 MHz timing requirements for standard DDR3 SDRAM. The interface drivers are SSTL_15 drivers matching the EIA/JEDEC standard JESD79-3E.

Table 3-8 DDR3 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Average clock period	1.25	-	ns	
tCH(avg)	Average clock high pulse width	0.47	0.53	tCK(avg)	
tCL(avg)	Average clock low pulse width	0.47	0.53	tCK(avg)	
tCH(abs)	Absolute clock high pulse width	0.43	-	tCK(avg)	
tCL(abs)	Absolute clock low pulse width	0.43	-	tCK(avg)	
tIS	Command/Address setup time to CK	170	-	ps	
tIH	Command/Address hold time from CK	120	-	ps	
tDQSCK	DQS output access time from CK	-225	225	ps	
tDQSQ	Data skew of DQS and associated DQ	-	100	ps	
tQSH	DQS output high time	0.4	-	tCK(avg)	
tQSL	DQS output low time	0.4	-	tCK(avg)	
tQH	DQ/DQS output hold time from DQS	0.38	-	tCK(avg)	
tRPRE	DQS read preamble	0.9	-	tCK(avg)	
tRPST	DQS read postamble	0.3	-	tCK(avg)	
tDH	DQ hold time from DQS	45	-	ps	
tDS	DQ setup time to DQS	10	-	ps	
tDIPW	DQ and DM input pulse width	360	-	Ps	
tDQSS	DQS rising edge to CK rising edge	-0.27	0.27	tCK(avg)	
tDQSH	DQS input high pulse width	0.45	0.55	tCK(avg)	
tDQSL	DQS input low pulse width	0.45	0.55	tCK(avg)	
tDSS	DQS falling edge setup time to CK	0.18	-	tCK(avg)	
tDSH	DQS falling edge hold time from CK	0.18	-	tCK(avg)	
tWPRE	DQS write preamble	0.9	-	tCK(avg)	
tWPST	DQS write postamble	0.3	-	tCK(avg)	

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3.7.2 RGMII Interface

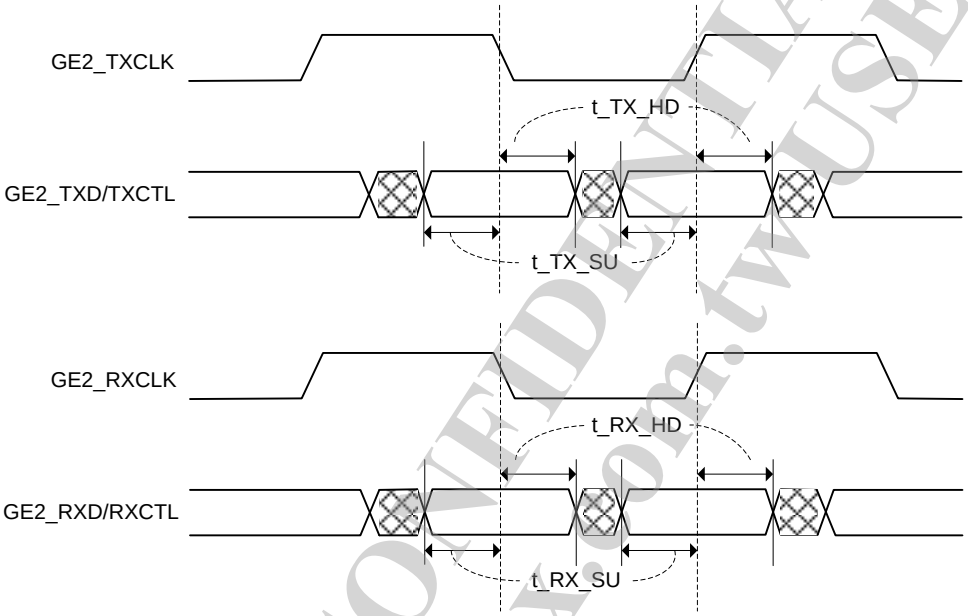

Figure 3-1 RGMII Timing

Table 3-9 RGMII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. GE0_TXD*, GE0_TXEN)	1.2	-	ns	output load: 5 pF
t_TX_HD	Hold time for output signals	1.2	-	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

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3.7.3 MII Interface (25 Mhz)

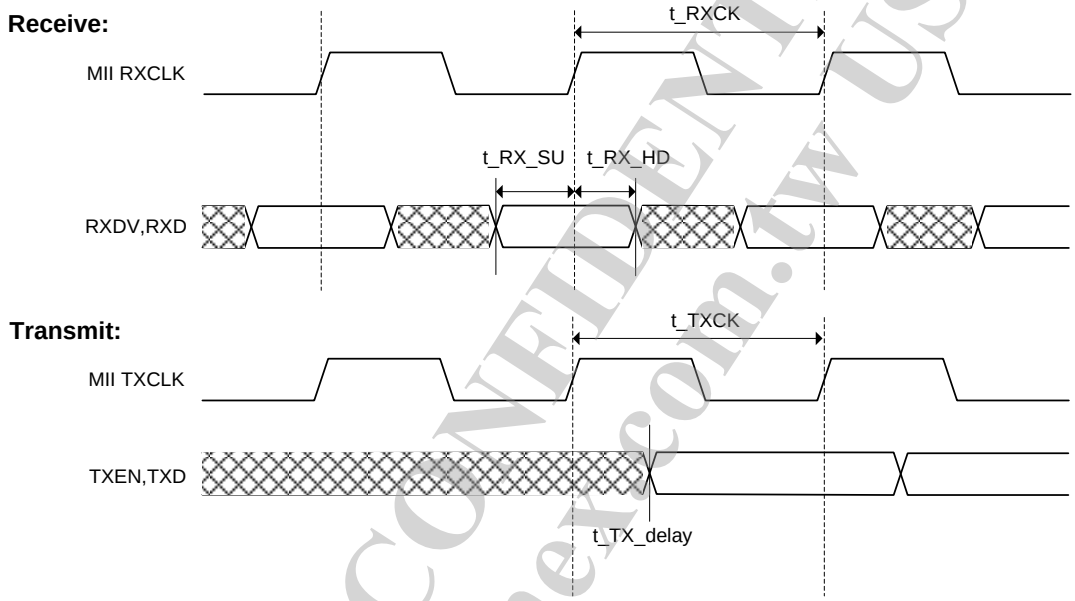

Figure 3-2 MII Timing

Table 3-10 MII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Delay to output signals (e.g. GE0_TXD*, GE0_TXEN)	6	22	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	10	-	ns	
t_RX_HD	Hold time for input signals	5	-	ns	

Note: For 25 Mhz TXCLK & RXCLK

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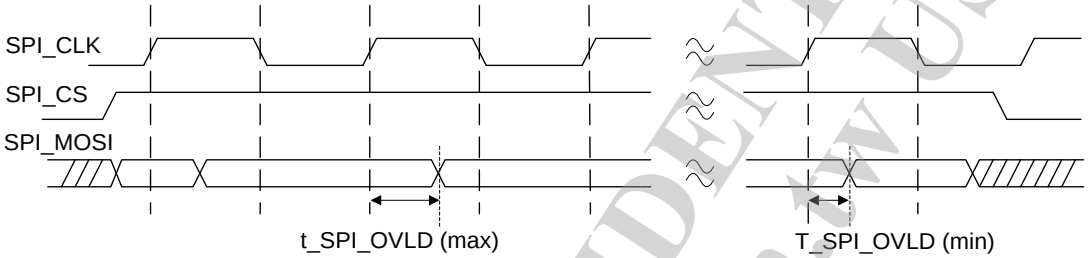
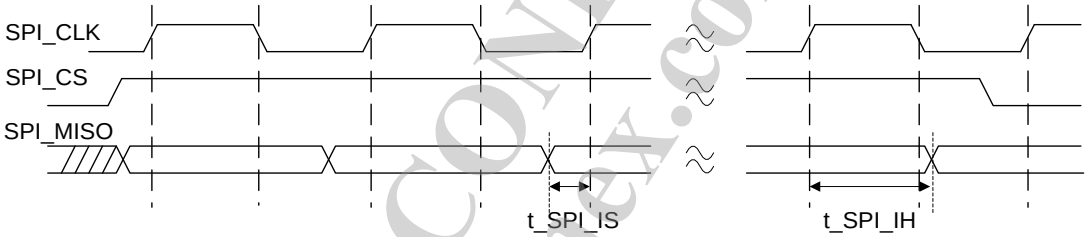
3.7.4 SPI Interface

Write operation (driven by clock rising edge)



Read operation (Driven by clock rising edge (slave-device) and latched by clock rising edge)



NOTE: 1) SPI_CLK is a gated clock.
2) SPI_CS is controlled by software

Figure 3-3 SPI Timing

Table 3-11 SPI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_SPI_IS	Setup time for SPI input	6.0	-	ns	
t_SPI_IH	Hold time for SPI input	-1.0	-	ns	
t_SPI_OVLD	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5 pF

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3.7.5 I2S Interface

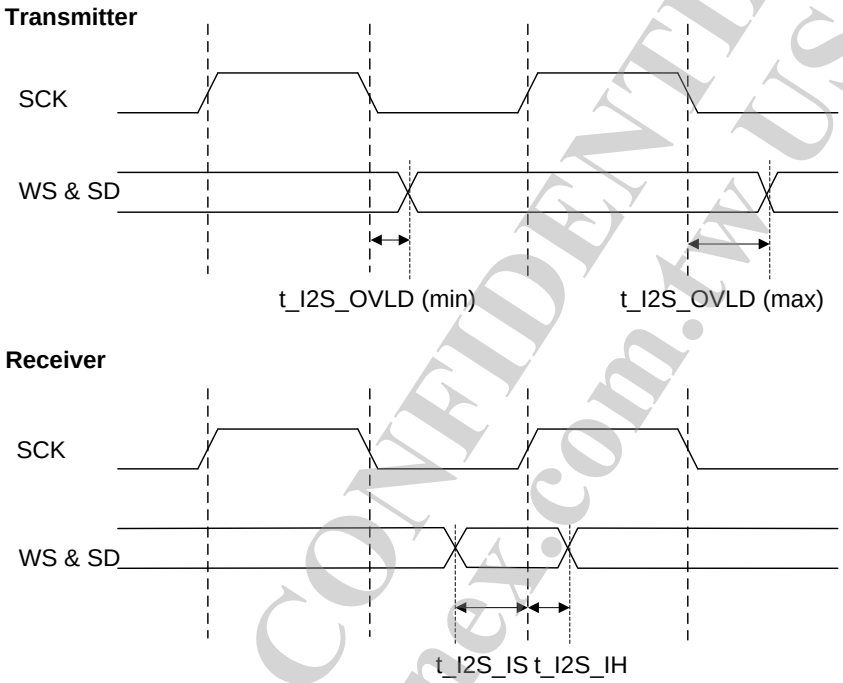

Figure 3-4 I2S Timing

Table 3-12 I2S Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_I2S_IS	Setup time for I2S input (data & WS)	3.5	-	ns	
t_I2S_IH	Hold time for I2S input (data & WS)	0.5	-	ns	
t_I2S_OVLD	I2S_CLK to I2S output (data & WS) valid	2.5	10.0	ns	output load: 5 pF

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3.7.6 PCM Interface

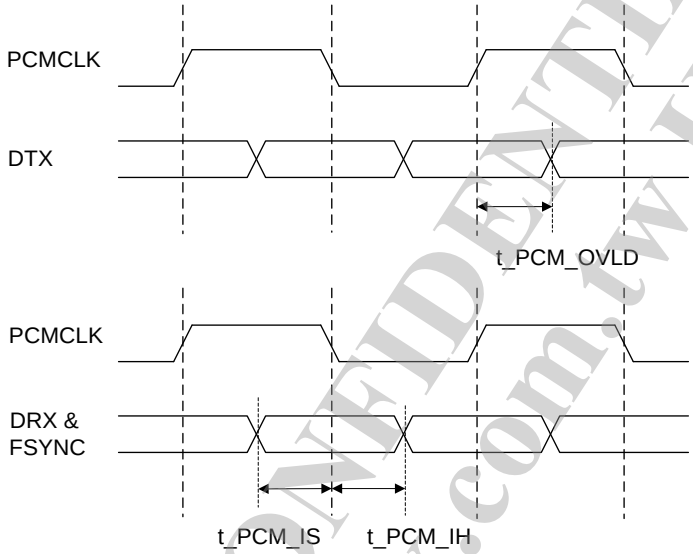

Figure 3-5 PCM Timing

Table 3-13 PCM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_PCM_IS	Setup time for PCM input to PCM_CLK fall	3.0	-	ns	
t_PCM_IH	Hold time for PCM input to PCM_CLK fall	1.0	-	ns	
t_PCM_OVLD	PCM_CLK rise to PCM output valid	10.0	35.0	ns	output load: 5 pF

3.7.7 I2C Interface

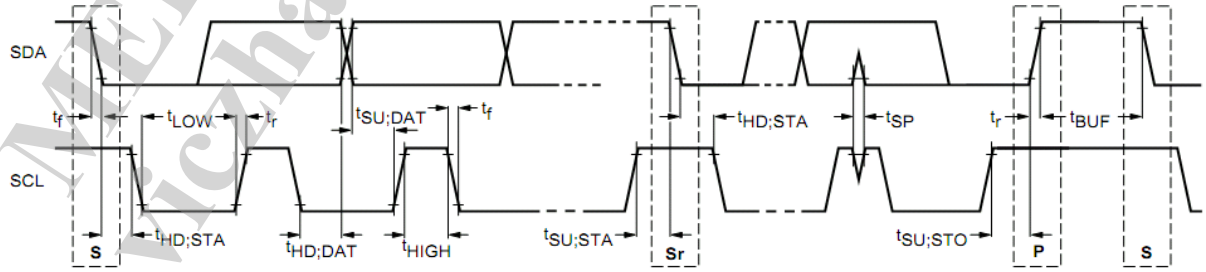

Figure 3-6 I2C Timing

Table 3-14 I2C Interface Diagram Key

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Symbol	Description	Min	Max	Unit	Remark
fSCL	SCL clock frequency	0	400	kHz	
tBUF	Bus free time between a STOP and START condition	1.3	-	us	
tHD	Hold time (repeated) START condition. After this period, the first clock pulse is generated	-	-	us	
tLOW	LOW period of the SCL clock	1.3	-	us	
tHIGH	HIGH period of the SCL clock	0.6		us	
tSU:STA	Setup time for a repeated START condition	0.6	-	us	
THD:DAT	Data hold time:	-	-	us	
tSU:DAT	Data setup time	100	-	ns	
tr	Rise time of both SDA and SCL signals	20	300	ns	
tf	Fall time of both SDA and SCL signals	20	300	ns	
tSU:STO	Setup time for STOP condition	0.6	-	us	

3.7.8 SDIO Interface

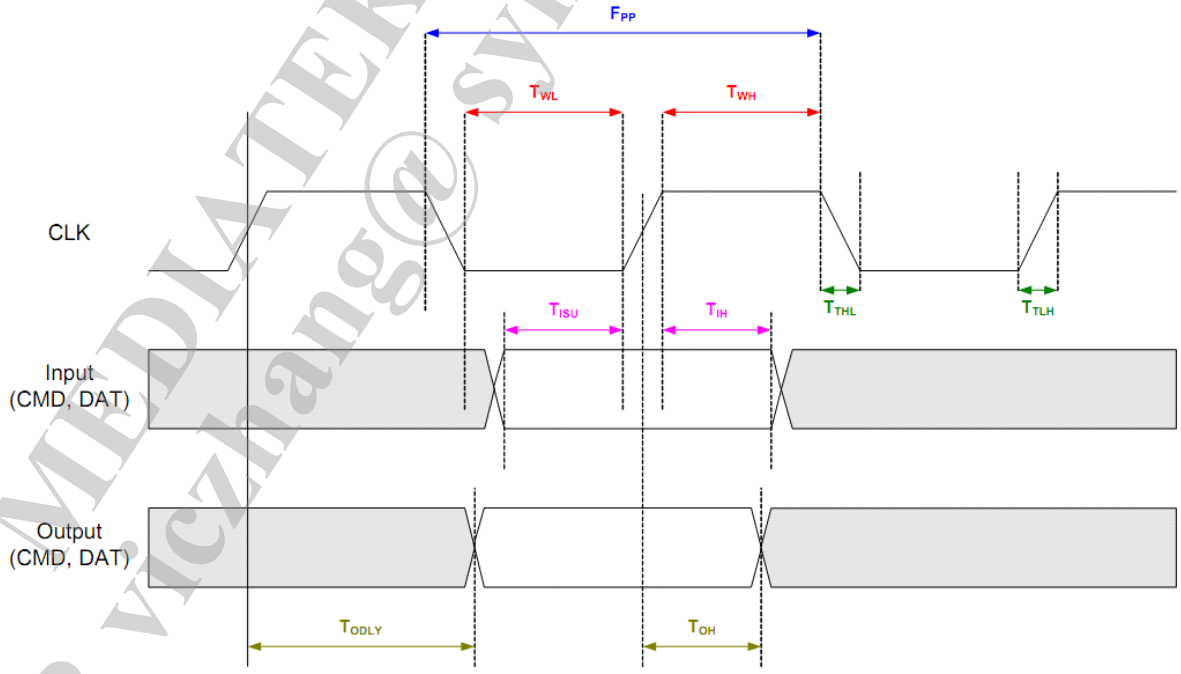

Figure 3-7 SDIO Timing

Table 3-15 SDIO Interface Diagram Key

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Symbol	Description	Min	Max	Unit	Remark
fPP	Clock frequency data transfer mode	0	50	MHz	
tWL	Clock low	7		ns	
tWH	Clock high	7		ns	
tTLH	Clock rise		3	ns	
tTHL	Clock fll		3	ns	
tISU	Input setup	6		ns	
tIH	Input hold	2		ns	
tOH	Output hold	2.5		ns	
tO_DLY(max)	Output dellay time	0	14	ns	

3.7.9 NAND Flash Interface (Samsung Compatible Device)

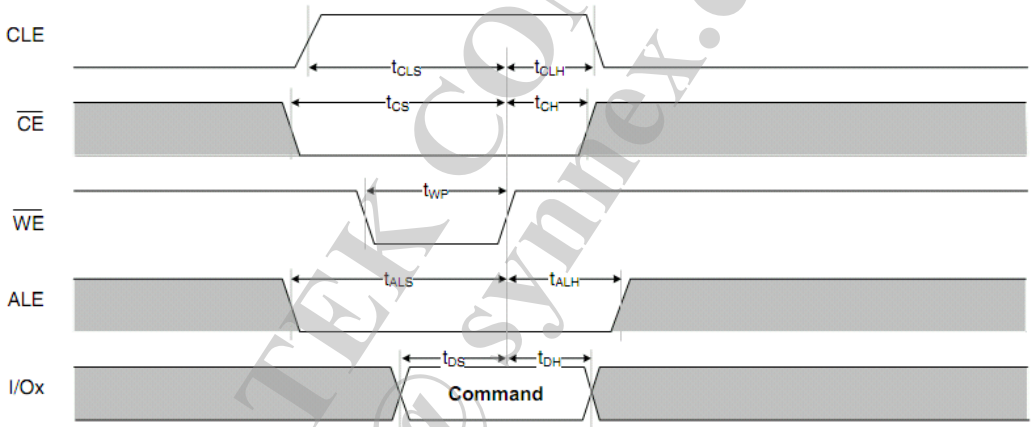

Figure 3-8 NAND Flash Command Timing

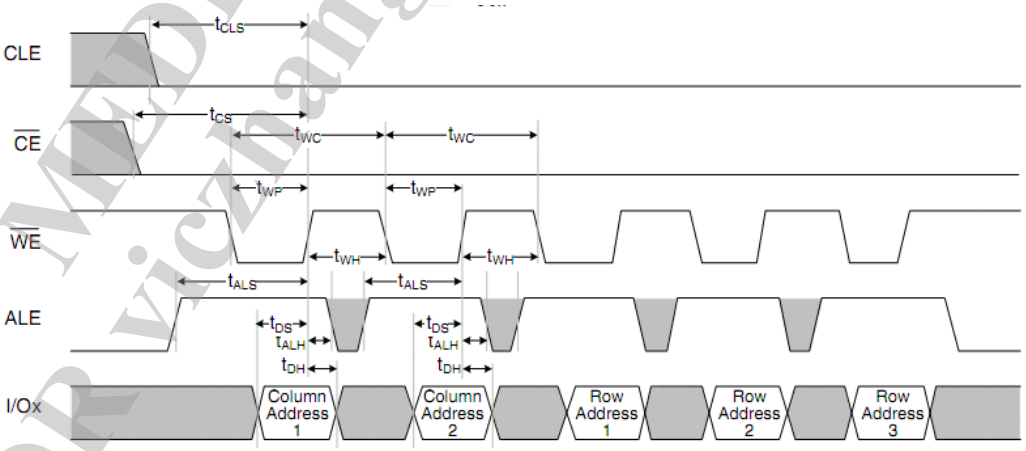

Figure 3-9 NAND Flash Address Latch Timing

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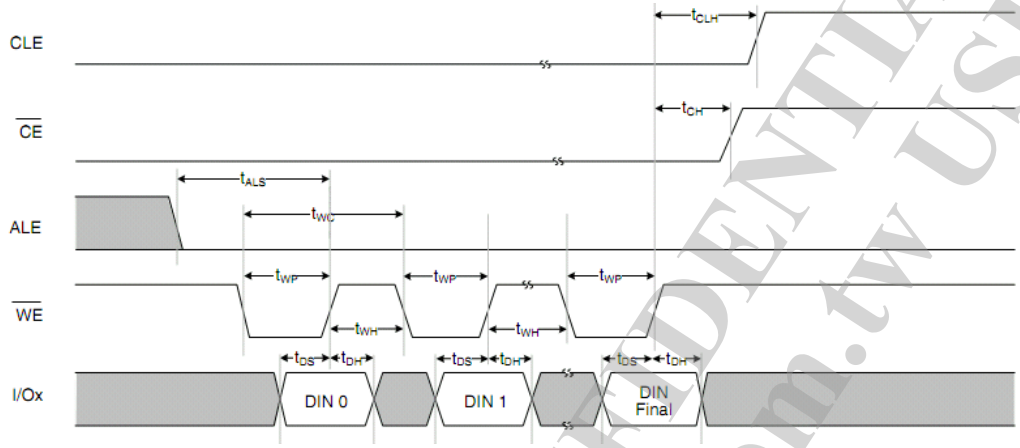

Figure 3-10 NAND Flash Write Timing

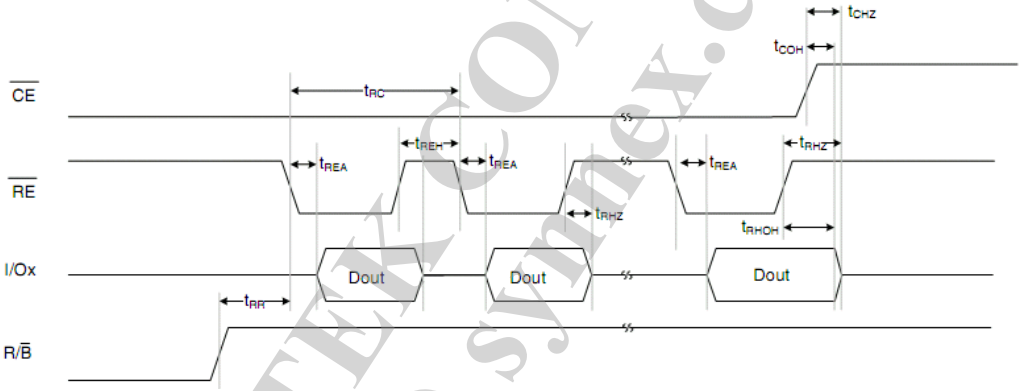

Figure 3-11 NAND Flash Read Timing

Table 3-16 NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCLS	CLE setup time	12	-	ns	
tCLH	CLE hold time	5		ns	
tCS	CE setup time	20		ns	
tCH	CE hold time	5		ns	
tWP	WE pulse width	12		ns	
tALS	ALE setup time	12		ns	
tALH	ALE hold time	5		ns	
tDS	Data setup time	12		ns	
tDH	Data hold time	5		ns	
tWC	Write cycle time	25		ns	

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Symbol	Description	Min	Max	Unit	Remark
tWH	WE high hold time	10		ns	

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3.8 Power On Sequence

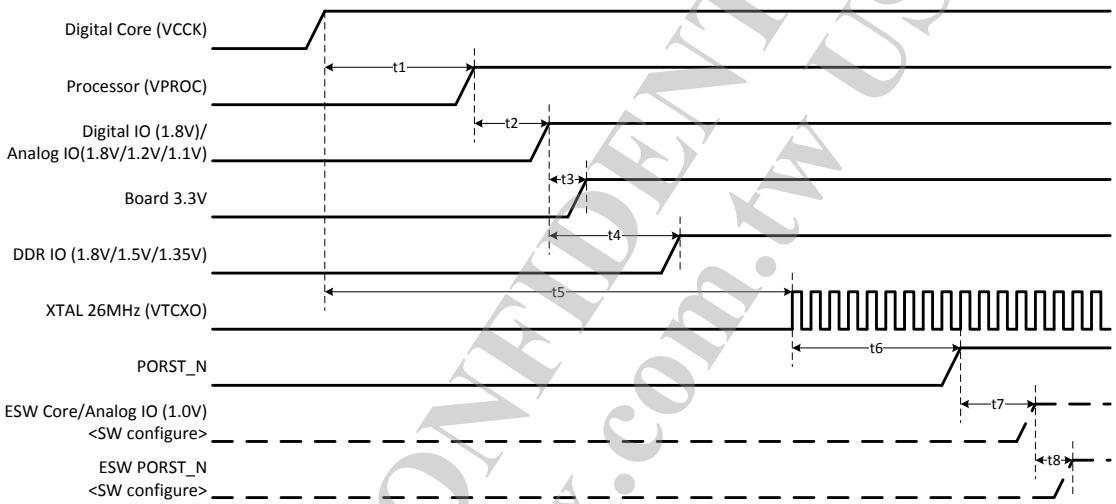

Figure 3-12 Power ON Sequence

Table 3-17 Power ON Sequence Diagram Key

Symbol	Description	Min	Max	Unit
t1	Digital core power on to processer(CA7) power on	8	10	ms
t2	Processor(CA7) power on to digital IO(1.8V) and analog IO(1.8V/1.2V/1.1V) power on	2	4	ms
t3	Digital IO power(1.8V) on to board 3.3V power on	2	4	ms
t4	Digital IO power(1.8V) on to DDR IO(1.8V/1.5V/1.35V) power on	6	8	ms
t5	Digital core power on to XTAL start	0	30	ms
t6	XTAL start to PORST_N de-assertion	41	164	ms
t7	PORST_N de-assertion to SW configure ESW(Ethernet Switch) core power on	-	-	ms
t8	ESW core power on to ESW PORST_N de-assertion	200	-	ms

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4 Package Information

4.1 Dimensions - FBGA (21 x 21mm)

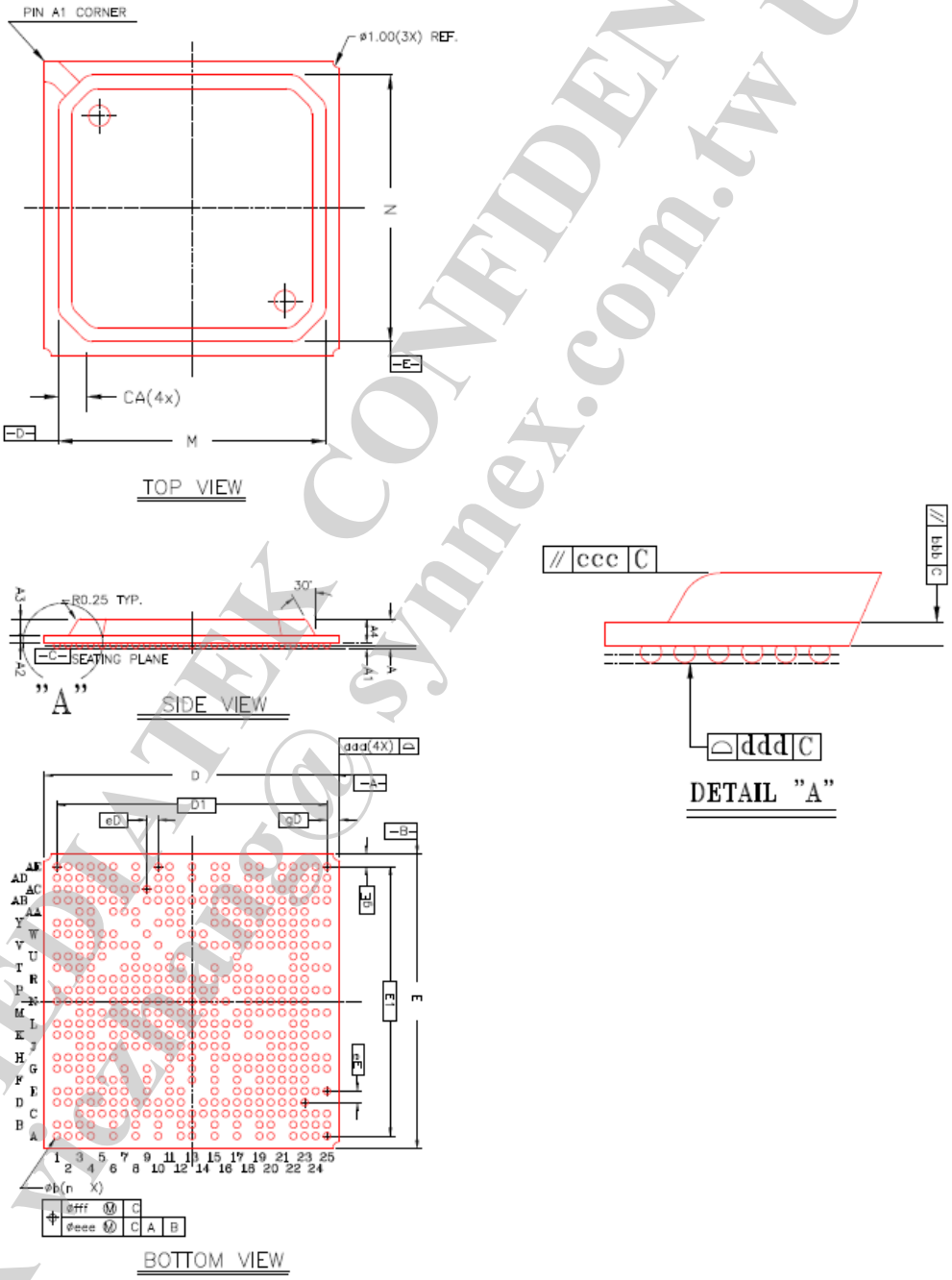

Figure 4-1 Package Dimension

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4.1.1 Diagram Key

Table 4-1 Package Diagram Key

Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			FBGA		
Body Size	X	D	20.85	21	21.15
	Y	E	20.85	21	21.15
Ball Pitch	X	eD		0.80	
	Y	eE		0.80	
Mold Thickness		A3		1.17 Ref.	
Substrate Thickness		A2		0.56 Ref.	
Substrate+Mold Thickness		A4	1.66	1.73	1.80
Total Thickness		A	2.00	2.13	2.26
Ball Diameter				0.50	
Ball Stand Off		A1	0.35	0.40	0.45
Ball Width		b	0.45	0.50	0.55
Mold Area	X	M		19.00	
	Y	N		19.00	
Chamfer		CA		2.00*45°	
Package Edge Tolerance		aaa		0.15	
Substrate Flatness		bbb		0.10	
Mold Flatness		ccc		0.20	
Coplanarity		ddd		0.15	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.08	
Ball Count		n		486	
Edge Ball Center to Center	X	D1		19.20	
	Y	E1		19.20	
Edge Ball Center to Package Edge	X	gD		0.90	
	Y	gE		0.90	

NOTE:

1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: bbb, ddd.
5. The pattern of pin 1 fiducial is for reference only.

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4.2 Reflow Profile Guideline

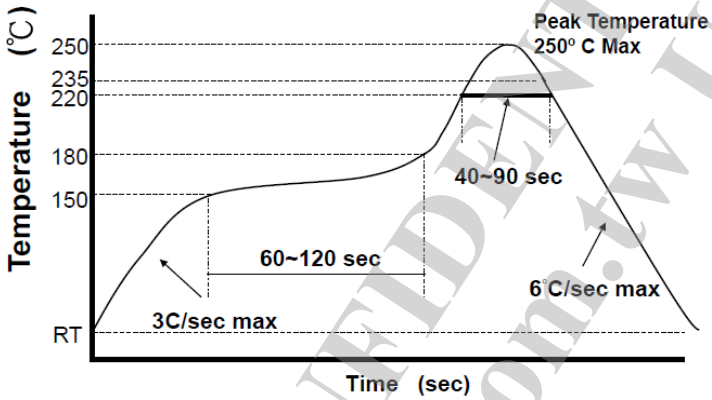

Figure 4-2 Reflow profile

Notes:

1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

4.3 Top Marking

MT7623AI: Part number
YYWW: Date code
####: Internal control code
LLLLLLLLL: Lot number
".": Pin #1 dot

Figure 4-3 Top marking

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4.4 Ordering Information

Part Number	Package (Green/RoHS Compliant)
MT7623AI	21 x 21mm, 486-balls FBGA

Note: a heat sink is required in max ambient temperature.

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