MT7530 Giga Switch Programming Guide

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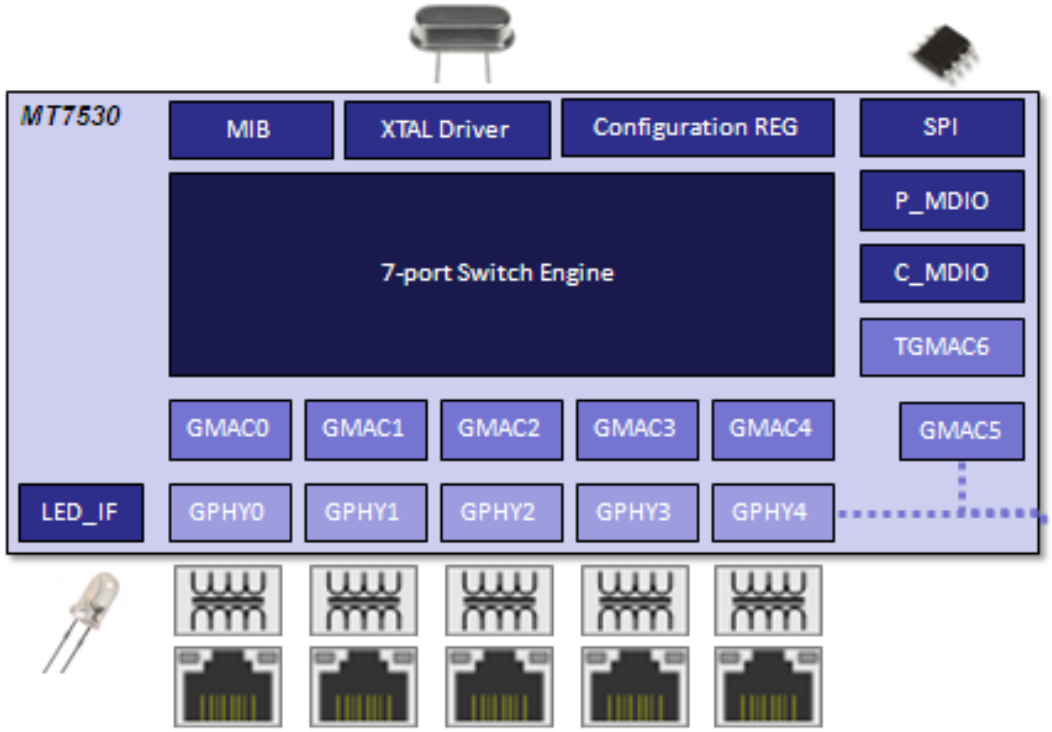
Document Revision History

Revision	Date	Author	Note
V00	**2013/07/10**	**JayYC**	**Initial release**
V01	**2013/09/10**	**JayYC**	**Draft version**
V02	**2014/01/29**	**JayYC**	1. Add Broadcast Storm suppression 2. Add TrTCM setting 3. Add QoS 4. Add ingress & egress rate control
V03	**2014/04/25**	**JayYC**	
V04,V05	**2014/08/11**	**JayYC**	**Update switch configuration** **DSCP**
V06	**2014/08/18**	**JayYC**	**Loop detection**
V07	**2014/10/12**	**JayYC**	**VLAN ID translation**

Table of Content

Introduction

MT7530 including 7-port Gigabit Ethernet MAC and 5-port Gigabit Ethernet PHY for several applications, such as xDSL , xPON and Wifi router. It complies with IEEE 802.3az for Energy Efficient Ethernet and cable-length /link down power saving mode. Please refer to the below figure to know the construct of MT7530.



Mode setting

The register 0x 7800 is hardware trap, it is made when power on (define by boot-strap resistance). You can change it by writing 0x7804. Finally, the system would active according ox7804 not 0x7800. Some registers of 0x7800 cannot be changed. For detail, please check the switch register map. You should check it bit by bit.

00007800 HWTRAP Hardware Trap Status Register 01007FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ht_loopdet_dis	ht_p5_intf_sel	ht_smi_addr		ht_xtal_fsel		ht_p6_intf_dis	ht_p5_intf_mode	ht_p5_intf_dis	ht_c_mdio_bps_n	ht_eeprom_en	ht_chip_mode			
Type		RO	RO	RO		RO		RO	RO	RO	RO	RO	RO			
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

If you want to change 0x7804, you need to set bit 16 as 1 of 0x7804 first.

00007804 MHWTRAP Modified Hardware Trap Status Register 0100000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												csr_p5_phy0_sel				csr_chg_trap
Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_gsw_ck_sel	csr_loopdet_dis	csr_p5_intf_sel	csr_smi_addr		csr_xtal_fsel		csr_p6_intf_dis	csr_p5_intf_mode	csr_p5_intf_dis	csr_c_mdio_bps_n	csr_eeprom_en	csr_chip_mode			
Type	RW	RW	RW	RO		RO		RW	RW	RW	RW	RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
20	csr_p5_phy0_sel	**When p5_intf_sel == 1'b0, the external device will be connected to** 1'b0: GPHY4 1'b1: GPHY0
16	csr_chg_trap	**Change HW-TRAP setting** 1'b1: Change 1'b0: Use default HW-TRAP setting
15	csr_gsw_ck_sel	**Control GSW_CK (if csr_chg_trap == 1)** 1'b0: 500MHz 1'b1: 200MHz
14	csr_loopdet_dis	**Hardware Loop Detection Disable (if csr_chg_trap == 1)** 1'b0: Enable 1'b1: Disable
13	csr_p5_intf_sel	**Port 5 Interface Selection (if csr_chg_trap == 1)** 1'b1: P5 Interface connects to GMAC5 1'b0: P5 Interface connects to GePHY4 or GePHY0 (depends on csr_p5_phy0_sel)
12:11	csr_smi_addr	**csr_smi_addr is equal to ht_smi_addr[1:0] (offset: 0x7800, bit 12~11) since this hardware trap cannot be modified by software.**
10:9	csr_xtal_fsel	**csr_xtal_fsel is equal to ht_xtal_fsel[1:0](offset: 0x7800, bit 10~9)since this hardware trap cannot be modified by software.**
8	csr_p6_intf_dis	**From hw_trap[8]** Port 6 Interface Disable (if csr_chg_trap == 1) 1'b0: Enable

		1'b1: Disable
7	csr_p5_intf_mode	**Port 5 Interface Mode (if csr_chg_trap == 1)** 1'b0: GMII/MII 1'b1: RGMII
6	csr_p5_intf_dis	**Port 5 Interface Disable (if csr_chg_trap == 1)** 1'b1: Disable 1'b0: Enable
5	csr_c_mdio_bps_n	**Directly access phy mdc (if csr_chg_trap==1)** 0: Directly access PHY registers via C_MDC/C_MDIO 1: Indirectly access PHY registers
4	csr_eeprom_en	**csr_eeprom_en is equal to ht_eeprom_en (offset: 0x7800, bit 4) since this hardware trap cannot be modified by software.**
3:0	csr_chip_mode	**csr_chip_mode is equal to ht_chip_mode[3:0] (offset: 0x7800, bit 3~0) since this hardware trap cannot be modified by software.**

Please also check the detail hardware strapping of MT7530.

Pin Name	Type	Pin Number	Description
P4_LED_0 P3_LED_0	I/O	99 102	Crystal clock frequency selection {P4_LED_0, P3_LED_0} signals are used to control the crystal clock input frequency to XO and XI. 00: Reserved. 01: 20MHz 10: 40MHz 11: 25MHz (default)
P3_LED_2 P3_LED_1	I/O	100 101	SMI Address selection {P3_LED_2, P3_LED_1} signals are used to define decoded Serial Management Interface(SMI) addresses of C_MDC/C_MDIO for command registers access 00 : Use 7 to 12 SMI addresses 01 : Use 15 to 20 SMI addresses 10 : Use 23 to 28 SMI addresses 11 : Use 31 and 0 to 4 SMI addresses (default)
P1_LED_1	I/O	107	SMI Access control 0: PHY access mode 0 1: PHY access mode 1 (default)
P1_LED_2	I/O	106	P5 Interface Disable 0: Enable P5 IO 1: Disable P5 IO (default)
P2_LED_1	I/O	104	P5 Interface Mode 0: GMII or MII mode 1: RGMII mode (default)
P4_LED_1	I/O	98	P5 Interface Selection 0: P5 IO is connected to GPHY4 1: P5 IO is connected to GMAC5 (default)
P2_LED_2	I/O	103	P6 Interface Disable

Pin Name	Type	Pin Number	Description
			0: Enable P6 IO 1: Disable P6 IO (default)
P0_LED_2	I/O	109	EEPROM Auto Initialization 0: Disable EEPROM auto initialization 1: Enable EEPROM auto initialization (default)
P4_LED_2	I/O	97	Loop Detection Alarm 0: Enable loop detection 1: Disable loop detection (default)

*Note 1: We would suggest that SMI address of MT7530 is 5'b11111. If not, you need to change the driver of MT7530.

Reset

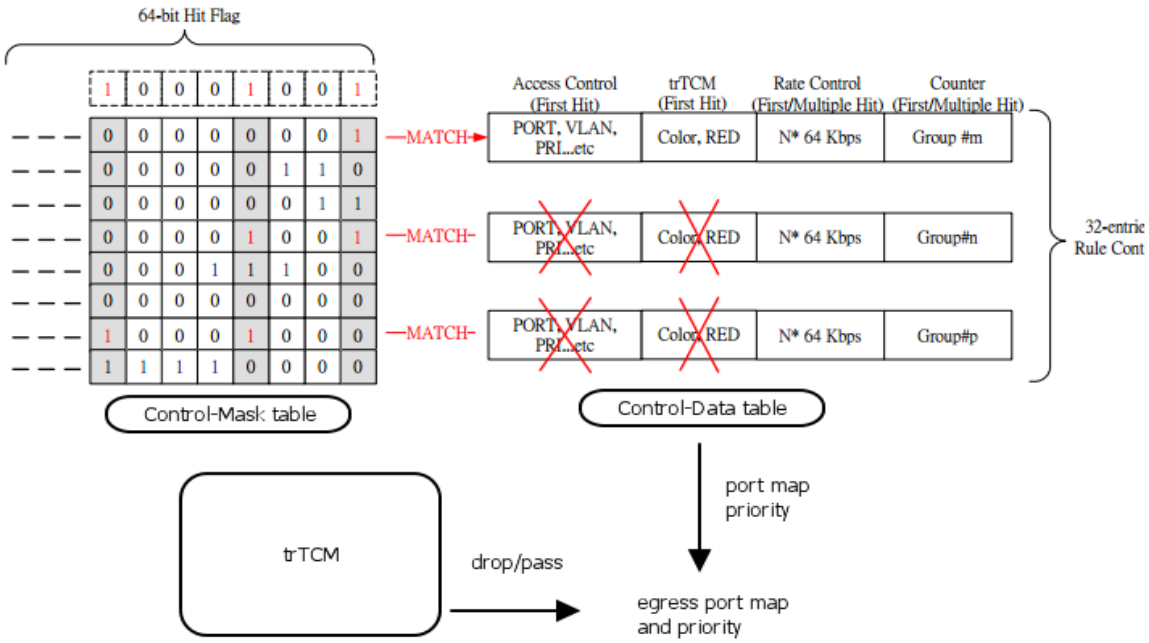
Check the Register 0x7000 if you want to do the software reset to switch or PHY. Usually, we would set 0x7000 as 0x3 for re-start switch.

00007000 **SYS_CTRL** **System Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ACL_TAB_INIT	MAC_TAB_INIT	VLAN_TAB_INIT				BMU_MEM_INIT
Type										RO	RO	RO				RO
Reset										0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRTCM_BIST_STS	MASK_BIST_STS	CTRL_BIST_STS	ADDR_BIST_STS	VLN_BIST_STS	MIB_BIST_STS	PB_BIST_STS	PL_BIST_STS	FL_BIST_STS	MBIST_CMP	MBIST_EN		SW_PHY_RST	SW_SYS_RST	SW_REG_RST
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW		R/W/SC	R/W/SC	R/W/SC
Reset		0	0	0	0	0	0	0	0	0	0	0		0	0	0

Access control list (ACL)

ACL Rule table is implemented along with packet parser. For the incoming packet, 2-bytes packet content will be filtered sequentially and compared with 64 patterns in the ACL rule table. When one pattern is hit, the corresponding rule flag will be set. After the whole packet is done, the final 64-bits rule flag will be sent to the ACL look-up engine to get the corresponding rule control. MT7530 can support up to 32 entries ACL rules.



Take port 0 for example:
0x2004 ff0400 //enable ACL of port 0, this setting is by per-port.

After enable ACL, you need to setup ACL hit pattern. We would check the VLAN for example here.

First:

Set ACL pattern:

0x94 ffff8100 //"ffff" mean compare 2-bytes payload and need match 0x8100.
0x98 0008ff0c //ACL pattern enable, MAC header. P0 to P6. Offset 12byte.
0x90 80005001 //bit [15:12]: 4'b0101:
//Write the specific ACL Table entry. It is 1st rule.

Second:

Set ACL mask:

0x94 00000021 //0x21 = 0010.0001 . Active 1st and 6th rule.
0x98 00000000
0x90 80009002 //bit [15:12]: 4'b1001: Write the specific 3rd ACL Mask entry
//use mask can enable many rules at the same time

Or set ACL mask (another sample):

0x94 00000004 //0x4= 0100. Active 3th rule.
0x98 80000000 //0x80000000= 1000.0000.0000.0000 . Active 63th rule.
0x90 8000903F //bit [15:12]: 4'b1001: Write the specific 64th ACL Mask entry
//The first Mask start from "0", so the 64th mask entry is 0x3f(63).

Setup the ACL action:

0x94 18000080 //Refer to 0x0094 (ACL rule control). This is used for drop packet.
0x98 00000000
0x90 8000b001 //bit [15:12]: 4'b1011: Write ACL rule control entry, Action for 1st rule.
//The first rule entry need to start from "1".

Destination Address	Source Address	VLAN TAG	Type / Length	Payload	FCS
6 byte	6 byte	4byte	2byte	1500 byte	4 byte

00002004 PCR **Port Control of P0** **00FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000090 VTCR **VLAN Table Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_INVLD
Type	W1C	DC														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BUSY	**VLAN Table Is Busy** SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.
30:17	REV0	**Reserved**
16	IDX_INVLD	**Entry is not Valid** This index for the access control is out of the valid index.
15:12	FUNC	**Access Control Function** Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits . 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry.

		4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved
11:0	VID	**1. VLAN ID Number: 0x0 to 0x1F (16)** 2. ACL table index: 0x0 to 0x3F (64) 3. ACL mask control: 0x0 to 0x3F (32 or 64)

0x94

(ACL Rule Table)

Bits	Type	Name	Description	Initial value
31:16	RW	BIT_MASK	**Comparison Pattern Mask**	0x0
15:0	RW	CMP_PAT	**Comparison Pattern**	0x0

(ACL Rule Mask)

Bits	Type	Name	Description	Initial value
31:0	RW	ACL_MASK	**ACL Mask[31:0]**	0x0

(ACL Rule Control)

Bits	Type	Name	Description	Initial value
31:30	-	-	**Reserved**	0x0
29	RW	ACL_MANG	**Management Frame Attribute**	0x0
28	RW	INT_EN	**Interrupt Enable**	0x0
27	RW	ACL_CNT_EN	**Enable ACL Hit Count**	0x0
26:24	RW	CNT_IDX	**Counter Group Index**	0x0
23	RW	VLAN_PORT_EN	**Swap VLAN Member**	0x0
22	RW	DA_SWAP	**Multicast MAC Address Swap**	0x0
21	RW	SA_SWAP	**Source MAC Address Swap**	0x0
20	RW	PPP_RM	**PPPoE Header Removal**	0x0
19	RW	LKY_VLAN	**Leaky VLAN**	0x0
18:16	RW	EG_TAG	**Egress VLAN Tag Attribute**	0x0
15:8	RW	PORT	**Destination Port / VLAN Member**	0x0
7	RW	PORT_EN	**Force Destination port**	0x0
6:4	RW	PRI_USER	**User Priority from ACL**	0x0
3	RW	MIR_EN	**Frame Copy to Mirror Port**	0x0
2:0	RW	PORT_FW	**Frame TO_CPU Forwarding**	0x0

0x98

(ACL Rule Table)

Bits	Type	Name	Description	Initial value
31:20	-	-	**Reserved**	0x0
19	RW	EN	**ACL Pattern Enable**	0x0
18:16	RW	OFST_TP	**Offset Range**	0x0
15:8	RW	SP	**Incoming Source Port Bit-map**	0x0
7:1	RW	WORD_OFST	**Word Offset**	0x0
0	RW	CMP_SEL	**Comparison mode selection**	0x0

Offset range table:

3'b000: MAC Header (inc. VLAN tags and Length/Type) (L2 Offset)
3'b001: L2 Payload (L2 Offset)
3'b010: IP Header (L3 Offset)
3'b011: IP Datagram (L3 Offset)
3'b100: TCP/UDP Header (L4 Offset)
3'b101: TCP/UDP Datagram (L4 Offset)
3'b110: IPv6 Header (L3 Offset)
3'b111: Reserved

(ACL Rule Mask)

Bits	Type	Name	Description	Initial value
31:0	RW	ACL_MASK	**ACL Mask[63:32]**	0x0

(ACL Rule Control)

Bits	Type	Name	Description	Initial value
31:24	RW	Reserved		0x0
23:19	RW	ACL_CLASS_IDX	**Class index for the 32-entries meter table**	0x0
18:17	RW	Reserved		0x0
16	RW	Reserved		0x0
15:14	RW	Reserved		0x0
13:11	RW	DROP_PCD_G	**User Defined Drop Precedence for Green color packet**	0x0
10:8	RW	DROP_PCD_Y	**User Defined Drop Precedence for Yellow color packet**	0x0
7:5	RW	DROP_PCD_R	**User Defined Drop Precedence for Red color packet**	0x0
4:2	RW	CLASS_SLR	**User Defined Class Selector**	0x0
1	RW	CLASS_SLR_SEL	**Select original class_selector value or ACL control table defined class selector value**	0x0
0	RW	DROP_PCD_SEL	**Select original drop precedence value or ACL control table defined drop Precedence value**	0x0

Broadcast Storm suppression

Broadcast Storm is commonly caused by faulty protocol implementations, undetected network loops, or faulty network equipment. Broadcast storms can cause significant disruption to the network. Broadcast control is possible by using filters or user-defined throttle settings that limit broadcast/multicast propagation to a certain rate.
MT7530 provide the per-port broadcast storm controller , loop detection and alarm signal to avoid it. Here we show the example to do the rate-base control of Broadcast storm.
Register 0x30c0 is used for setting the loop detection.

You may set it if Broadcast storm came from port 1:
Set 0x30c0 as 0x1f130000 //port 0 ~ port 4 enable LPDET,
Set 0x211c as 0xce030303 //set port 1 to detect broadcast storm according to rate-based , and drop the packet. The limit rate is around 3Mbps for 1000Mbps, 100Mbps and 10Mbps base.

Read 0x30c0 again to check the per-port LPDET_ALARMx information.

000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LPDET_EN6	LPDET_EN5	LPDET_EN4	LPDET_EN3	LPDET_EN2	LPDET_EN1	LPDET_EN0	LPDET_PERIOD_EN	LPDET_ALARM_EN	LPDET_PASS	LPDET_PERIOD	LPDET_LED_RATE	LPDET_THRESHOLD		
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_ST_LOOP	LPDET_ST_BCST	LPDET_TRAP_EN							LPDET_ALARM6	LPDET_ALARM5	LPDET_ALARM4	LPDET_ALARM3	LPDET_ALARM2	LPDET_ALARM1	LPDET_ALARM0
Type	RO	RO	RO							RO	RO	RO	RO	RO	RO	W1C
Reset	0	0	0							0	0	0	0	0	0	0

Bit(s)	Name	Description
30	LPDET_EN6	**Enable the loop detection ability of user port 6.** 0: Disable 1: Enable
29	LPDET_EN5	**Enable loop detection the ability of user port 5.** 0: Disable 1: Enable
28	LPDET_EN4	**Enable loop detection the ability of user port 4.** 0: Disable 1: Enable
27	LPDET_EN3	**Enable loop detection the ability of user port 3.** 0: Disable 1: Enable
26	LPDET_EN2	**Enable loop detection the ability of user port 2.** 0: Disable 1: Enable
25	LPDET_EN1	**Enable loop detection the ability of user port 1.** 0: Disable 1: Enable
24	LPDET_EN0	**Enable loop detection the ability of user port 0.** 0: Disable

		1: Enable
23	LPDET_PERIOD_EN	**The loop detection frame is triggered by a periodical timer or by broadcast storm.** 0: Broadcast mode 1: Periodical mode
22	LPDET_ALARM_EN	**Enable 2 kHz alarm output and per-port LED when loop is detected.** 0: Disable 1: Enable
21	LPDET_PASS	**Loop detection frame is blocked or passed to packet memory.** 0: Blocked 1: Pass
20	LPDET_PERIOD	**Interval of transmitting loop detection frame in Periodical mode.** 0: 125 us 1: 1000 ms
19	LPDET_LED_RATE	**LED blinking rate of per port when loop is detected.** 0: LED blinking at 2 Hz 1: LED blinking at 4 Hz
18:16	LPDET_THRESHOLD	**Number of missed loop detection frame before 2 kHz alarm is reset**
15	LPDET_ST_LOOP	**The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.** 0: Not in Loop state 1: Loop state
14	LPDET_ST_BCST	**The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.** 0: Not in BCST state 1: BCST state
13	LPDET_TRAP_EN	**Status of strap pin for loop detection** 0: Disabled 1: Enabled
6	LPDET_ALARM6	**The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
5	LPDET_ALARM5	**The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
4	LPDET_ALARM4	**The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
3	LPDET_ALARM3	**The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
2	LPDET_ALARM2	**The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
1	LPDET_ALARM1	**The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
0	LPDET_ALARM0	**The status of loop detected on port 0. This bit is cleared when it is written as 1.** 0: Not detected 1: Detected

0000201C **BSR** **Broadcast Storm Rate Control of P0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

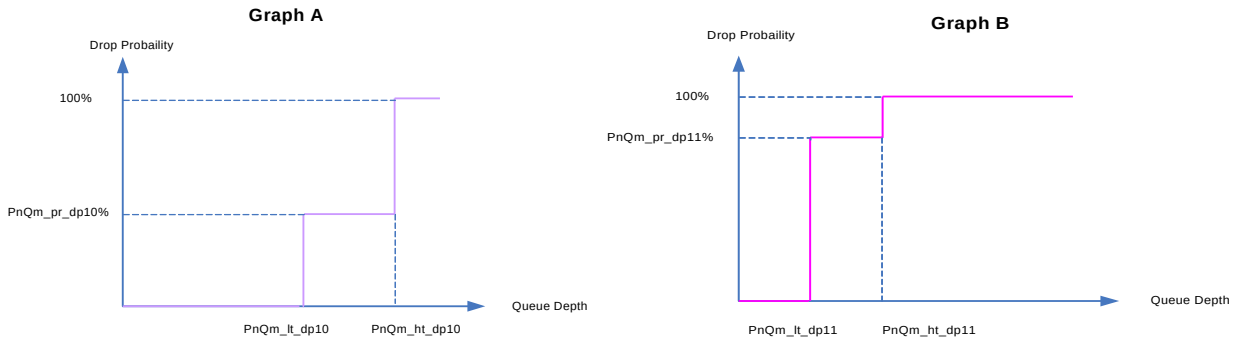
Drop Precedence control

The “Drop Precedence” is addon function for the Flow Control. The function can enable or disable. When an enqueue request is on, the control signals of the packet like as queue priority, drop precedence which are from ARL module will feed into Drop Precedence controller, the controller will check the queue depth and drop probability to

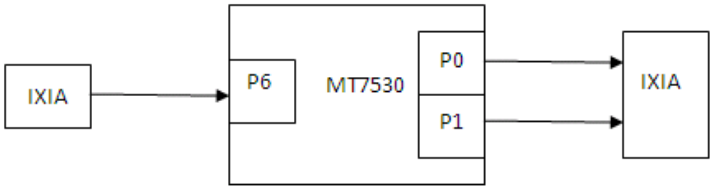
decide the packet will be dropped or not. Fin ally, it will feedback the “dp_packet_drop” signal to tell the Flow Control to drop the packet or not. The drop precedence of value is by user setting inthe ACL entry or trTCM engine.

The meaning of dorop precedence which is from ARL is
(a) 2’b00, 2’b01 : No drop.
(b) 2’b10 : The drop probability of the incoming packet is based on “Graph A” setting.
(c) 2’b11 : The drop probability of the incoming packet is based on “Graph B” setting.

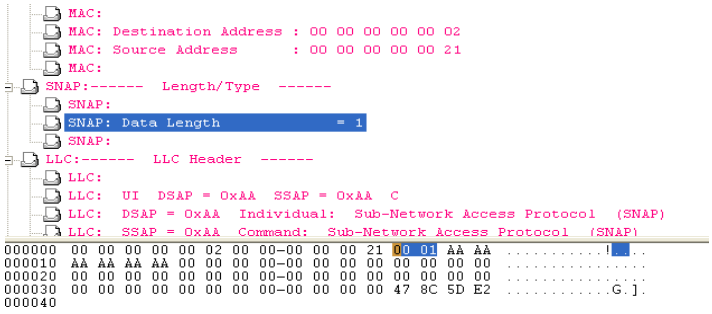
PnQm_pr_dp10/11 : Drop probability of Port n Queue m when drop precedence = 2’b10/2’b11.
PnQm_lt_dp10/11 : Low threshold of of Port n Queue m when drop precedence = 2’b10/2’b11.
PnQm_ht_dp10/11 : High threshold of of Port n Queue m when drop precedence = 2’b10/2’b11.



Here we show the test environment as below:



We would design one ACL to hit the”0x0001” in the data from port 6 to mark a color for it. And use DROP precedence at port 0.



;ACL port enable
ethphxcmd gsww 2604 00ff0403

```
;ACL entry
ethphxcmd gsww 0094 ffff0001        // 0xffff - compare 2-byte data
                                    // 0x0001- compare pattern should be as 0x0001

ethphxcmd gsww 0098 0008400c        // 0x000 MAC offset (bit 18:16)
                                    //0x8 – ACL pattern enable
                                    // 0x4 – incoming source port is port 6(bit 15:8)
                                    // 0xc –offset
ethphxcmdgsww 0090 80005000         //Write ACL table entry

ethphxcmd gsww 0094 00000001
ethphxcmd gsww 0098 00000000
ethphxcmd gsww 0090 80009000       //Write ACL mask

ethphxcmd gsww 0094 00000000
ethphxcmd gsww 0098 00060000       //mark as red
ethphxcmd gsww 0090 8000b000       //ACL rule control
```

- Set Drop precedence for Port 0 Q2

```
ethphxcmd gsww 180c 80000000  //enable drop precedence
ethphxcmd gsww 1814 80000000
ethphxcmd gsww 182c 011ff000     // Drop probability of P0 Q2
```

0x0098 (ACL Rule Control)

Bits	Type	Name	Description	Initial value
31:24	RW	Reserved		0x0
23:19	RW	ACL_CLASS_IDX	ACL Class index for the 32-entries meter table (TrTcm)	0x0
18:17	RW	ACL_ User defined color remark	00:default, 01:Green, 10:Yellow, 11:Red)	0x0
16	RW	Select Color	1: TrTcm 0: ACL	0x0
15:14	RW	Reserved		0x0
13:11	RW	DROP_PCD_G	User Defined Drop Precedence for Green	0x0
10:8	RW	DROP_PCD_Y	User Defined Drop Precedence for Yellow	0x0
7:5	RW	DROP_PCD_R	User Defined Drop Precedence for Red	0x0
4:2	RW	CLASS_SLR	User Defined Class Selector	0x0
1	RW	CLASS_SLR_SEL	Select ACL Defined Class Selector	0x0
0	RW	DROP_PCD_	Select ACL Defined Drop Precedence	0x0

		SEL		

0000180C MMDPR_10_Q0P0 Drop Precedence control 10 of Q0 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P0_DP_en					P0Q0_pr_dp10						P0Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp10[3:0]							P0Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P0_DP_en	**Enable Drop Precedence function of P0. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P0Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P0Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P0Q0_lt_dp10 <= queue depth < P0Q0_ht_dp10, the drop probability of incoming packet is based on the setting P0Q0_pr_dp10. 0: Disable 1: Enable
26:24	P0Q0_pr_dp10	**Drop probability of P0 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q0_ht_dp10	**High threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q0_lt_dp10	**Low threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001814 MMDPR_10_Q2P0 Drop Precedence control 10 of Q2 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q2_pr_dp10						P0Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q2_ht_dp10[3:0]							P0Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q2_pr_dp10	**Drop probability of P0 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q2_ht_dp10	**High threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q2_lt_dp10	**Low threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size**

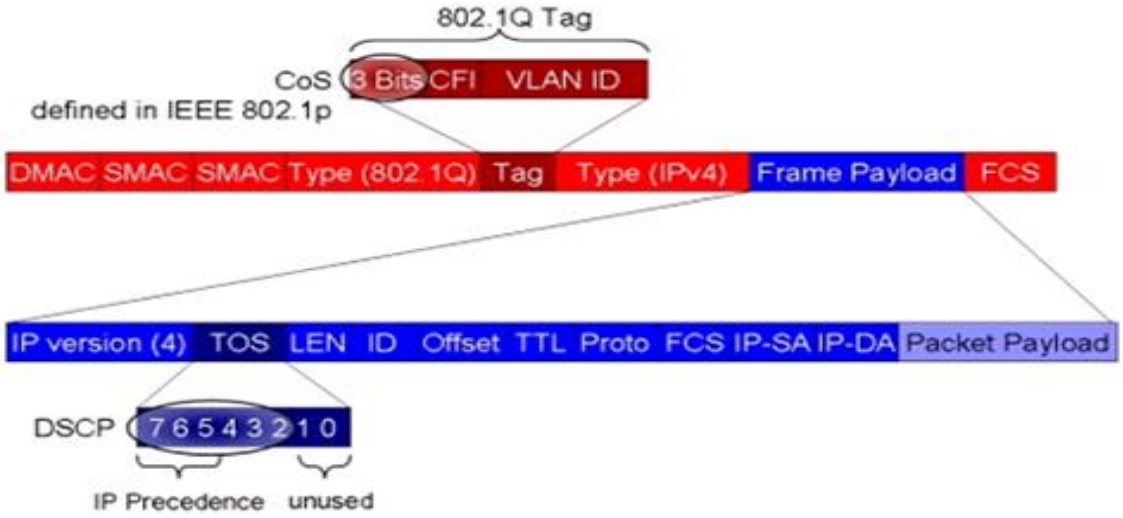
0000182C **MMDPR_11_Q0P0** **Drop Precedence control 11 of Q0 Port 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q0_pr_dp11						P0Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp11[3:0]							P0Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

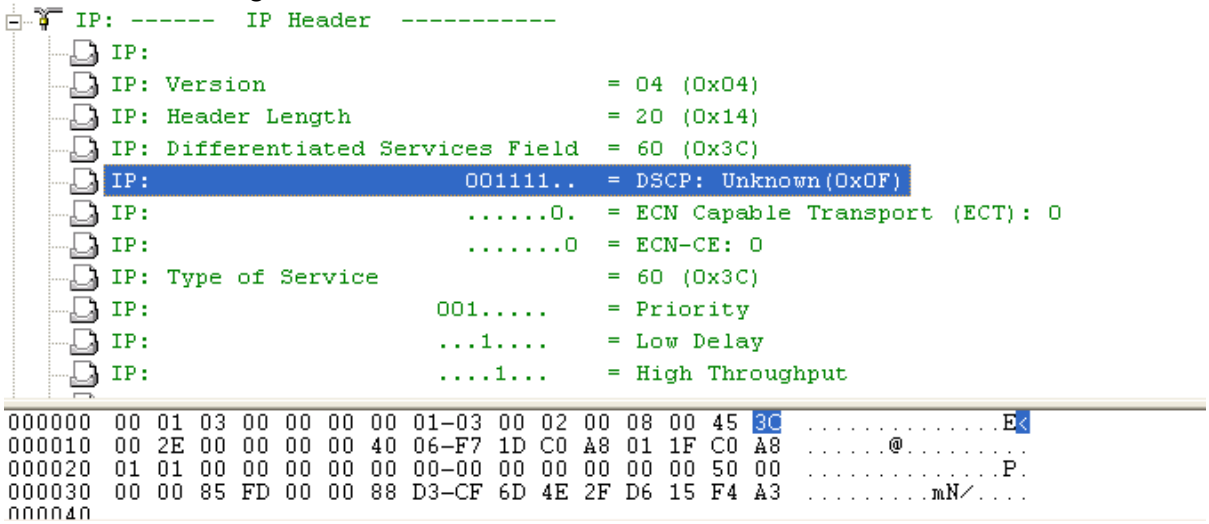
Bit(s)	Name	Description
26:24	P0Q0_pr_dp11	**Drop probability of P0 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q0_ht_dp11	**High threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q0_lt_dp11	**Low threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size**

DSCP

DSCP means Differentiated Services Code Point. DSCP use 6 bits and the range is between 0 to 63.



Refer to IXIA setting.



Follow the step to set the QoS of DSCP.

1. Disable flow control : 0x1fe0 bit 31 as 0
2. Set DSCP UPW as high: 0x44 bit 12 to bit 14 as 3'h111.
3. Set SP and WRR as you want.

Please also know the DSCP mapping table map as below.

Default User Priority Mapping Table from PEM1 ~ PEM4

User Priority	VLAN Pri	DSCP	LAN/WAN Queue	CPU Queue
3'h0	3'h0	6'h00	2'h1	3'h2
3'h1	3'h1	6'h08	2'h0	3'h0
3'h2	3'h2	6'h10	2'h0	3'h1
3'h3	3'h3	6'h18	2'h1	3'h3
3'h4	3'h4	6'h20	2'h2	3'h4
3'h5	3'h5	6'h28	2'h2	3'h5
3'h6	3'h6	6'h30	2'h3	3'h6
3'h7	3'h7	6'h38	2'h3	3'h7

EEPROM:

Before use EEPROM, please read 0x7800 bit 4 is 1 or not. If you want to use it, it should be as 1.
You need to use 0x7120 as the register for EEPROM programming. Here take the changing the port 0 register 4 for example.
Ethphxcmd gsww 7120 c0003075 // Must write the initial address of EEPROM as 7530
Ethphxcmd gsww 7120 c0021c70 // Use 0x701c to write PHY register, and write to address 2.
Ethphxcmd gsww 7120 c00405e1 // Write data 05e1 to address 4.
Ethphxcmd gsww 7120 c0068805
// Write data 8805 to address 6, the final data would be 880505e1

It means write 05E1 to register 4 of port 0.

00007120 EEPR_IND EEPROM INDIRECT ACCESS CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EP_IND_ACT	EP_IND_WR							EP_IND_ADDR							
Type	RW	RW							RW							
Reset	0	0							0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP_IND_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0000701C PHY_IAC PHY Indirect Access Control 00090000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_ACS_ST		MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		MDIO_ST	
Type	R/W/SC		RW					RW					RW		RW	
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDIO_RW_DATA															
Type	R/W/RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Write command example:

command	switch reg	EEPROM ADD					
ethphxcmd gsww	7120	c000	3	0	7	5	*chip ID, only need write at EEPROM reg 0.
ethphxcmd gsww	7120	c002	1	c	7	0	*MDIO register
ethphxcmd gsww	7120	c004	0	1	8	1	* data
ethphxcmd gsww	7120	c006	8	8	0	5	*command line

Read command example:

command	switch reg	EEPROM ADD					
ethphxcmd gsww	7120	c000	3	0	7	5	*chip ID, only need write at EEPROM reg 0.
ethphxcmd gsww	7120	c002	1	c	7	0	*MDIO register
ethphxcmd gsww	7120	c004	0	0	0	0	*command line
ethphxcmd gswr	7120						

Egress Rate limit control

There are many ways to do the rate control, like ACL rate control, ingress or egress rate control. If you want to use egress rate control, please disable flow control first to avoid the ingress congestion.

Set bit 31 of 0x1fe0 as 0 to disable global flow control.
Set 0x10e0 as 0x118 to include the IPG byte for egress rate control.
Here we show the sample for port 1 egress rate control.

egress rate	Reg 0x1140
10Mbps	0x0138898f
20Mbps	0x0271898f
30Mbps	0x03a9898f
40Mbps	0x04e2898f
100Mbps	0x0c35898f

000010E0 **GERLCR** **Global Egress Rate Limit Control Register** **00000104**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EGC_MFRM_EX	EGC_IPG_OP	EGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
9	EGC_MFRM_EX	**When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)** 0: Include management frames 1: Exclude management frames
8	EGC_IPG_OP	**Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	EGC_IPG_BYTE	**Egress Rate IPG Byte Count** Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC (default) 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble

00001040 **ERLCR_P0** **Egress Rate Limit Control Register of Port 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P0			EGC_RATE_CIR_16_P0	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0				EGC_TB_EN_P0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P0	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P0	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable

		1: Enable
12	EGC_RATE_CIR_16_P0	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P0 _EGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P0	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P 0_EGC_TB_CBS_P0	**Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

Flow control

You should set 0x1fe0 bit 31 as 1 for global flow control first.

We take Port 5 for example, if you want to disable TX and RX flow control, you should set the bit 5 and bit 4 of 0x3500 as 0. And read 4th and 5th bit of 0x3508 to check it works or not.

Please know we just discussed about the MAC layer flow control. You need to check the PHY ability if you use auto polling mode. Please check the blow table:

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR		
0	0	Don't care	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don't care	1	Don't care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_EN		FC_OFF2ON_OPT	FC_ON2OFF_OPT					FC_PORT_BLK_THD							
Type	RW		RW	RW					RW							
Reset	1		1	0					0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FC_FREE_BLK_HITHD								FC_FREE_BLK_LOTHD							
Type	RW								RW							
Reset	0	1	1	1	1	0	0	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
31	FC_EN	0: Disable flow control 1: Enable flow control
29	FC_OFF2ON_OPT	**Flow control assertion option** 0: Disable 1: Enable aggressive frame discard option in flow control transition from OFF to ON
28	FC_ON2OFF_OPT	**Flow control de-assertion option** 0: Disable 1: Enable aggressive frame discard option in flow control transition from ON to OFF
23:16	FC_PORT_BLK_THD	**Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)**
15:8	FC_FREE_BLK_HITHD	**High water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.**
7:0	FC_FREE_BLK_LOTHD	**Low water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.**

00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P5		EXT_PHY_P5	MAC_MODE_P5
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P5	MAC_TX_EN_P5	MAC_RX_EN_P5		MAC_PRE_P5		BKOFF_EN_P5	BACKPR_EN_P5	FORCE_EEE1G_P5	FORCE_EEE100_P5	FORCE_RX_FC_P5	FORCE_TX_FC_P5	FORCE_SPD_P5		FORCE_DPX_P5	FORCE_LNK_P5
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

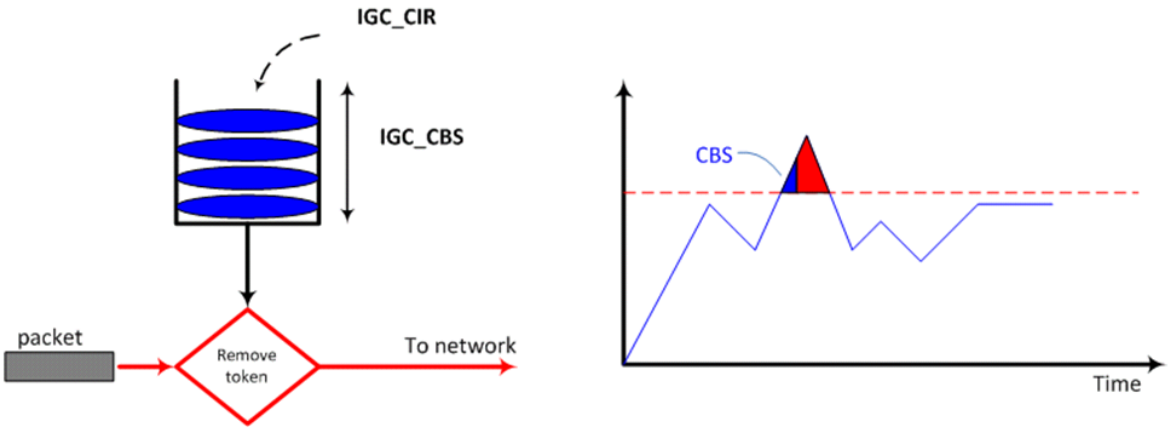
00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5		MAC_DPX_STS_P5	MAC_LNK_STS_P5
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P5	**PORT 5 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P5	**PORT 5 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P5	**PORT 5 RX XFC Status. Port 5 Rx flow control status** 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P5	**PORT 5 TX XFC Status** PORT 5 TX flow control status 0: Disabled. 1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P5	**PORT 5 Speed [1:0] Status** Current speed of PORT 5 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P5	**PORT 5 duplex Status** Current duplex mode of port 5 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P5	**Port 5 Link Up Status. Link up status of PORT 5.** 0: Link Down 1: Link Up

Ingress rate control

Ingress rate control is one of basic rate control. We cannot limit the rate of physical transmission line, but we can limit the resources of packet process rate.
Refer to the below to know the behavior of ingress rate control:



-Each interval of time (programmable) H/W fill IGC_CIR bit token to bucket.
-H/W remove token (equal to packet size) when there is packet income.
-if remain token > packet, the packet can pass to network otherwise will drop packet.
-A bucket with CBS sizes allow some burst traffic pass switch.

For example, to set the ingress rate as 1000kbps
EGC_TBEN = 1
EGC_CIR = 1000K/32K = 31 = 0x1f
EGC_TB_T = ¼ ms

To avoid the inter-fame gap effect, please set 0x1ff0 as 0x00110118
We provide some reference data to do the rate control. For port 1, please set the register 0x1800.

Ingress CIR	Reg 0x1800
10Mbps	0x0138898f
20Mbps	0x0271898f
30Mbps	0x03a9898f
40Mbps	0x04e2898f
100Mbps	0x0c35898f

00001FF0 **GIRLCR** **Global Ingress Rate Limit Control Register** **00110104**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IGC_FC_OFF_THD				IGC_FC_DROP_THD			
Type									RW				RW			
Reset									0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IGC_MFRM_EX	IGC_IPG_OP	IGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
23:20	IGC_FC_OFF_THD	**Ingress Rate Limit Pause-Off Threshold** Pause-off frame is sent when the ingress token bucket is higher than pause-off threshold. Threshold = max_bucket_size >> igc_fc_off_thd
19:16	IGC_FC_DROP_THD	**Ingress Rate Limit Drop Threshold** If Port Flow Control and rate limit control is enabled, frame is drop when the ingress token bucket is less than drop threshold. Threshold = -(max_bucket_size >> igc_fc_drop_thd)
9	IGC_MFRM_EX	**Ingress Rate Excludes Management Frames** Management frames will be ignored by rate limit. (management frame type is set by ARL registers) 0: Include management frames 1: Exclude management frames
8	IGC_IPG_OP	**Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	IGC_IPG_BYTE	**Ingress Rate IPG Byte Count** Byte count should be added while calculating the rate limit 8'h4: add 4 byte CRC (byte rate calculation) 8'h18: add 4 byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation)

00001800 **IRLCR_P0** **Ingress Rate Limit Control Register of Port 0** **00000000**

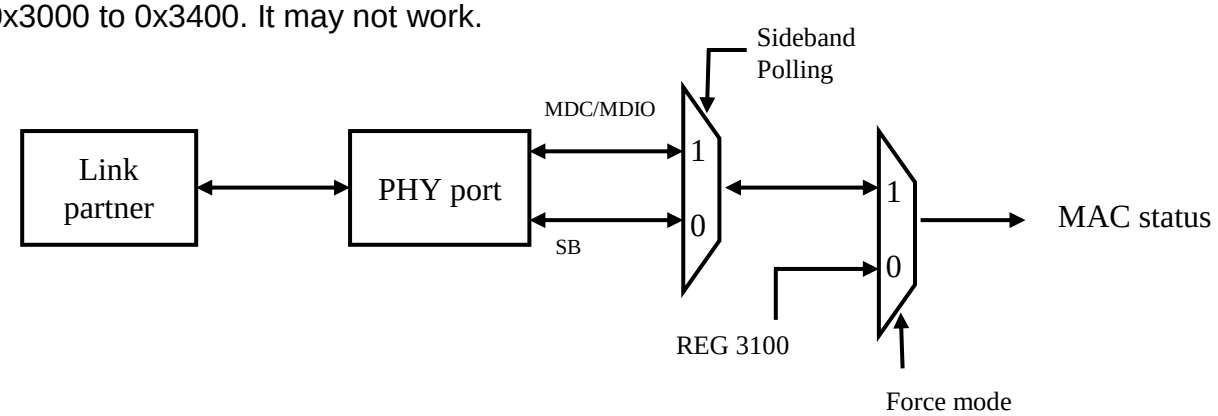
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	IGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P0			IGC_RATE_CIR_16_P0	IGC_RATE_EXP_P0_IGC_TB_T_P0				IGC_TB_EN_P0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P0	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P0	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P0	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P0_IGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P0	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0	**Mantissa part of port 0 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

Link Status

You can find MAC control register put at 0x3500 for MAC 5, and 0x3600 for MAC 6. You can change MAC ability at this register. We would suggest don't use the register 0x3000 to 0x3400. It may not work.



00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P5		EXT_PHY_P5	MAC_MODE_P5
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P5	MAC_TX_EN_P5	MAC_RX_EN_P5		MAC_PRE_P5		BKOFF_EN_P5	BACKPR_EN_P5	FORCE_EEE1G_P5	FORCE_EEE100_P5	FORCE_RX_FC_P5	FORCE_TX_FC_P5	FORCE_SPD_P5		FORCE_DPX_P5	FORCE_LNK_P5
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P5	**PORT 5 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P5	**PORT 5 External PHY** Port 5 connects with external PHY. 0: PORT 5 DOES NOT connect with external PHY. 1: PORT 5 connects with external PHY.
16	MAC_MODE_P5	**PORT 5 MAC Mode** PORT 5 operates in MAC mode. 0: PORT 5 operates in PHY mode. 1: PORT 5 operates in MAC mode.
15	FORCE_MODE_P5	**PORT 5 Force Mode** PORT 5 operates in force mode. It is used to control PORT 5 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g. 0: Force mode is off (mac status is determined by phy auto-polling module). 1: Force mode is on (mac status is determined by force_xxx_P5 register).
14	MAC_TX_EN_P5	**Port 5 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P5	**PORT 5 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P5	**TX short preamble mode** 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P5	**PORT 5 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 5 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P5	**PORT 5 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P5	**PORT 5 Force LPI Mode For 1000Mbps** When (force_mode_P5 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps
6	FORCE_EEE100_P5	**PORT 5 Force LPI Mode For 100Mbps** When (force_mode_P5 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps

5	FORCE_RX_FC_P5	**PORT 5 Force RX FC** When (force_mode_P5 = 1), this bit is used to control the RX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P5	**PORT 5 Force TX FC** When (force_mode_P5 = 1), this bit is used to control the TX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P5	**PORT 5 Force Speed [1:0]** When (force_mode_P5 = 1), these bits are used to control MAC speed of PORT 5. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P5	**PORT 5 Force duplex** When (force_mode_P5 = 1), this bit is used to control MAC duplex of PORT 5. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P5	**PORT 5 Force MAC Link Up** When (force_mode_P5 = 1), this bit is used to control link status of PORT 5. 0: Link Down 1: Link Up

For MAC 5 and MAC6, they have its own status to check register. 0x3508 is for MAC 5 status and 0x3608 is for MAC 6. If you want to change MAC 5 status, you can use 0x3500 to change its ability.

00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5		MAC_DPX_STS_P5	MAC_LNK_STS_P5
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P5	**PORT 5 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P5	**PORT 5 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P5	**PORT 5 RX XFC Status. Port 5 Rx flow control status** 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P5	**PORT 5 TX XFC Status** PORT 5 TX flow control status 0: Disabled. 1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P5	**PORT 5 Speed [1:0] Status** Current speed of PORT 5 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps

		11: Reserved
1	MAC_DPX_STS_P5	**PORT 5 duplex Status** Current duplex mode of port 5 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P5	**Port 5 Link Up Status. Link up status of PORT 5.** 0: Link Down 1: Link Up

Link Status change

You can find the 0x700c is a record if PHY status was changed. For example, if you plug into PHY 1, you can find the 0x700c become 00080002. Then drew the PHY 1, the 0x700c would still keep 00080002.You need to write “1” to the bit which you want clean at the register 0x700c. After that you can find it would become 00080000.

0000700C SYS_INT_STS System Interrupt Status 00000000

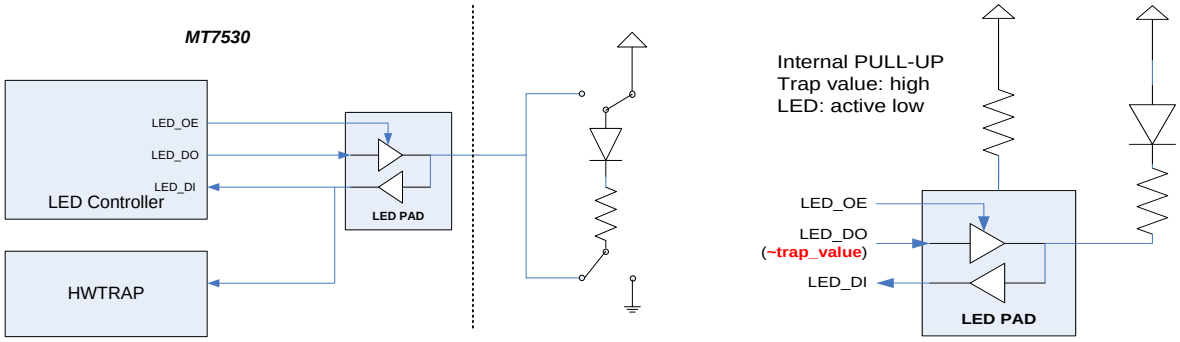
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_INT	ARL_SEC_TAG_INT	ARL_SEC_VLAN_INT	ARL_SEC_IG1X_INT	ARL_PKT_BC_INT	ARL_EQ_ERR_INT	ARL_PKT_QERR_INT	ARL_TBL_ERR_INT					PTP_INT	MIB_INT	BMU_INT	MAC_PC_INT
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PHY6_INT	PHY5_INT	PHY4_INT	PHY3_INT	PHY2_INT	PHY1_INT	PHY0_INT		PHY6_LC_INT	PHY5_LC_INT	PHY4_LC_INT	PHY3_LC_INT	PHY2_LC_INT	PHY1_LC_INT	PHY0_LC_INT
Type		W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

LED controller

All hardware traps of MT7530 are weakly pull-up internally. The only way to pull-down these traps is using an external pull-down circuit. However, hardware traps and LEDs share the same pins in MT7530. To make LEDs work normally, the hardware configurations of LEDs will depend on its related values in the current design.
Every port has 3 LED to mean its behavior:

MT7530 Px_LED_0 is used for any ability linkup and traffic (10/100/1000).
MT7530 Px_LED_1 is used for 10/100 ability linkup and traffic (10/100).
MT7530 Px_LED_2 is used for Giga ability linkup and traffic (1000).

For trapping-high pins, the external LEDs should be active low. Its configuration is shown as below. OEs (output enables) of LED pads are controlled by the internal circuits, and LED_DO will always be LOW under this configuration. So the external LEDs should be active low.



For LED configuration, you can follow the below descrition.

00007D00 LED_EN LED I/O function enable 00077777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_EN		
Type														RW		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_EN				P2_LED_EN				P1_LED_EN				P0_LED_EN		
Type		RW				RW				RW				RW		
Reset		1	1	1		1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
18:16	P4_LED_EN	**P4 LED I/O Enable** P4_LED_EN[2] for P4 LED #2 P4_LED_EN[1] for P4 LED #1 P4_LED_EN[0] for P4 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
14:12	P3_LED_EN	**P3 LED I/O Enable** P3_LED_EN[2] for P3 LED #2 P3_LED_EN[1] for P3 LED #1 P3_LED_EN[0] for P3 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
10:8	P2_LED_EN	**P2 LED I/O Enable** P2_LED_EN[2] for P2 LED #2 P2_LED_EN[1] for P2 LED #1 P2_LED_EN[0] for P2 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
6:4	P1_LED_EN	**P1 LED I/O Enable** P1_LED_EN[2] for P1 LED #2 P1_LED_EN[1] for P1 LED #1 P1_LED_EN[0] for P1 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
2:0	P0_LED_EN	**P0 LED I/O Enable** P0_LED_EN[2] for P0 LED #2 P0_LED_EN[1] for P0 LED #1 P0_LED_EN[0] for P0 LED #0 For individual LED 1'b0: Disable 1'b1: Enable

00007D04 **LED_IO_MODE** **LED I/O Mode** **00077777**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_MODE		
Type														RW		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_MODE				P2_LED_MODE				P1_LED_MODE				P0_LED_MODE		
Type		RW				RW				RW				RW		
Reset		1	1	1		1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
18:16	P4_LED_MODE	**P4 LED I/O Mode** P4_LED_MODE[2] for P4 LED #2 P4_LED_MODE[1] for P4 LED #1 P4_LED_MODE[0] for P4 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
14:12	P3_LED_MODE	**P3 LED I/O Mode** P3_LED_MODE[2] for P3 LED #2 P3_LED_MODE[1] for P3 LED #1 P3_LED_MODE[0] for P3 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
10:8	P2_LED_MODE	**P2 LED I/O Mode** P2_LED_MODE[2] for P2 LED #2 P2_LED_MODE[1] for P2 LED #1 P2_LED_MODE[0] for P2 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
6:4	P1_LED_MODE	**P1 LED I/O Mode** P1_LED_MODE[2] for P1 LED #2 P1_LED_MODE[1] for P1 LED #1 P1_LED_MODE[0] for P1 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
2:0	P0_LED_MODE	**P0 LED I/O Mode** P0_LED_MODE[2] for P0 LED #2 P0_LED_MODE[1] for P0 LED #1 P0_LED_MODE[0] for P0 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED

If you want to change the LED behavior, please write these registers of Ethernet physical.

51F00240 **dev1Fh_reg024h** **LED0 On Control Register** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led0_en	rg_led0_pol								led0_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led0_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z)

		1: Enable
14	rg_led0_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led0_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00250 dev1Fh_reg025h LED0 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led0_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led0_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error Bit[8]:RX Idle Error Bit[9]:Force Blinks (Logic 1)

51F00260 dev1Fh_reg026h LED1 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led1_en	rg_led1_pol								led1_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led1_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led1_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led1_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1.

Bit[0]:Link 1000
Bit[1]:Link 100
Bit[2]:Link 10
Bit[3]:Link Down
Bit[4]:Full Duplex
Bit[5]:Half Duplex
Bit[6]:Force On (Logic 1)

51F00270 dev1Fh_reg027h LED1 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led1_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led1_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error Bit[8]:RX Idle Error Bit[9]:Force Blinks (Logic 1)

51F00280 dev1Fh_reg028h LED2 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led2_en	rg_led2_pol								led2_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led2_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led2_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led2_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00290 dev1Fh_reg029h LED2 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led2_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led2_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error Bit[8]:RX Idle Error Bit[9]:Force Blinks (Logic 1)

51F002A0 dev1Fh_reg02Ah LED3 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led3_en	rg_led3_pol								led3_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led3_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led3_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led3_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F002B0 dev1Fh_reg02Bh LED3 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led3_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

9:0	led3_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error Bit[8]:RX Idle Error Bit[9]:Force Blinks (Logic 1)

Loop detection

When loop detection function is enabled by setting hardware strapping(0x7804), the MT7530 provide two different signal out. One is sent the loop frame with the SID as 0180c2000001, another is sent the period LED from the 96th pin of MT7530.
Follow the step to check it:

1. Set 0x30c0 (for example : enable p0,p1,p3, set as 0x07130000)
2. Set 0x201c,0x211c ..0x261c to enable per port broadcast storm detection(for example, set 0x201c as cc030303 for port 0)

   After that, you can check the Loop frame and alarm signal from 96th pin.

3. Read 0x30c0 to check the Alarm message.
   (You can write bit 1 of 0x30c0 as 1 to clean the status)

000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LPDET_EN6	LPDET_EN5	LPDET_EN4	LPDET_EN3	LPDET_EN2	LPDET_EN1	LPDET_EN0	LPDET_PERIOD_EN	LPDET_ALARM_EN	LPDET_PASS	LPDET_PERIOD	LPDET_LED_RATE	LPDET_THRESHOLD		
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_ST_LOOP	LPDET_ST_BCST	LPDET_TRAP_EN							LPDET_ALARM6	LPDET_ALARM5	LPDET_ALARM4	LPDET_ALARM3	LPDET_ALARM2	LPDET_ALARM1	LPDET_ALARM0
Type	RO	RO	RO							RO	RO	RO	RO	RO	RO	W1C
Reset	0	0	0							0	0	0	0	0	0	0

Bit(s)	Name	Description
30	LPDET_EN6	**Enable the loop detection ability of user port 6.** 0: Disable 1: Enable
29	LPDET_EN5	**Enable loop detection the ability of user port 5.** 0: Disable 1: Enable
28	LPDET_EN4	**Enable loop detection the ability of user port 4.** 0: Disable 1: Enable

27	LPDET_EN3	**Enable loop detection the ability of user port 3.** 0: Disable 1: Enable
26	LPDET_EN2	**Enable loop detection the ability of user port 2.** 0: Disable 1: Enable
25	LPDET_EN1	**Enable loop detection the ability of user port 1.** 0: Disable 1: Enable
24	LPDET_EN0	**Enable loop detection the ability of user port 0.** 0: Disable 1: Enable
23	LPDET_PERIOD_EN	**The loop detection frame is triggered by a periodical timer or by broadcast storm.** 0: Broadcast mode 1: Periodical mode
22	LPDET_ALARM_EN	**Enable 2 kHz alarm output and per-port LED when loop is detected.** 0: Disable 1: Enable
21	LPDET_PASS	**Loop detection frame is blocked or passed to packet memory.** 0: Blocked 1: Pass
20	LPDET_PERIOD	**Interval of transmitting loop detection frame in Periodical mode.** 0: 125 us 1: 1000 ms
19	LPDET_LED_RATE	**LED blinking rate of per port when loop is detected.** 0: LED blinking at 2 Hz 1: LED blinking at 4 Hz
18:16	LPDET_THRESHOLD	**Number of missed loop detection frame before 2 kHz alarm is reset**
15	LPDET_ST_LOOP	**The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.** 0: Not in Loop state 1: Loop state
14	LPDET_ST_BCST	**The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.** 0: Not in BCST state 1: BCST state
13	LPDET_TRAP_EN	**Status of strap pin for loop detection** 0: Disabled 1: Enabled
6	LPDET_ALARM6	**The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
5	LPDET_ALARM5	**The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
4	LPDET_ALARM4	**The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
3	LPDET_ALARM3	**The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
2	LPDET_ALARM2	**The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected

1	LPDET_ALARM1	**The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
0	LPDET_ALARM0	**The status of loop detected on port 0. This bit is cleared when it is written as 1.** 0: Not detected 1: Detected

0000201C **BSR** **Broadcast Storm Rate Control of P0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

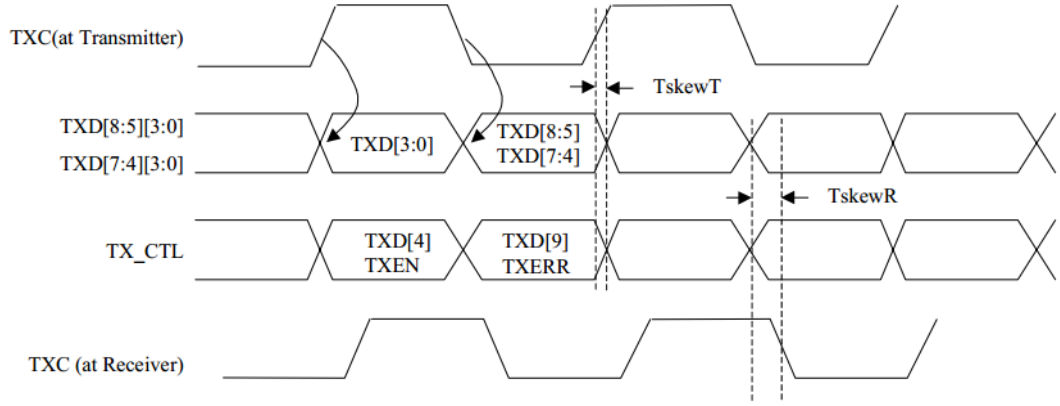
Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

MAC 5 interface setup

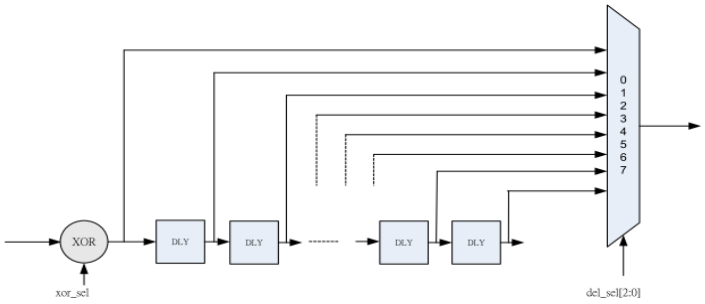
Usually, GMII of P5 does not need to do the delay. If you want to use as RGMII, you may modify the TX or RX delay timing. Please also notice that 10Mbps and 100Mbps mode also can do the delay. But, you know that their CLK timing is 400ns and 40ns. So, that also means the 2ns delay latency may not useful to them.

00007B04 P5RGMIITXCR P5 RGMII Wrapper TX Clock Control Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														csr_rgmii_txen_cfg		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_rgmii_txd_cfg						csr_rgmii_txc_cfg				
Type						RW						RW				
Reset						0	0	0				1	0	0	0	0



You can adjust 0x7b04 for P5 CLK, data and enable delay timing.
0x7b04: P5 RGMII Wrapper TX Clock Control Register
Bit 4 ([4] - Using 90-degree TXC (central align)) is used for adjusting align. You can change the bit if you got the short packet.
Bit 3 ([3] - Inverted RXC) is used for enable the XOR, like the below figure. It is usually for a large timing adjustment.



If you need to change the RX delay of P5, please modify 0x7b00. rxd_cfg and rctl_cfg . Here is the sample when MT7530 link with Vitesse PHY.

(a) Change reg7B00[18:16] rxd_cfg[2:0]，from 3'b000 to 3'b010

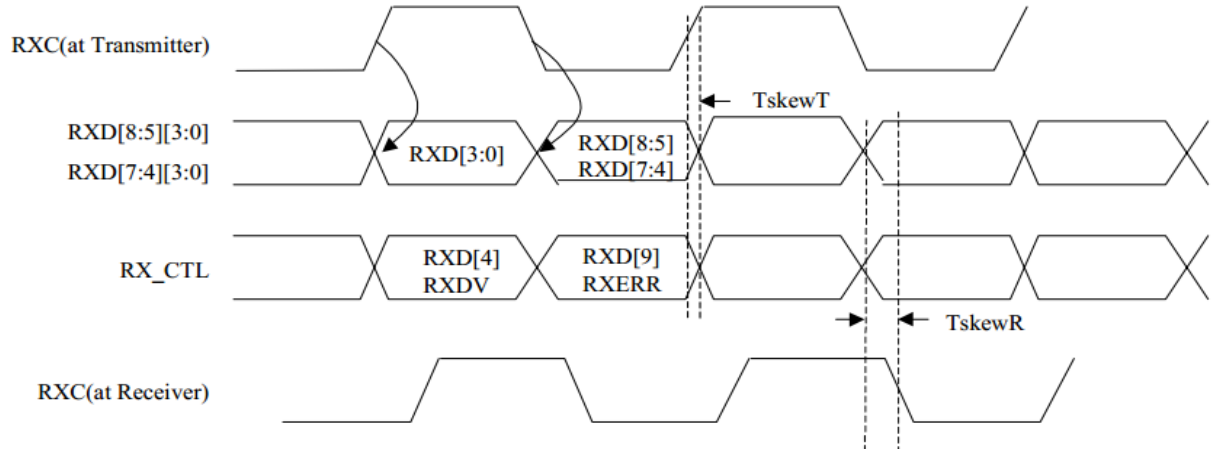
(b) Change reg7B00[26:24] rctl_cfg[2:0]，from3'b000 to 3'b010

You may also change the CLK align.

(a) Change reg7B04[4:0] GTXC setting，from 5'b10000 to 5'b01001

00007B00 P5RGMIIRXCR P5 RGMII Wrapper RX Clock Control Register 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						csr_rgmii_rctl_cfg								csr_rgmii_rxd_cfg		
Type						RW								RW		
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								csr_rgmii_central_align					csr_rgmii_rxc_0deg_cfg			
Type								RW					RW			
Reset								1					0	1	0	0



Please notice the bit 8 of 7b00 is used for checking the enable delay or not. The delay chain would be no longer valid if the 8th bit set as 1.

csr_rgmii_central_align **1: RXC/RXD is central-aligned; RXC does not pass through the delay chain.**
0: RXC/RXD is not central-aligned (edge-aligned); RXC passes through the delay chain.

0x7810 is used for setting TXC driving. P5 CLK driving is 12mA as default value. Others, like TXD, MDC and TXEN are also locate at this register.

00007810 IO_DRV_CR IO Driving Strength Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							csr_normal_drv				csr_mdc_drv				csr_led_mdio_drv	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			csr_p6_data_io_drv				csr_p6_clk_io_drv				csr_p5_io_data_drv				csr_p5_io_clk_drv	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

If P5 want to connect a PHY IC, you should check the below flow to make sure the PHY status:

1. Check 0x3508 : check the link up status

2. Check PHY is link up or not, use “tce miir 5 1”. If you get 796D, it means the PHY is link up.
3. Check 0x3500, 56300 is correct for its status.
4. Check 0x7018, it need to 7f7f8600 for enable polling mode.

00007018 PHY_POLL PHY Polling and SMI Master Control Register 007F8600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PHY_AP_EN								EEE_POLL_EN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PHY_PRE_EN	RX_TA1_CHK_OFF		PHY_END_ADDR					PMDC_CFG			PHY_ST_ADDR				
Type	RW	RW		RW					RW			RW				
Reset	1	0		0	0	1	1	0	0	0		0	0	0	0	0

MAC 6 interface setup

MT7530 TX driving use full power as default setting. You can change the register to change it:

0x7a54, 0x7a5c, 0x7a64, 0x7a6c, 0x7a74.

All of them are used ff as default. You can change to 44 if you need.

00007A54 TRGMII_TD0_ODT TRGMII TD0 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DM_DRVN_PRE		TD0_DM_DRVP_PRE		TD0_DM_TDSEL				TD0_ODTEN			TD0_DME_PRE	TD0_DM_DRVNT0	TD0_DM_DRVPT0	TD0_DM_DRVNTE	TD0_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD0_DM_ODTN				TD0_DM_ODTP			TD0_DM_DRVN				TD0_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A5C TRGMII_TD1_ODT TRGMII TD1 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD1_DM_DRVN_PRE		TD1_DM_DRVP_PRE		TD1_DM_TDSEL				TD1_ODTEN			TD1_DME_PRE	TD1_DM_DRVNT0	TD1_DM_DRVPT0	TD1_DM_DRVNTE	TD1_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD1_DM_ODTN				TD1_DM_ODTP			TD1_DM_DRVN				TD1_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A64 TRGMII_TD2_ODT TRGMII TD2 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD2_DM_DRVN_PRE		TD2_DM_DRVP_PRE		TD2_DM_TDSEL				TD2_ODTEN			TD2_DME_PRE	TD2_DM_DRVNT0	TD2_DM_DRVPT0	TD2_DM_DRVNTE	TD2_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD2_DM_ODTN				TD2_DM_ODTP			TD2_DM_DRVN				TD2_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A6C TRGMII_TD3_ODT TRGMII TD3 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD3_DM_DRVN_PRE		TD3_DM_DRVP_PRE		TD3_DM_TDSEL				TD3_ODTEN			TD3_DME_PRE	TD3_DM_DRVNT0	TD3_DM_DRVPT0	TD3_DM_DRVNTE	TD3_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD3_DM_ODTN				TD3_DM_ODTP			TD3_DM_DRVN				TD3_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A74 TRGMII_TXCTL_ODT TRGMII TXCTL ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXCTL_DM_DRVN_PRE		TXCTL_DM_DRVP_PRE		TXCTL_DM_TDSEL				TXCTL_ODTEN			TXCTL_DME_PRE	TXCTL_DM_DRVNT0	TXCTL_DM_DRVPT0	TXCTL_DM_DRVNTE	TXCTL_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TXCTL_DM_ODTN				TXCTL_DM_ODTP			TXCTL_DM_DRVN				TXCTL_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A7C TRGMII_TCK_ODT TRGMII TCK ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCK_DM_DRVN_PRE		TCK_DM_DRVP_PRE		TCK_DM_TDSEL				TCK_ODTEN			TCK_DME_PRE	TCK_DM_DRVNT0	TCK_DM_DRVPT0	TCK_DM_DRVNTE	TCK_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TCK_DM_ODTN				TCK_DM_ODTP			TCK_DM_DRVN				TCK_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

If you want to change P6 RX delay, please change the bit 0th to bit 6th of the follow register:
RXDO 0x7a10
RXD1 0x7a18
RXD2 0x7a20
RXD3 0x7a28
RXCTL 0x7a30

00007A10 TRGMII_RD0 TRGMII RD0 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD0_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD0_ERRCNT					RD0_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To trigger a bitslip operation, this bit should be written as 1. This bit is toggled after it is written as 1.** 1: Bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks, this bit should be written as 1. The comparison error is stored in ERRCNT. This bit is toggled after it is written as 1.** 1: Training comparison is performed for 16 clocks.
28	EDGE_CHK_PAT	**Training pattern selection for comparison** 0: The training pattern is the toggling pattern. 1: The training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when the bitslip is enabled. The suggested value is 15, 0, or 1.** 0: Normal operation
23:16	RD0_WD	**This register holds the received word for RD0.**
11:8	RD0_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of the training phase, the data received are compared to the data received at the previous clock. This register holds the mismatch counter of RD0.**
6:0	RD0_TAP	**This is the delay tap of RD0. To modify the delay tap, it should be increased or decreased by 1.**

If you want to change P6 TX delay, please change the bit 8th to bit 11th of the follow register:
TXDO 0x7a50
TXD1 0x7a58
TXD2 0x7a60
TXD3 0x7a68
TXCTL 0x7a70
Note:1 unit about 30ps

00007A50 TRGMII_TD0_CTRL TRGMII TD0 CTRL REGISTER 00000455

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DMPEDRV					TD0_DM_RTT										
Type	RW					RW										
Reset	0					0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD0_DM_SR	TD0_DMERODT	TD0_DMOECTL		TD0_TAP				TD0_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	1	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TD0_DMPEDRV	
26:24	TD0_DM_RTT	**This is the RTT setting.**
15	TD0_DM_SR	
14	TD0_DMERODT	**This is the ODT setting.**
13	TD0_DMOECTL	**OE edge selection**
11:8	TD0_TAP	**This is the delay tap of TD0. The delay tap is encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD0_TRAIN_WD	**This is the training word in training mode.**

MAC forward control

0x0010 is used for MAC forwarding control rule. For different traffic, like broadcast, Unknown multicast...etc, you can set the forwarding port at this register.

00000010 MFC MAC Forward Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BC_FFP								UNM_FFP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNU_FFP								CPU_EN	CPU_PORT			MIRROR_EN	MIRROR_PORT		
Type	RW								RW	RW			RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BC_FFP	**Broadcast Frame Flooding Ports** If MAC receives broadcast frames, this field indicates the flooding ports. [NOTE] 1. The flooding port excludes the received port on the switch. 2. Frame dropped though BC_FFP=6'b0
23:16	UNM_FFP	**Unknown Multicast Frame Flooding Ports** If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports. [NOTE] 1. The flooding port will exclude the received port by HW. 2. Frame dropped though UNM_FFP=6'b0.

15:8	UNU_FFP	**Unknown Unicast Frame Flooding Ports** If MAC receives the unicast or multicast frames which can not be found on the ARL. The field indicates the flooding port. [NOTE] 1. The flooding port will excludes the received port by HW 2. Frame dropped though UNM_FFP=6'b0
7	CPU_EN	**CPU Port Enable** Enable the CPU port specified in CPU_PORT. 0: No CPU port exists. 1: Enable
6:4	CPU_PORT	**CPU Port Number** Set the CPU port number. 3'h0: Port 0 ... 3'h7: Port 7
3	MIRROR_EN	**Mirror Port Enable** Enable the mirror port specified in MIRROR_PORT. 0: No mirror available 1: Enable mirror
2:0	MIRROR_PORT	**Mirror Port Number** Set the mirror port number. 3'h0: Port 0 ... 3'h7: Port 7

Here also show the forwarding rule which you can set at register 0x0010.

FTAG	ACL Enable	ARL/DIP Table	Action
BC	ACL Hit and Port Map is enabled	-	Follow ACL Forwarding Port Map
	Disable or ACL not Hit	-	Follow MFC .BC_FFP register
MC IP_MULT IPV6_MULTI	ACL Hit and Port Map is enabled	-	Follow ACL Forwarding Port Map
	Disable or ACL not Hit	ARL Hit	Follow ARL Forwarding Port Map
		ARL not Hit	Follow MFC.UNM_FFP register
UC	ACL Hit and Port Map is enabled	-	Follow ACL Forwarding Port Map
	Disable or ACL not Hit	ARL Hit	Follow ARL Forwarding Port Map
		ARL not Hit	Follow MFC.UNU_FFP register

MAC table aging time

Aging time is used for recording the MAC is exist or not and would be clean after 300 seconds if there is no traffic pass through again. For changing this, you can modify the 0x00A0.

The aging time would be depending on the switch core clock speed.

000000A0 **AAC** **Address Age Control** **00095001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0											AGE_	AGE_CNT[7:4]			

												DIS				
Type	DC											RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_CNT[3:0]				AGE_UNIT											
Type	RW				RW											
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:21	REV0	**Reserved**
20	AGE_DIS	**Address Table Aging Disable** Disable or pause MAC address aging.
19:12	AGE_CNT	**Address Table Age Count** This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds.
11:0	AGE_UNIT	**Address Table Age Unit** The applied aging unit is equal to (AGE_UNIT+1) seconds.

MAC table

We have 2048 MAC entries exist in switch.
MT7530 build in the API command:
Ethphxcmd arl mactbl-disp
MAC AABBCCDDEEFF : TIMER:149, SA_PORT_FW:0, SA_MIR_EN:0, USER_PRI:0, EG_TAG:0, LEAKY_EN:0, PORT:4, STATUS:1, TYPE:0
You can find that have an aging time, source port information over there.

For RT63368 or others platform, you can use the command flow to check the MAC table list:

```
Ethphxcmd gsww 80 8002   //clean
Ethphxcmd gsww 80 8004   //first MAC entry
Ethphxcmd gswr 84        // show the first entry
Ethphxcmd gswr 88        // show the firstentry
Ethphxcmd gsww 80 8005   //next MAC entry
Ethphxcmd gswr 84        // show the second entry
Ethphxcmd gswr 88        // show the second entry
```

For detail, you can check the register 0x0080,0x0084 and 0x0088.

00000080 ATC Address Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				ADDR											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSY	SRCH_END	SRCH_HIT	ADDR_INVLD	AC_MAT				REV1		AC_SAT		REV2	AC_CMD		
Type	W1C	RO	RO	RO	RW				DC		RW		DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000084 **TSRA1** **Table Search Read Address I** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[47:40] / Destination IP(DIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[39:32] / Destination IP(DIP) Address [23:16]**
15:8	BYTE_2	**MAC Address[31:24] / Destination IP(DIP) Address [15:8]**
7:0	BYTE_3	**MAC Address[23:16] / Destination IP(DIP) Address [7:0]**

00000088 **TSRA2** **Table Search Read Address II** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[15:8] / Source IP(SIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[7:0] / Source IP(SIP) Address [23:16]**
15:8	BYTE_2	**SIP Address [15: 8] or** bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table.
7:0	BYTE_3	**SIP Address[7:0] or CVID[7:0]**

MAC number control

PHY auto polling and SMI master control register

Set the 0x7018 if you want to use auto polling mode for each PHY port.

00007018 **PHY_POLL** **PHY Polling and SMI Master Control Register** **007F8600**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PHY_AP_EN								EEE_POLL_EN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PHY_	RX_TA		PHY_END_ADDR					PMDC_CFG			PHY_ST_ADDR				

	PRE_EN	1_CHK_OFF															
Type	RW	RW		RW					RW			RW					
Reset	1	0		0	0	1	1	0	0	0		0	0	0	0	0	

Bit(s)	Name	Description
30:24	PHY_AP_EN	**PHY Auto-Polling Enable** It indicates the updating PHY status by auto-polling or side-band signals. bit 24 => port 0 bit 25 => port 1 bit 30 => port 6 1: PHY status obtained by Auto-polling 0: PHY status obtained by side-band signals
22:16	EEE_POLL_EN	**PHY EEE Polling Enable** It indicates polling the EEE capability of each PHY. bit 16 => port 0 bit 17 => port 1 bit 22 => port 6 1: Enable 0: Disable
15	PHY_PRE_EN	**PHY Preamble Enable** It indicates that the SMI master will send preamble bits (32 bits) at each MDIO read/write transaction. 1: Enable 0: Disable Note: This bit will affect both PHY auto-polling mode and PHY indirect access mode.
14	RX_TA1_CHK_OFF	**Disable the checking of RX_TA1 value.** 1: Do not check the value of RX_TA1 state 0: Check the value of RX_TA1. If this value is not 0, it means that there is no response from PHYs, and all rx_data are invalid.
12:8	PHY_END_ADDR	**PHY Polling End Address** It indicates the end address of PHY auto-polling process.
7:6	PMDC_CFG	**PHY MDC Clock Configuration** It is used to configure the divider N for MDC clock frequency. The MDC clock is from the system clock (500MHz) and is divided by N. 2'b00: N=256 2'b01: N=64 2'b10: N=32 2'b11: N=16 Note: MDC clock should not be over the MDC clock maximum value of PHY.
4:0	PHY_ST_ADDR	**PHY Polling Start Address** It indicates the start address of PHY auto-polling process.

Output queue

Each port has 8 queues for different QoS services. Please know that QoS only active when traffic jam happen. It means that you should have flow control first for QoS. If not, you would only find the packet loss.
Free page: Read the 0x1fc0

For MT7530, if you want to check the queue, please use:
ethphxcmd gsww 7038 220
ethphxcmd gswr 7034

Here show the Q map:

	Q1 & Q0	Q3 & Q2	Q5 & Q4	Q7 & Q6
P0	220	221	222	223
P1	224	225	226	227
P2	228	229	22a	22b
P3	22c	22d	22e	22f
P4	230	231	232	233
P5	234	235	236	237
P6	238	239	23a	23b

00001FC0 FPLC Free Page Link Count Register 01EE01EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MIN_FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0

Bit(s)	Name	Description
25:16	MIN_FREE_PL_CNT	**Minimal Free Page Link Count in LMU from last read access**
9:0	FREE_PL_CNT	**Free Page Link Count in LMU**

VLAN setting

You need use three registers to make one VLAN rule. Please follow the below information to do that:
Set the port you want into security mode and as user port, take port 1 as example:

0x 2104 00ff0003 //set as security mode
0x 2110 81000000 //set as user port
You should set up the each VLAN port you want to be security mode and user port.
Next, you need to setup the VLAN ID and group member. Here, we set port 0 to 3 and port 6 as one group and their VLAN ID is 10. And just only port 3 get the egress tag.

0x94 104F0001 Port member 0~3+6 (4f =0100 1111)
0x98 000000c0 Egress tag enable for port 3 , refer to register 0x98
0x90 80001003 VID member VID set as 03
Note: Please don't use 0 and 4095 for VID.

If you do not want to add egress tag at any port, just set 0x98 as 0. For detail, check the register 0x0098 at the below.

00002104 PCR Port Control of P1 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							

		_EN														
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000090 **VTCR** **VLAN Table Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_INVLD
Type	W1C	DC														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BUSY	**VLAN Table Is Busy** SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.
30:17	REV0	**Reserved**
16	IDX_INVLD	**Entry is not Valid** This index for the access control is out of the valid index.
15:12	FUNC	**Access Control Function** Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits . 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry. 4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved
11:0	VID	**1. VLAN ID Number: 0x0 to 0x1F (16)** 2. ACL table index: 0x0 to 0x3F (64) 3. ACL mask control: 0x0 to 0x3F (32 or 64)

0x94

(VLAN Entry)

Bits	Type	Name	Description	Initial value
31	RW	PORT_STAG	Port based STAG	0x0
30	RW	IVL_MAC	Independent VLAN Learning	0x0
29	RW	EG_CON	Egress Tag Consistent	0x0
28	RW	VTAG_EN	Per VLAN Egress Tag Control	0x0
27	RW	COPY_PRI	Copy User Priority Value from Customer Priority Tag for Stack VLAN	0x0
26:24	RW	USER_PRI	Service Tag User Priority Value from VLAN Table	0x0
23:16	RW	PORT_MEM	VLAN Member Control	0x0
15:4	RW	S_TAG1	Service Tag I	0x0
3:1	RW	FID	Filtering Database	0x0
0	RW	VALID	VLAN Entry Valid	0x0

0x98

(VLAN Entry)

Bits	Type	Name	Description	Initial value
31:16	RW	S_TAG2	Service Tag II	0x0
15:14	-	-	Reserved	0x0
13:12	RW	P6_TAG	P6 Egress Tag Control	0x0
11:10	RW	P5_TAG	P5 Egress Tag Control	0x0
9:8	RW	P4_TAG	P4 Egress Tag Control	0x0
7:6	RW	P3_TAG	P3 Egress Tag Control	0x0
5:4	RW	P2_TAG	P2 Egress Tag Control	0x0
3:2	RW	P1_TAG	P1 Egress Tag Control	0x0
1:0	RW	P0_TAG	P0 Egress Tag Control	0x0

00002010 PVC Port VLAN Control of P0 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.

15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

Note: if you want to drop (or not)packet with VLAN tag(or not), you can set bit 1:0 of REG 0x2010,0x2110,0x2210…0x2610 to do that.

VLAN translation

We provide two ways to do the VLAN ID translation. One is port base, another is not.

Port base VLAN translation:

You can follow the script to do the test(Use for ProComm plus). It is for VID=2 and VID3 translation and for Port 0 to Port 2.

```
**************************************************
proc main

;set security mode and user port of port 0.
transmit "ethphxcmd gsww 2004 00ff0003^M"
transmit "ethphxcmd gsww 2010 81000000^M"

;set security mode and user port of port 1.
transmit "ethphxcmd gsww 2104 00ff0003^M"
transmit "ethphxcmd gsww 2110 81000000^M"

;set security mode and user port of port 2.
transmit "ethphxcmd gsww 2204 00ff0003^M"
transmit "ethphxcmd gsww 2210 81000000^M"

;bit 31 of 0x94 as 1 ,means enable port base. Red bit means for index 0.
transmit "ethphxcmd gsww 94 907f0001^M"
transmit "ethphxcmd gsww 98 00001555^M"  ; egress tag control enable
transmit "ethphxcmd gsww 90 80001002^M" ; VID=2

;bit 31 of 0x94 as 1 ,means enable port base. Red bit means for index 2.
transmit "ethphxcmd gsww 94 907f0021^M"
transmit "ethphxcmd gsww 98 00001555^M"  ; egress tag control enable
transmit "ethphxcmd gsww 90 80001003^M" ; VID=3

; Note the index has 3 bit for setting, means from Index 0 to Index 7.

;set the index 0 from port 0 to port 6, and the translation ID is 100,200 and 300.
transmit "ethphxcmd gsww 2020 100^M"
transmit "ethphxcmd gsww 2120 200^M"
transmit "ethphxcmd gsww 2220 300^M"

;set the index 2 from port 0 to port 6, and the translation ID is 102,202 and 302.
transmit "ethphxcmd gsww 2024 102^M"
transmit "ethphxcmd gsww 2124 202^M"
transmit "ethphxcmd gsww 2224 302^M"

endproc
**************************************************
```

Not Port base VLAN translation:

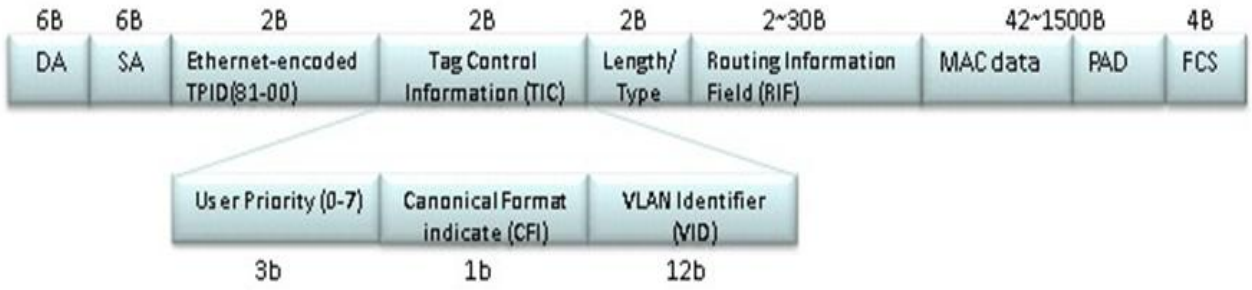
You can follow the script to do the test(Use for ProComm plus). It is for VID=2 and VID3 translation to VID=33 and VID=44.

```
**************************************************
proc main

transmit "ethphxcmd gsww 2004 00ff0003^M"
transmit "ethphxcmd gsww 2010 81000000^M"

transmit "ethphxcmd gsww 2104 00ff0003^M"
transmit "ethphxcmd gsww 2110 81000000^M"

transmit "ethphxcmd gsww 2204 00ff0003^M"
transmit "ethphxcmd gsww 2210 81000000^M"



;bit 31 of 0x94 as 0 ,means disable port base. Red bit means for VID=33.
transmit "ethphxcmd gsww 94 107f0331^M"
transmit "ethphxcmd gsww 98 00001555^M"
transmit "ethphxcmd gsww 90 80001002^M"

;bit 31 of 0x94 as 0 ,means disable port base. Red bit means for VID=44.
transmit "ethphxcmd gsww 94 107f0441^M"
transmit "ethphxcmd gsww 98 00001555^M"
transmit "ethphxcmd gsww 90 80001003^M"

endproc
**************************************************
```

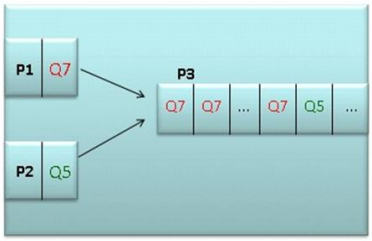
About the register 0x94 , 0x98 and 0x90, please refer to the above VLAN setting table.

QoS (Quality of Services)

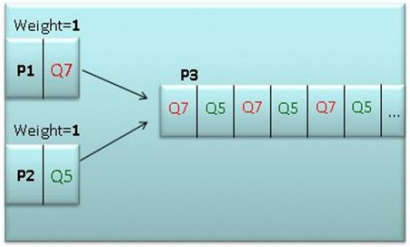
QoS is the ability to provide different priority to different applications or the data flows. MT7530 can support strict priority (SP) and weighted round-robin (WRR) mode for QoS. Please refer to packet format at the below figure and know the VID and user priority are the key for QoS. We will suggest that you should disable flow control if you want to use QoS.



SP:



WRR:

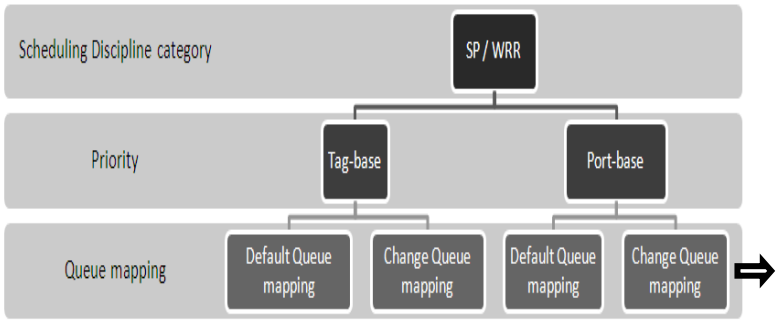


You may need to make the port you want as security mode and user port first. For detail, please check the page about VALN setting in this document.

0x 2104 00ff0003 //set as security mode
0x 2110 81000000 //set as user port

0x94 104F0001 Port member 0~3+6 (4f =0100 1111)
0x98 000000c0 Egress tag enable for port 3 , refer to register 0x98
0x90 80001003 VID member VID set as 03
Please also refer the chapter of VLAN to know the detail setting.

Follow the step to setup the QoS:



Default Priority-to-queue mapping (802.3D QoS)
Priority 7 – Queue 7
Priority 6 – Queue 6
Priority 5 – Queue 5
Priority 4 – Queue 4
Priority 3 – Queue 3
Priority 1 – Queue 2
Priority 0 – Queue 1
Priority 2 – Queue 0

You can swap the Q map as you want.
For example:
Change priority 1 from Q2 to Q1:
0x0048 09080240
Change priority 1 from Q1 to Q2:
0x0048 0a080240

Please notice the MT7530 use output queue structure. That means you should set these setting at output port.
Set as Tag-base
0x0044 as 0x222722 //Tag-base for first priority

If want to use SP:
0x1000 as 0x80000000 //SP for Q0 of Port 0
0x1004 as 0x00000000 //SP for Q0 of Port 0
0x1008 as 0x80000000 //SP for Q1 of Port 0
0x100c as 0x00000000 //SP for Q1 of Port 0

If want to use WRR:
0x1000 as 0x80008000 //WRR for Q0 of P0
0x1004 as 0x01000000 //weight of Q0 of P0
0x1008 as 0x80008000 //WRR for Q1 of P0
0x100c as 0x03000000 //weight of Q1 of P0

Set the port weight:
0x1004 as 0x01000000 //Weighting of P0 Q0 is 2 (**q0_max_weight+1'b1)**
0x100c as 0x03000000 //Weighting of P0 Q1 is 4 (**q1_max_weight+1'b1)**
…
Note: Queue n service with probability Pn (Pn = weight n / Sum (weight))

Follow the table and set the mode as SP or WRR.

	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Port 0	0x1000	0x1008	0x1010	0x1018	0x1020	0x1028	0x1030	0x1038
Port 1	0x1100	0x1108	0x1110	0x1118	0x1120	0x1128	0x1130	0x1138
Port 2	0x1200	0x1208	0x1210	0x1218	0x1220	0x1228	0x1230	0x1238
Port 3	0x1300	0x1308	0x1310	0x1318	0x1320	0x1328	0x1330	0x1338
Port 4	0x1400	0x1408	0x1410	0x1418	0x1420	0x1428	0x1430	0x1438
Port 5	0x1500	0x1508	0x1510	0x1518	0x1520	0x1528	0x1530	0x1538
Port 6	0x1600	0x1608	0x1610	0x1618	0x1620	0x1628	0x1630	0x1638

P0 weighting setting map:

00001004	**MMSCR1_Q0P0**	32	**Max-Min Scheduler Control Register 1 of Queue 0/Port 0**
0000100C	**MMSCR1_Q1P0**	32	**Max-Min Scheduler Control Register 1 of Queue 1/Port 0**
00001014	**MMSCR1_Q2P0**	32	**Max-Min Scheduler Control Register 1 of Queue 2/Port 0**
0000101C	**MMSCR1_Q3P0**	32	**Max-Min Scheduler Control Register 1 of Queue 3/Port 0**
00001024	**MMSCR1_Q4P0**	32	**Max-Min Scheduler Control Register 1 of Queue 4/Port 0**
0000102C	**MMSCR1_Q5P0**	32	**Max-Min Scheduler Control Register 1 of Queue 5/Port 0**
00001034	**MMSCR1_Q6P0**	32	**Max-Min Scheduler Control Register 1 of Queue 6/Port 0**
0000103C	**MMSCR1_Q7P0**	32	**Max-Min Scheduler Control Register 1 of Queue 7/Port 0**

00000044 UPW User Priority Weight 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0									ARL_UPW			REV1	PORT_UPW		
Type	DC									RW			DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	DC	RW			DC	RW			DC	RW			DC	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
31:23	REV0	**Reserved**
22:20	ARL_UPW	**ARL User Priority Weight (MAC/DIP Hit)**
19	REV1	**Reserved**
18:16	PORT_UPW	**Port-Based User Priority Weight Value** Weights range from 0x0 to 0x7.
15	REV2	**Reserved**
14:12	DSCP_UPW	**DSCP Priority Weight (IPv4)**
11	REV3	**Reserved**
10:8	TAG_UPW	**Priority Tag User Priority Weight**
7	REV4	**Reserved**
6:4	STAG_UPW	**Special Tag User Priority Weight**
3	REV5	**Reserved**
2:0	ACL_UPW	**ACL User Priority Weight (ACL Hit)**

00000048 PEM1 User Priority Egress Mapping I 08480240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_1			QUE_CPU_1			QUE_LAN_1		DSCP_PRI_1					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_0			QUE_CPU_0			QUE_LAN_0		DSCP_PRI_0					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_1	**User Priority 1 Priority Tag Value**
26:24	QUE_CPU_1	**User Priority 1 CPU Queue Selectio**
23:22	QUE_LAN_1	**User Priority 1 LAN Queue Selection**
21:16	DSCP_PRI_1	**User Priority 1 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_0	**User Priority 0 Priority Tag Value**
10:8	QUE_CPU_0	**User Priority 0 CPU Queue Selectio**
7:6	QUE_LAN_0	**User Priority 0 LAN Queue Selection**
5:0	DSCP_PRI_0	**User Priority 0 DSCP Value**

0000004C PEM2 User Priority Egress Mapping II 1B581110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_3			QUE_CPU_3			QUE_LAN_3		DSCP_PRI_3					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_2			QUE_CPU_2			QUE_LAN_2		DSCP_PRI_2					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_3	**User Priority 3 Priority Tag Value**
26:24	QUE_CPU_3	**User Priority 3 CPU Queue Selectio**
23:22	QUE_LAN_3	**User Priority 3 LAN Queue Selection**
21:16	DSCP_PRI_3	**User Priority 3 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_2	**User Priority 2 Priority Tag Value**
10:8	QUE_CPU_2	**User Priority 2 CPU Queue Selectio**
7:6	QUE_LAN_2	**User Priority 2 LAN Queue Selection**
5:0	DSCP_PRI_2	**User Priority 2 DSCP Value**

00001000 MMSCR0_Q0P0 Max-Min Scheduler Control Register 0 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P0				MIN_RATE_CTRL_EXP_Q0_P0					MIN_RATE_CTRL_MAN_Q0_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P0	**Port 0 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P0	**Port 0 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass (infinite rate). 1: Queue 0 min. rate limit control is enabled.
11:8	MIN_RATE_CTRL_EXP_Q0_P0	**Exponent part of Port 0 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P0	**Mantissa part of Port 0 Queue 0 min. shaper rate limit control** Value range: 1..100

00001004 MMSCR1_Q0P0 Max-Min Scheduler Control Register 1 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P0				MAX_WEIGHT_Q0_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P0				MAX_RATE_CTRL_EXP_Q0_P0					MAX_RATE_CTRL_MAN_Q0_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P0	**Port 0 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P0	**Port 0 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P0	**Port 0 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate). 1: Queue 0 maximum shaper rate limit is enabled.
11:8	MAX_RATE_CTRL_EXP_Q0_P0	**Exponent part of Port 0 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P0	**Mantissa part of Port 0 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001008 MMSCR0_Q1P0 Max-Min Scheduler Control Register 0 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P0				MIN_RATE_CTRL_EXP_Q1_P0					MIN_RATE_CTRL_MAN_Q1_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P0	**Port 0 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P0	**Port 0 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P0	**Exponent part of Port 0 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P0	**Mantissa part of Port 0 Queue 1 min. shaper rate limit control**

Value range: 1..127

0000100C MMSCR1_Q1P0 Max-Min Scheduler Control Register 1 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P0				MAX_WEIGHT_Q1_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P0				MAX_RATE_CTRL_EXP_Q1_P0					MAX_RATE_CTRL_MAN_Q1_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P0	**Port 0 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P0	**Port 0 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P0	**Port 0 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P0	**Exponent part of Port 0 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P0	**Mantissa part of Port 0 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001010 MMSCR0_Q2P0 Max-Min Scheduler Control Register 0 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P0				MIN_RATE_CTRL_EXP_Q2_P0					MIN_RATE_CTRL_MAN_Q2_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P0	**Port 0 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P0	**Port 0 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P0	**Exponent part of Port 0 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P0	**Mantissa part of Port 0 Queue 2 min. shaper rate limit control** Value range: 1..127

00001014 MMSCR1_Q2P0 Max-Min Scheduler Control Register 1 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P0				MAX_WEIGHT_Q2_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P0				MAX_RATE_CTRL_EXP_Q2_P0					MAX_RATE_CTRL_MAN_Q2_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P0	**Port 0 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P0	**Port 0 Queue 2 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P0	**Port 0 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P0	**Exponent part of Port 0 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P0	**Mantissa part of Port 0 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001018 MMSCR0_Q3P0 Max-Min Scheduler Control Register 0 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P0				MIN_RATE_CTRL_EXP_Q3_P0					MIN_RATE_CTRL_MAN_Q3_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P0	**Port 0 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P0	**Port 0 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P0	**Exponent part of Port 0 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P0	**Mantissa part of Port 0 Queue 3 min. shaper rate limit control** Value range: 1..127

0000101C MMSCR1_Q3P0 Max-Min Scheduler Control Register 1 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P0				MAX_WEIGHT_Q3_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P0				MAX_RATE_CTRL_EXP_Q3_P0					MAX_RATE_CTRL_MAN_Q3_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P0	**Port 0 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P0	**Port 0 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P0	**Port 0 Queue 3 maximum shaper rate limit control is enabled.** 0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P0	**Exponent part of Port 0 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P0	**Mantissa part of Port 0 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001020 MMSCR0_Q4P0 Max-Min Scheduler Control Register 0 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P0				MIN_RATE_CTRL_EXP_Q4_P0					MIN_RATE_CTRL_MAN_Q4_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P0	**Port 0 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P0	**Port 0 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P0	**Exponent part of Port 0 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P0	**Mantissa part of Port 0 Queue 4 min. shaper rate limit control** Value range: 1..127

00001024 MMSCR1_Q4P0 Max-Min Scheduler Control Register 1 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P0				MAX_WEIGHT_Q4_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P0				MAX_RATE_CTRL_EXP_Q4_P0					MAX_RATE_CTRL_MAN_Q4_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P0	**Port 0 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P0	**Port 0 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P0	**Port 0 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P0	**Exponent part of Port 0 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P0	**Mantissa part of Port 0 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001028 MMSCR0_Q5P0 Max-Min Scheduler Control Register 0 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P0				MIN_RATE_CTRL_EXP_Q5_P0					MIN_RATE_CTRL_MAN_Q5_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P0	**Port 0 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P0	**Port 0 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P0	**Exponent part of Port 0 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P0	**Mantissa part of Port 0 Queue 5 min. shaper rate limit control** Value range: 1..127

0000102C MMSCR1_Q5P0 Max-Min Scheduler Control Register 1 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P0				MAX_WEIGHT_Q5_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P0				MAX_RATE_CTRL_EXP_Q5_P0					MAX_RATE_CTRL_MAN_Q5_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P0	**Port 0 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P0	**Port 0 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P0	**Port 0 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P0	**Exponent part of Port 0 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P0	**Mantissa part of Port 0 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001030 MMSCR0_Q6P0 Max-Min Scheduler Control Register 0 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P0				MIN_RATE_CTRL_EXP_Q6_P0					MIN_RATE_CTRL_MAN_Q6_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P0	**Port 0 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P0	**Port 0 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P0	**Exponent part of Port 0 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P0	**Mantissa part of Port 0 Queue 6 min. shaper rate limit control** Value range: 1..127

00001034 MMSCR1_Q6P0 Max-Min Scheduler Control Register 1 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P0				MAX_WEIGHT_Q6_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P0				MAX_RATE_CTRL_EXP_Q6_P0					MAX_RATE_CTRL_MAN_Q6_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P0	**Port 0 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P0	**Port 0 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P0	**Port 0 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P0	**Exponent part of Port 0 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P0	**Mantissa part of Port 0 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001038 MMSCR0_Q7P0 Max-Min Scheduler Control Register 0 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P0				MIN_RATE_CTRL_EXP_Q7_P0					MIN_RATE_CTRL_MAN_Q7_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P0	**Port 0 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P0	**Port 0 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P0	**Exponent part of Port 0 Queue 7 min. shaper rate limit control** Value range: 0..13

6:0	MIN_RATE_CTRL_MAN_Q7_P0	**Mantissa part of Port 0 Queue 7 min. shaper rate limit control** Value range: 1..127

0000103C MMSCR1_Q7P0 Max-Min Scheduler Control Register 1 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P0				MAX_WEIGHT_Q7_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P0				MAX_RATE_CTRL_EXP_Q7_P0					MAX_RATE_CTRL_MAN_Q7_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P0	**Port 0 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P0	**Port 0 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P0	**Port 0 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P0	**Exponent part of Port 0 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P0	**Mantissa part of Port 0 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001040 ERLCR_P0 Egress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P0			EGC_RATE_CIR_16_P0	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0				EGC_TB_EN_P0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P0	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P0	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P0	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement,

		0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P0	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0	**Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

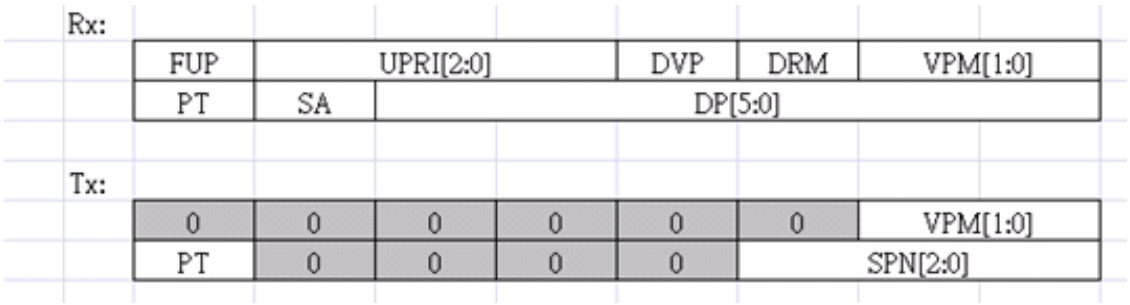
000010E0 **GERLCR** **Global Egress Rate Limit Control Register** **00000104**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EGC_MFRM_EX	EGC_IPG_OP	EGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
9	EGC_MFRM_EX	**When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)** 0: Include management frames 1: Exclude management frames
8	EGC_IPG_OP	**Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	EGC_IPG_BYTE	**Egress Rate IPG Byte Count** Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC (default) 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble

Special tag format

Special is used for taking the per-port information to CPU port. It replaces the VLAN tag and inserts the special tag format as below:



RX

Bit	15	14	13	12	11	10	9	8
Name	FUP	UPR[2:0]			DVP	DRM	VPM[1:0]	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PT	SA	DP[5:0]					

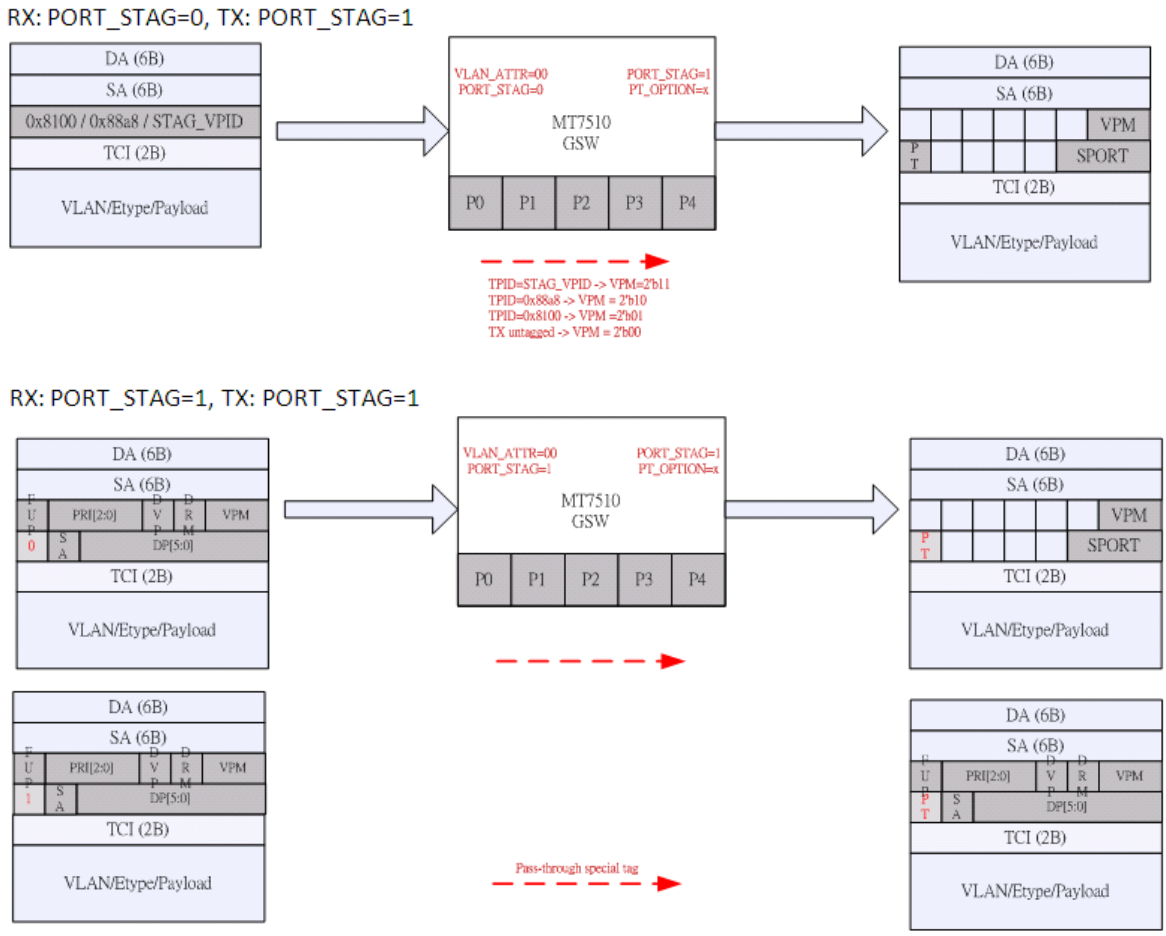
Bit(s)	Name	Description
15	FUP	**Force PPE user priority**
14:12	UPR	PPE user priority
11	DVP	Disable VALN priority remarking
10	DRM	Disable DSCP priority remarking
9:8	VPM	Tag attribute before special tag insertion; 2'b00 untagged; 2'b01 TPID=8100; 2'b10 TPID=predefined (e.g. 0x9100 or 0x88a8) Pass through
7	PT	Disable SA learning
6	SA	
5:0	DP	Force forwarding port map; all 0 means disable.

TX

Bit	15	14	13	12	11	10	9	8
Name	0	0	0	0	0	0	VPM[1:0]	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PT	0	0	0	0	SPN[2:0]		

Bit(s)	Name	Description
9:8	VPM	Tag attribute before special tag insertion; 2'b00 untagged; 2'b01 TPID=8100; 2'b10 TPID=predefined (e.g. 0x9100 or 0x88a8) Pass through
7	PT	Disable VALN priority remarking
2:0	SPN	Source port number

We show some case here to explain the behavior of special tag:



You can enable them at Reg 0x2010,0x2110…etc.., for per-port ability.

00002010 PVC Port VLAN Control of P0 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Local port enable

This is used for debugging not for normal use. It means it would add the self port to the MAC table. So, the same packet would come out from the input port. Set 7th of 0x000c to enable it.

0000000C AGC ARL Global Control 00071819

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MLDv2_int_en	REV0												ACL_INT	VLAN_INT	ADDR_INT
Type	RW	DC												RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATE_COMP	COMP_BNUM							LOCAL_EN	ARL_PADDING	ACL_MULTI	L2LEN_CHK	CTRL_DROP	VLAN4CPU	ARL_PRI	ALR_RST_N
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1

System MAC Controller

MT7530 build-in the internal MAC. The default MAC is 00000017a501. We put them at 0x30E8 and 0x30E4. You can change the default value as you want.

000030E4 SMACCR0 System MAC Control Register 0 0017A501

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMACCR0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR0[15:0]															
Type	RW															
Reset	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	SMACCR0	**System MAC Address, sys_mac [31:0]. The first 32-bit of system MAC address. It is unique and is specified for pause frame.**

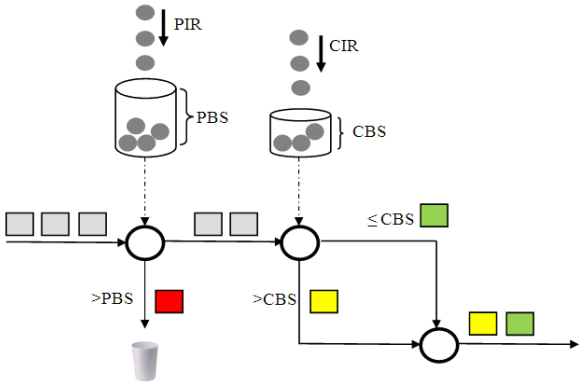
000030E8 SMACCR1 System MAC Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SMACCR1	**System MAC Address, sys_mac [47:32]. The second 16-bit of system MAC address. It is unique and is specified for pause frame.**

Two Rate Three Color Marker (TrTCM)

RFC2698 clearly points out the behavior of trTCM. The implementation adopts 2 token bucket counters to realize 64Kbps-step rate metering. CIR/PIR stands for token accumulating rate and CBS/PBS is the bucket depth. trTCM engine is divided into bucket filling engine and marker. The bucket filling engine utilize one shared hardware engine is running full- time to update 32 token bucket counters. When there comes a packet need for coloring, the marker has higher priority to take the owner ship of meter-table to mark the packet a color. You can know the concept below.




```
ethphxcmd gsww 94 ffff0001  //rule pattern
ethphxcmd gsww 98 0008400c
ethphxcmd gsww 90 80005000

 ethphxcmd gsww 94 00000001 ; acl mask
 ethphxcmd gsww 98 00000000
 ethphxcmd gsww 90 80009000

 ethphxcmd gsww 94 30004000   ; CBS , PBS
 ethphxcmd gsww 98 03200640   ; CIR = 50Mbps,PIR=100Mbps
 ethphxcmd gsww 90 80007000   ;trtcm meter table

 ethphxcmd gsww 94 18000000   ; Enable ACL interrupt [28] and hit count [27] . ACL hit index[26:24] is 0
 ethphxcmd gsww 98 00010000   ; meter idx & color by trtcm_
 ethphxcmd gsww 90 8000b000   ; ACL rule

 ethphxcmd gsww 9c 80000000   ;trtcm enable_

ethphxcmd gsww 180c 80000000
ethphxcmd gsww 1814 04020000   ;yellow for port 0 Q=2
ethphxcmd gsww 1834 07030010   ;Red for port 0 Q=2
```

0x0094 TrTCM Meter table

31:16	RW	CBS	**Committed Burst Size** The maximum number of bytes allowed for incoming packets to burst above the CIR, but still be marked green. The CBS burst size should be larger than CIR for token added.	0x0
15:0	RW	PBS	**Peak Burst Size** The maximum number of bytes allowed for incoming packets to burst above the CIR and still be marked yellow. The PBS burst size should be larger than PIR for token added.	0x0

0x0098 TrTCM Meter table

31:16	RW	CIR	**Committed Information Rate** 16'h0: 0 * 64Kbps 16'h1: 1 * 64Kbps ~~ 16'hFFFF: 65536* 64Kbps (Note: 1*64Kbps means that ACL will add 1 token (1-Byte) to the CBS burst bucket every 125us.)	0x0
15:0	RW	PIR	**Peak Information Rate** 16'h0: 0 * 64Kbps 16'h1: 1 * 64Kbps ~~ 16'hFFFF: 65536* 64Kbps (Note: 1*64Kbps means that ACL will add 1 token (1-Byte) to the PBS burst bucket every 125us.)	0x0

You can read these registers to check the ACL status.
(You need to enable 27th bit for enable ACL hit count and 26th to 24th bit for counter group index at 0x0094 ACL rule control,)

00004F00	**AE0CNT**	32	**ACL Event 0 Counter**
00004F04	**AE1CNT**	32	**ACL Event 1 Counter**
00004F08	**AE2CNT**	32	**ACL Event 2 Counter**
00004F0C	**AE3CNT**	32	**ACL Event 3 Counter**
00004F10	**AE4CNT**	32	**ACL Event 4 Counter**
00004F14	**AE5CNT**	32	**ACL Event 5 Counter**
00004F18	**AE6CNT**	32	**ACL Event 6 Counter**
00004F1C	**AE7CNT**	32	**ACL Event 7 Counter**

MIB (management information base) counter

MIB counters are used to record the packet number of ingress and egress port. You can use software reset to clean it. Or write 0x4fe0 as 0 then write 80000000 to restart it.

MIB counter of port 0:

00004000	TDPC_P0	32	**TX Drop Packet Counter of Port 0**
00004004	TCRC_P0	32	**TX CRC Packet Counter of Port 0**
00004008	TUPC_P0	32	**TX Unicast Packet Counter of Port 0**
0000400C	TMPC_P0	32	**TX Multicast Packet Counter of Port 0**
00004010	TBPC_P0	32	**TX Broadcast Packet Counter of Port 0**
00004014	TCEC_P0	32	**TX Collision Event Counter of Port 0**
00004018	TSCEC_P0	32	**TX Single Collision Event Counter of Port 0**
0000401C	TMCEC_P0	32	**TX Multiple Collision Event Counter of Port 0**
00004020	TDEC_P0	32	**TX Deferred Event Counter of Port 0**
00004024	TLCEC_P0	32	**TX Late Collision Event Counter of Port 0**
00004028	TXCEC_P0	32	**TX excessive Collision Event Counter of Port 0**
0000402C	TPPC_P0	32	**TX Pause Packet Counter of Port 0**
00004030	TL64PC_P0	32	**TX packet Length in 64-byte slot Packet Counter of Port 0**
00004034	TL65PC_P0	32	**TX packet Length in 65-byte slot Packet Counter of Port 0**
00004038	TL128PC_P0	32	**TX packet Length in 128-byte slot Packet Counter of Port 0**
0000403C	TL256PC_P0	32	**TX packet Length in 256-byte slot Packet Counter of Port 0**
00004040	TL512PC_P0	32	**TX packet Length in 512-byte slot Packet Counter of Port 0**
00004044	TL1024PC_P0	32	**TX packet Length in 1024-byte slot Packet Counter of Port 0**
00004048	TOCL_P0	32	**TX Octet Counter Low double word of Port 0**
0000404C	TOCH_P0	32	**TX Octet Counter High double word of Port 0**
00004060	RDPC_P0	32	**RX Drop Packet Counter of Port 0**
00004064	RFPC_P0	32	**RX Filtering Packet Counter of Port 0**
00004068	RUPC_P0	32	**RX Unicast Packet Counter of Port 0**
0000406C	RMPC_P0	32	**RX Multicast Packet Counter of Port 0**
00004070	RBPC_P0	32	**RX Broadcast Packet Counter of Port 0**
00004074	RAEPC_P0	32	**RX Alignment Error Packet Counter of Port 0**
00004078	RCEPC_P0	32	**RX CRC(FCS) Error Packet Counter of Port 0**
0000407C	RUSPC_P0	32	**RX Undersize Packet Counter of Port 0**
00004080	RFEPC_P0	32	**RX Fragment Error Packet Counter of Port 0**
00004084	ROSPC_P0	32	**RX Oversize Packet Counter of Port 0**
00004088	RJEPC_P0	32	**RX Jabber Error Packet Counter of Port 0**
0000408C	RPPC_P0	32	**RX Pause Packet Counter of Port 0**
00004090	RL64PC_P0	32	**RX packet Length in 64-byte slot Packet Counter of Port 0**
00004094	RL65PC_P0	32	**RX packet Length in 65-byte slot Packet Counter of Port 0**
00004098	RL128PC_P0	32	**RX packet Length in 128-byte slot Packet Counter of Port 0**
0000409C	RL256PC_P0	32	**RX packet Length in 256-byte slot Packet Counter of Port 0**
000040A0	RL512PC_P0	32	**RX packet Length in 512-byte slot Packet Counter of Port 0**
000040A4	RL1024PC_P0	32	**RX packet Length in 1024-byte slot Packet Counter of Port 0**
000040A8	ROCL_P0	32	**RX Octet Counter Low double word of Port 0**
000040AC	ROCH_P0	32	**Rx Octet Counter High double word of Port 0**
000040B0	RDPC_CTRL_P0	32	**RX CTRL Drop Packet Counter of Port 0**
000040B4	RDPC_ING_P0	32	**RX Ingress Drop Packet Counter of Port 0**

000040B8	RDPC_ARL_P0	32	RX ARL Drop Packet Counter of Port 0
000040D0	TMIB_HF_STS_P0	32	TX Port MIB Counter Half Full Status of Port 0
000040D4	RMIB_HF_STS_P0	32	RX Port MIB Counter Half Full Status of Port 0

MIB counter of port 1:

00004100	TDPC_P1	32	TX Drop Packet Counter of Port 1
00004104	TCRC_P1	32	TX CRC Packet Counter of Port 1
00004108	TUPC_P1	32	TX Unicast Packet Counter of Port 1
0000410C	TMPC_P1	32	TX Multicast Packet Counter of Port 1
00004110	TBPC_P1	32	TX Broadcast Packet Counter of Port 1
00004114	TCEC_P1	32	TX Collision Event Counter of Port 1
00004118	TSCEC_P1	32	TX Single Collision Event Counter of Port 1
0000411C	TMCEC_P1	32	TX Multiple Collision Event Counter of Port 1
00004120	TDEC_P1	32	TX Deferred Event Counter of Port 1
00004124	TLCEC_P1	32	TX Late Collision Event Counter of Port 1
00004128	TXCEC_P1	32	TX excessive Collision Event Counter of Port 1
0000412C	TPPC_P1	32	TX Pause Packet Counter of Port 1
00004130	TL64PC_P1	32	TX packet Length in 64-byte slot Packet Counter of Port 1
00004134	TL65PC_P1	32	TX packet Length in 65-byte slot Packet Counter of Port 1
00004138	TL128PC_P1	32	TX packet Length in 128-byte slot Packet Counter of Port 1
0000413C	TL256PC_P1	32	TX packet Length in 256-byte slot Packet Counter of Port 1
00004140	TL512PC_P1	32	TX packet Length in 512-byte slot Packet Counter of Port 1
00004144	TL1024PC_P1	32	TX packet Length in 1024-byte slot Packet Counter of Port 1
00004148	TOCL_P1	32	TX Octet Counter Low double word of Port 1
0000414C	TOCH_P1	32	TX Octet Counter High double word of Port 1
00004160	RDPC_P1	32	RX Drop Packet Counter of Port 1
00004164	RFPC_P1	32	RX Filtering Packet Counter of Port 1
00004168	RUPC_P1	32	RX Unicast Packet Counter of Port 1
0000416C	RMPC_P1	32	RX Multicast Packet Counter of Port 1
00004170	RBPC_P1	32	RX Broadcast Packet Counter of Port 1
00004174	RAEPC_P1	32	RX Alignment Error Packet Counter of Port 1
00004178	RCEPC_P1	32	RX CRC(FCS) Error Packet Counter of Port 1
0000417C	RUSPC_P1	32	RX Undersize Packet Counter of Port 1
00004180	RFEPC_P1	32	RX Fragment Error Packet Counter of Port 1
00004184	ROSPC_P1	32	RX Oversize Packet Counter of Port 1
00004188	RJEPC_P1	32	RX Jabber Error Packet Counter of Port 1
0000418C	RPPC_P1	32	RX Pause Packet Counter of Port 1
00004190	RL64PC_P1	32	RX packet Length in 64-byte slot Packet Counter of Port 1
00004194	RL65PC_P1	32	RX packet Length in 65-byte slot Packet Counter of Port 1
00004198	RL128PC_P1	32	RX packet Length in 128-byte slot Packet Counter of Port 1
0000419C	RL256PC_P1	32	RX packet Length in 256-byte slot Packet Counter of Port 1
000041A0	RL512PC_P1	32	RX packet Length in 512-byte slot Packet Counter of Port 1
000041A4	RL1024PC_P1	32	RX packet Length in 1024-byte slot Packet Counter of Port 1
000041A8	ROCL_P1	32	RX Octet Counter Low double word of Port 1
000041AC	ROCH_P1	32	Rx Octet Counter High double word of Port 1
000041B0	RDPC_CTRL_P1	32	RX CTRL Drop Packet Counter of Port 1
000041B4	RDPC_ING_P1	32	RX Ingress Drop Packet Counter of Port 1

000041B8	RDPC_ARL_P1	32	**RX ARL Drop Packet Counter of Port 1**
000041D0	TMIB_HF_STS_P1	32	**TX Port MIB Counter Half Full Status of Port 1**
000041D4	RMIB_HF_STS_P1	32	**RX Port MIB Counter Half Full Status of Port 1**

MIB counter of port 2:

00004200	TDPC_P2	32	**TX Drop Packet Counter of Port 2**
00004204	TCRC_P2	32	**TX CRC Packet Counter of Port 2**
00004208	TUPC_P2	32	**TX Unicast Packet Counter of Port 2**
0000420C	TMPC_P2	32	**TX Multicast Packet Counter of Port 2**
00004210	TBPC_P2	32	**TX Broadcast Packet Counter of Port 2**
00004214	TCEC_P2	32	**TX Collision Event Counter of Port 2**
00004218	TSCEC_P2	32	**TX Single Collision Event Counter of Port 2**
0000421C	TMCEC_P2	32	**TX Multiple Collision Event Counter of Port 2**
00004220	TDEC_P2	32	**TX Deferred Event Counter of Port 2**
00004224	TLCEC_P2	32	**TX Late Collision Event Counter of Port 2**
00004228	TXCEC_P2	32	**TX excessive Collision Event Counter of Port 2**
0000422C	TPPC_P2	32	**TX Pause Packet Counter of Port 2**
00004230	TL64PC_P2	32	**TX packet Length in 64-byte slot Packet Counter of Port 2**
00004234	TL65PC_P2	32	**TX packet Length in 65-byte slot Packet Counter of Port 2**
00004238	TL128PC_P2	32	**TX packet Length in 128-byte slot Packet Counter of Port 2**
0000423C	TL256PC_P2	32	**TX packet Length in 256-byte slot Packet Counter of Port 2**
00004240	TL512PC_P2	32	**TX packet Length in 512-byte slot Packet Counter of Port 2**
00004244	TL1024PC_P2	32	**TX packet Length in 1024-byte slot Packet Counter of Port 2**
00004248	TOCL_P2	32	**TX Octet Counter Low double word of Port 2**
0000424C	TOCH_P2	32	**TX Octet Counter High double word of Port 2**
00004260	RDPC_P2	32	**RX Drop Packet Counter of Port 2**
00004264	RFPC_P2	32	**RX Filtering Packet Counter of Port 2**
00004268	RUPC_P2	32	**RX Unicast Packet Counter of Port 2**
0000426C	RMPC_P2	32	**RX Multicast Packet Counter of Port 2**
00004270	RBPC_P2	32	**RX Broadcast Packet Counter of Port 2**
00004274	RAEPC_P2	32	**RX Alignment Error Packet Counter of Port 2**
00004278	RCEPC_P2	32	**RX CRC(FCS) Error Packet Counter of Port 2**
0000427C	RUSPC_P2	32	**RX Undersize Packet Counter of Port 2**
00004280	RFEPC_P2	32	**RX Fragment Error Packet Counter of Port 2**
00004284	ROSPC_P2	32	**RX Oversize Packet Counter of Port 2**
00004288	RJEPC_P2	32	**RX Jabber Error Packet Counter of Port 2**
0000428C	RPPC_P2	32	**RX Pause Packet Counter of Port 2**
00004290	RL64PC_P2	32	**RX packet Length in 64-byte slot Packet Counter of Port 2**
00004294	RL65PC_P2	32	**RX packet Length in 65-byte slot Packet Counter of Port 2**
00004298	RL128PC_P2	32	**RX packet Length in 128-byte slot Packet Counter of Port 2**
0000429C	RL256PC_P2	32	**RX packet Length in 256-byte slot Packet Counter of Port 2**
000042A0	RL512PC_P2	32	**RX packet Length in 512-byte slot Packet Counter of Port 2**
000042A4	RL1024PC_P2	32	**RX packet Length in 1024-byte slot Packet Counter of Port 2**
000042A8	ROCL_P2	32	**RX Octet Counter Low double word of Port 2**
000042AC	ROCH_P2	32	**Rx Octet Counter High double word of Port 2**
000042B0	RDPC_CTRL_P2	32	**RX CTRL Drop Packet Counter of Port 2**
000042B4	RDPC_ING_P2	32	**RX Ingress Drop Packet Counter of Port 2**

000042B8	RDPC_ARL_P2	32	RX ARL Drop Packet Counter of Port 2
000042D0	TMIB_HF_STS_P2	32	TX Port MIB Counter Half Full Status of Port 2
000042D4	RMIB_HF_STS_P2	32	RX Port MIB Counter Half Full Status of Port 2

MIB counter of port 3:

00004300	TDPC_P3	32	TX Drop Packet Counter of Port 3
00004304	TCRC_P3	32	TX CRC Packet Counter of Port 3
00004308	TUPC_P3	32	TX Unicast Packet Counter of Port 3
0000430C	TMPC_P3	32	TX Multicast Packet Counter of Port 3
00004310	TBPC_P3	32	TX Broadcast Packet Counter of Port 3
00004314	TCEC_P3	32	TX Collision Event Counter of Port 3
00004318	TSCEC_P3	32	TX Single Collision Event Counter of Port 3
0000431C	TMCEC_P3	32	TX Multiple Collision Event Counter of Port 3
00004320	TDEC_P3	32	TX Deferred Event Counter of Port 3
00004324	TLCEC_P3	32	TX Late Collision Event Counter of Port 3
00004328	TXCEC_P3	32	TX excessive Collision Event Counter of Port 3
0000432C	TPPC_P3	32	TX Pause Packet Counter of Port 3
00004330	TL64PC_P3	32	TX packet Length in 64-byte slot Packet Counter of Port 3
00004334	TL65PC_P3	32	TX packet Length in 65-byte slot Packet Counter of Port 3
00004338	TL128PC_P3	32	TX packet Length in 128-byte slot Packet Counter of Port 3
0000433C	TL256PC_P3	32	TX packet Length in 256-byte slot Packet Counter of Port 3
00004340	TL512PC_P3	32	TX packet Length in 512-byte slot Packet Counter of Port 3
00004344	TL1024PC_P3	32	TX packet Length in 1024-byte slot Packet Counter of Port 3
00004348	TOCL_P3	32	TX Octet Counter Low double word of Port 3
0000434C	TOCH_P3	32	TX Octet Counter High double word of Port 3
00004360	RDPC_P3	32	RX Drop Packet Counter of Port 3
00004364	RFPC_P3	32	RX Filtering Packet Counter of Port 3
00004368	RUPC_P3	32	RX Unicast Packet Counter of Port 3
0000436C	RMPC_P3	32	RX Multicast Packet Counter of Port 3
00004370	RBPC_P3	32	RX Broadcast Packet Counter of Port 3
00004374	RAEPC_P3	32	RX Alignment Error Packet Counter of Port 3
00004378	RCEPC_P3	32	RX CRC(FCS) Error Packet Counter of Port 3
0000437C	RUSPC_P3	32	RX Undersize Packet Counter of Port 3
00004380	RFEPC_P3	32	RX Fragment Error Packet Counter of Port 3
00004384	ROSPC_P3	32	RX Oversize Packet Counter of Port 3
00004388	RJEPC_P3	32	RX Jabber Error Packet Counter of Port 3
0000438C	RPPC_P3	32	RX Pause Packet Counter of Port 3
00004390	RL64PC_P3	32	RX packet Length in 64-byte slot Packet Counter of Port 3
00004394	RL65PC_P3	32	RX packet Length in 65-byte slot Packet Counter of Port 3
00004398	RL128PC_P3	32	RX packet Length in 128-byte slot Packet Counter of Port 3
0000439C	RL256PC_P3	32	RX packet Length in 256-byte slot Packet Counter of Port 3
000043A0	RL512PC_P3	32	RX packet Length in 512-byte slot Packet Counter of Port 3
000043A4	RL1024PC_P3	32	RX packet Length in 1024-byte slot Packet Counter of Port 3
000043A8	ROCL_P3	32	RX Octet Counter Low double word of Port 3
000043AC	ROCH_P3	32	Rx Octet Counter High double word of Port 3
000043B0	RDPC_CTRL_P3	32	RX CTRL Drop Packet Counter of Port 3
000043B4	RDPC_ING_P3	32	RX Ingress Drop Packet Counter of Port 3

000043B8	RDPC_ARL_P3	32	RX ARL Drop Packet Counter of Port 3
000043D0	TMIB_HF_STS_P3	32	TX Port MIB Counter Half Full Status of Port 3
000043D4	RMIB_HF_STS_P3	32	RX Port MIB Counter Half Full Status of Port 3

MIB counter of port 4:

00004400	TDPC_P4	32	TX Drop Packet Counter of Port 4
00004404	TCRC_P4	32	TX CRC Packet Counter of Port 4
00004408	TUPC_P4	32	TX Unicast Packet Counter of Port 4
0000440C	TMPC_P4	32	TX Multicast Packet Counter of Port 4
00004410	TBPC_P4	32	TX Broadcast Packet Counter of Port 4
00004414	TCEC_P4	32	TX Collision Event Counter of Port 4
00004418	TSCEC_P4	32	TX Single Collision Event Counter of Port 4
0000441C	TMCEC_P4	32	TX Multiple Collision Event Counter of Port 4
00004420	TDEC_P4	32	TX Deferred Event Counter of Port 4
00004424	TLCEC_P4	32	TX Late Collision Event Counter of Port 4
00004428	TXCEC_P4	32	TX excessive Collision Event Counter of Port 4
0000442C	TPPC_P4	32	TX Pause Packet Counter of Port 4
00004430	TL64PC_P4	32	TX packet Length in 64-byte slot Packet Counter of Port 4
00004434	TL65PC_P4	32	TX packet Length in 65-byte slot Packet Counter of Port 4
00004438	TL128PC_P4	32	TX packet Length in 128-byte slot Packet Counter of Port 4
0000443C	TL256PC_P4	32	TX packet Length in 256-byte slot Packet Counter of Port 4
00004440	TL512PC_P4	32	TX packet Length in 512-byte slot Packet Counter of Port 4
00004444	TL1024PC_P4	32	TX packet Length in 1024-byte slot Packet Counter of Port 4
00004448	TOCL_P4	32	TX Octet Counter Low double word of Port 4
0000444C	TOCH_P4	32	TX Octet Counter High double word of Port 4
00004460	RDPC_P4	32	RX Drop Packet Counter of Port 4
00004464	RFPC_P4	32	RX Filtering Packet Counter of Port 4
00004468	RUPC_P4	32	RX Unicast Packet Counter of Port 4
0000446C	RMPC_P4	32	RX Multicast Packet Counter of Port 4
00004470	RBPC_P4	32	RX Broadcast Packet Counter of Port 4
00004474	RAEPC_P4	32	RX Alignment Error Packet Counter of Port 4
00004478	RCEPC_P4	32	RX CRC(FCS) Error Packet Counter of Port 4
0000447C	RUSPC_P4	32	RX Undersize Packet Counter of Port 4
00004480	RFEPC_P4	32	RX Fragment Error Packet Counter of Port 4
00004484	ROSPC_P4	32	RX Oversize Packet Counter of Port 4
00004488	RJEPC_P4	32	RX Jabber Error Packet Counter of Port 4
0000448C	RPPC_P4	32	RX Pause Packet Counter of Port 4
00004490	RL64PC_P4	32	RX packet Length in 64-byte slot Packet Counter of Port 4
00004494	RL65PC_P4	32	RX packet Length in 65-byte slot Packet Counter of Port 4
00004498	RL128PC_P4	32	RX packet Length in 128-byte slot Packet Counter of Port 4
0000449C	RL256PC_P4	32	RX packet Length in 256-byte slot Packet Counter of Port 4
000044A0	RL512PC_P4	32	RX packet Length in 512-byte slot Packet Counter of Port 4
000044A4	RL1024PC_P4	32	RX packet Length in 1024-byte slot Packet Counter of Port 4
000044A8	ROCL_P4	32	RX Octet Counter Low double word of Port 4
000044AC	ROCH_P4	32	Rx Octet Counter High double word of Port 4
000044B0	RDPC_CTRL_P4	32	RX CTRL Drop Packet Counter of Port 4
000044B4	RDPC_ING_P4	32	RX Ingress Drop Packet Counter of Port 4

000044B8	RDPC_ARL_P4	32	RX ARL Drop Packet Counter of Port 4
000044D0	TMIB_HF_STS_P4	32	TX Port MIB Counter Half Full Status of Port 4
000044D4	RMIB_HF_STS_P4	32	RX Port MIB Counter Half Full Status of Port 4

MIB counter of port 5:

00004500	TDPC_P5	32	TX Drop Packet Counter of Port 5
00004504	TCRC_P5	32	TX CRC Packet Counter of Port 5
00004508	TUPC_P5	32	TX Unicast Packet Counter of Port 5
0000450C	TMPC_P5	32	TX Multicast Packet Counter of Port 5
00004510	TBPC_P5	32	TX Broadcast Packet Counter of Port 5
00004514	TCEC_P5	32	TX Collision Event Counter of Port 5
00004518	TSCEC_P5	32	TX Single Collision Event Counter of Port 5
0000451C	TMCEC_P5	32	TX Multiple Collision Event Counter of Port 5
00004520	TDEC_P5	32	TX Deferred Event Counter of Port 5
00004524	TLCEC_P5	32	TX Late Collision Event Counter of Port 5
00004528	TXCEC_P5	32	TX excessive Collision Event Counter of Port 5
0000452C	TPPC_P5	32	TX Pause Packet Counter of Port 5
00004530	TL64PC_P5	32	TX packet Length in 64-byte slot Packet Counter of Port 5
00004534	TL65PC_P5	32	TX packet Length in 65-byte slot Packet Counter of Port 5
00004538	TL128PC_P5	32	TX packet Length in 128-byte slot Packet Counter of Port 5
0000453C	TL256PC_P5	32	TX packet Length in 256-byte slot Packet Counter of Port 5
00004540	TL512PC_P5	32	TX packet Length in 512-byte slot Packet Counter of Port 5
00004544	TL1024PC_P5	32	TX packet Length in 1024-byte slot Packet Counter of Port 5
00004548	TOCL_P5	32	TX Octet Counter Low double word of Port 5
0000454C	TOCH_P5	32	TX Octet Counter High double word of Port 5
00004560	RDPC_P5	32	RX Drop Packet Counter of Port 5
00004564	RFPC_P5	32	RX Filtering Packet Counter of Port 5
00004568	RUPC_P5	32	RX Unicast Packet Counter of Port 5
0000456C	RMPC_P5	32	RX Multicast Packet Counter of Port 5
00004570	RBPC_P5	32	RX Broadcast Packet Counter of Port 5
00004574	RAEPC_P5	32	RX Alignment Error Packet Counter of Port 5
00004578	RCEPC_P5	32	RX CRC(FCS) Error Packet Counter of Port 5
0000457C	RUSPC_P5	32	RX Undersize Packet Counter of Port 5
00004580	RFEPC_P5	32	RX Fragment Error Packet Counter of Port 5
00004584	ROSPC_P5	32	RX Oversize Packet Counter of Port 5
00004588	RJEPC_P5	32	RX Jabber Error Packet Counter of Port 5
0000458C	RPPC_P5	32	RX Pause Packet Counter of Port 5
00004590	RL64PC_P5	32	RX packet Length in 64-byte slot Packet Counter of Port 5
00004594	RL65PC_P5	32	RX packet Length in 65-byte slot Packet Counter of Port 5
00004598	RL128PC_P5	32	RX packet Length in 128-byte slot Packet Counter of Port 5
0000459C	RL256PC_P5	32	RX packet Length in 256-byte slot Packet Counter of Port 5
000045A0	RL512PC_P5	32	RX packet Length in 512-byte slot Packet Counter of Port 5
000045A4	RL1024PC_P5	32	RX packet Length in 1024-byte slot Packet Counter of Port 5
000045A8	ROCL_P5	32	RX Octet Counter Low double word of Port 5
000045AC	ROCH_P5	32	Rx Octet Counter High double word of Port 5
000045B0	RDPC_CTRL_P5	32	RX CTRL Drop Packet Counter of Port 5
000045B4	RDPC_ING_P5	32	RX Ingress Drop Packet Counter of Port 5

000045B8	RDPC_ARL_P5	32	**RX ARL Drop Packet Counter of Port 5**
000045D0	TMIB_HF_STS_P5	32	**TX Port MIB Counter Half Full Status of Port 5**
000045D4	RMIB_HF_STS_P5	32	**RX Port MIB Counter Half Full Status of Port 5**

MIB counter of port 6:

00004600	TDPC_P6	32	**TX Drop Packet Counter of Port 6**
00004604	TCRC_P6	32	**TX CRC Packet Counter of Port 6**
00004608	TUPC_P6	32	**TX Unicast Packet Counter of Port 6**
0000460C	TMPC_P6	32	**TX Multicast Packet Counter of Port 6**
00004610	TBPC_P6	32	**TX Broadcast Packet Counter of Port 6**
00004614	TCEC_P6	32	**TX Collision Event Counter of Port 6**
00004618	TSCEC_P6	32	**TX Single Collision Event Counter of Port 6**
0000461C	TMCEC_P6	32	**TX Multiple Collision Event Counter of Port 6**
00004620	TDEC_P6	32	**TX Deferred Event Counter of Port 6**
00004624	TLCEC_P6	32	**TX Late Collision Event Counter of Port 6**
00004628	TXCEC_P6	32	**TX excessive Collision Event Counter of Port 6**
0000462C	TPPC_P6	32	**TX Pause Packet Counter of Port 6**
00004630	TL64PC_P6	32	**TX packet Length in 64-byte slot Packet Counter of Port 6**
00004634	TL65PC_P6	32	**TX packet Length in 65-byte slot Packet Counter of Port 6**
00004638	TL128PC_P6	32	**TX packet Length in 128-byte slot Packet Counter of Port 6**
0000463C	TL256PC_P6	32	**TX packet Length in 256-byte slot Packet Counter of Port 6**
00004640	TL512PC_P6	32	**TX packet Length in 512-byte slot Packet Counter of Port 6**
00004644	TL1024PC_P6	32	**TX packet Length in 1024-byte slot Packet Counter of Port 6**
00004648	TOCL_P6	32	**TX Octet Counter Low double word of Port 6**
0000464C	TOCH_P6	32	**TX Octet Counter High double word of Port 6**
00004660	RDPC_P6	32	**RX Drop Packet Counter of Port 6**
00004664	RFPC_P6	32	**RX Filtering Packet Counter of Port 6**
00004668	RUPC_P6	32	**RX Unicast Packet Counter of Port 6**
0000466C	RMPC_P6	32	**RX Multicast Packet Counter of Port 6**
00004670	RBPC_P6	32	**RX Broadcast Packet Counter of Port 6**
00004674	RAEPC_P6	32	**RX Alignment Error Packet Counter of Port 6**
00004678	RCEPC_P6	32	**RX CRC(FCS) Error Packet Counter of Port 6**
0000467C	RUSPC_P6	32	**RX Undersize Packet Counter of Port 6**
00004680	RFEPC_P6	32	**RX Fragment Error Packet Counter of Port 6**
00004684	ROSPC_P6	32	**RX Oversize Packet Counter of Port 6**
00004688	RJEPC_P6	32	**RX Jabber Error Packet Counter of Port 6**
0000468C	RPPC_P6	32	**RX Pause Packet Counter of Port 6**
00004690	RL64PC_P6	32	**RX packet Length in 64-byte slot Packet Counter of Port 6**
00004694	RL65PC_P6	32	**RX packet Length in 65-byte slot Packet Counter of Port 6**
00004698	RL128PC_P6	32	**RX packet Length in 128-byte slot Packet Counter of Port 6**
0000469C	RL256PC_P6	32	**RX packet Length in 256-byte slot Packet Counter of Port 6**
000046A0	RL512PC_P6	32	**RX packet Length in 512-byte slot Packet Counter of Port 6**
000046A4	RL1024PC_P6	32	**RX packet Length in 1024-byte slot Packet Counter of Port 6**
000046A8	ROCL_P6	32	**RX Octet Counter Low double word of Port 6**
000046AC	ROCH_P6	32	**Rx Octet Counter High double word of Port 6**
000046B0	RDPC_CTRL_P6	32	**RX CTRL Drop Packet Counter of Port 6**

000046B4	RDPC_ING_P6	32	**RX Ingress Drop Packet Counter of Port 6**
000046B8	RDPC_ARL_P6	32	**RX ARL Drop Packet Counter of Port 6**
000046D0	TMIB_HF_STS_P6	32	**TX Port MIB Counter Half Full Status of Port 6**
000046D4	RMIB_HF_STS_P6	32	**RX Port MIB Counter Half Full Status of Port 6**

Annex

User Port

The user port is the default VLAN port. The incoming VLAN-tagged frame will be stripped by the outer tag no matter the following inner tags. Per untagged or priority-tagged frame, PVID will be treated as VID1 tag. At the same time, VID1 is used to look for VLAN table to get the FID and Service tag for VID0. When a new Source MAC address is learned, the VID1 will also be learned on the MAC table.
On the TX_CTRL side, each frame will carry 2*N-port egress control bits on per-port based. Bit0 indicates that this frame will carry VID 0 or not; similarly, Bit.1 is for VID1. Once if "Consistent tag" is set, the egress tag format will follow the ingress tag format

Translation Port

The translation port is designated for 1:1 or N:1 VLAN aggregation according to CHINA TELECOM EPON requirement. When an incoming frame is received on the translation port, the corresponding custom VID will be found from MAC table and then the CVID would be the VID for VLAN table.
On the upload direction, several custom VID could be translated into one service VID from VLAN table which be carried on VID0. When this frame is transmitted on the translation port, etag_ctrl[1:0] will be 2'b01 (Swap) and then service VID will appear on the egress frame.

Transparent Port

When the port is chosen as transparent port, the VLAN tags on the incoming will be ignored and treated as un-tagged frames. VID0 and VID1 will store PVID as the default VID which is used to look up VLAN table. On the egress side, TX_CTRL can accept "UNTAG" control to send the original frame.

Security mode

Enable 802.1Q VLAN for all the received frames.
Discard received frame due to ingress membership violation (interrupt CPU)
Discard received frames once if VID is missed on the VLAN table (interrupt CPU)

Check mode

Enable 802.1Q function for all the received frames.
Don’t discard received frame due to ingress membership violation
Discard received frames once if VID is missed on the VLAN table (interrupt CPU)

Fallback mode

Enable 802.1Q function for all the received frames.
Don’t discard received frame due to ingress membership violation
Frames whose VID is missed on the VLAN table will be filtered by the Port Matrix Member

Port Matrix mode

802.1Q function disables (VLAN Security and VLAN Filter Table)
Frames filtered by the Port Matrix Member