MT7623 Programming Guide
ETHSYS Part

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1 ETHSYS Control

1.1 Description

This module collects sub-system's all global configuration registers. The block diagram could be shown in figure 1-1. The hard-wire output is used to control the hardware (EX. CG enable or clock MUX selection…etc.). And the hard-wire input is used to collect the hardware status output (EX. ID or monitor output…etc.).

1.2 Feature List

- Sub-system global configuration
- Sub-system clock MUX and CG control
- Sub-system SW reset control
- Sub-system MEMO

1.3 Block Diagram

Figure 1-1 ETHSYS Sub-system Control

1.4 Clock Plan

Below figure shows the clock plan of ETHSYS.

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1.5 Register Definition

Module name: ETHDMASYS_SYSCTL Base address: (+1B000000h)

Address	Name	Width	Register Function
1B000000	ID0_3	32	ID ASCII Character 0-3
1B000004	ID4_7	32	ID ASCII Character 4-7
1B00000C	Revision_ID	32	Revision Identification
1B000014	SYSCFG1	32	System Configuration Register 1
1B000018	TESTSTAT0	32	Firmware Test Status 0
1B00001C	TESTSTAT1	32	Firmware Test Status 1
1B00002C	CLKCFG0	32	Clock Configuration Register 0
1B000030	CLKCFG1	32	Clock Configuration Register 1
1B000034	RSTCTL	32	Reset Control Register
1B000068	MEMO0	32	Memory0
1B00006C	MEMO1	32	Memory1
1B000070	MEMO2	32	Memory2
1B000074	MEMO3	32	Memory3
1B000078	MEMO4	32	Memory4
1B00007C	MEMO5	32	Memory5

1B000000 **CHIPID0_3** **ID ASCII Character 0-3** **3637544D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ID3								ID2							
Type	RO								RO							
Reset	0	0	1	1	0	1	1	0	0	0	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ID1								ID0							
Type	RO								RO							
Reset	0	1	0	1	0	1	0	0	0	1	0	0	1	1	0	1

Bit(s)	Name	Description
31:24	ID3	ASCII Identification Character 3
23:16	ID2	ASCII Identification Character 2
15:8	ID1	ASCII Identification Character 1
7:0	ID0	ASCII Identification Character 0

1B000004 **ID4_7** **ID ASCII Character 4-7** **20203332**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam	ID7								ID6							

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1B000004 **ID4_7** **ID ASCII Character 4-7** **20203332**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	RO								RO							
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Name	ID5								ID4							
Type	RO								RO							
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
31:24	ID7	**ASCII dentification Character 7**
23:16	ID6	**ASCII Identification Character 6**
15:8	ID5	**ASCII Identification Character 5**
7:0	ID4	**ASCII Identification Character 4**

1B000014 **SYSCFG1** **System Configuration Register 1** **00000014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GE2_MODE		GE1_MODE								AXI_MST_SYNC_SEL		AXI_SLV_SYNC_SEL			AXI_SYNC_MODE
Type	RW		RW								RW		RW			RW
Reset	0	0	0	0							0	1	0	1		0

Bit(s)	Name	Description
15:14	GE2_MODE	**Gigabit Port #2 Mode** Sets the interface mode on Gigabit port 2 0: RGMII Mode (10/100/1000 Mbps) 1: MII Mode (10/100 Mbps) 2: Reverse MII Mode (10/100 Mbps) 3: Reduced MII (10/100Mbps)
13:12	GE1_MODE	**Gigabit Port #1 Mode** Sets the interface mode on Gigabit port 1 0: RGMII Mode (10/100/1000 Mbps) 1: MII Mode (10/100 Mbps) 2: Reverse MII Mode (10/100 Mbps) 3: Reserved
5:4	AXI_MST_SYNC_SEL	**AXI aslice master direction AFIFO synchronizer selection** 0: 1 DFF SYNC 1: 2 DFF SYNC 2: 3 DFF SYNC 3: 3 DFF SYNC
3:2	AXI_SLV_SYNC_SEL	**AXI aslice slave direction AFIFO synchronizer selection** 0: 1 DFF SYNC

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Bit(s)	Name	Description
0	AXI_SYNC_MODE	1: 2 DFF SYNC 2: 3 DFF SYNC 3: 3 DFF SYNC **AXI ASYNC slice configuration** 0: AXI bus in ASYNC 1: AXI bus in SYNC

1B000018 TESTSTAT0 Firmware Test Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTSTAT0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTSTAT0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TESTSTAT0	**Firmware Test Status Register 0** NOTE: This register is reset only by a power-on reset.

1B00001C TESTSTAT1 Firmware Test Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTSTAT1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTSTAT1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TESTSTAT1	**Firmware Test Status Register 1** NOTE: This register is reset only by a power-on reset.

1B00002C CLKCFG0 Clock Configuration Register 0 C4001880

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSC_1US_DIV															
Type	RW															
Reset	1	1	0	0	0	1										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam				FE	TR											

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1B00002C **CLKCFG0** **Clock Configuration Register 0** **C4001880**

e				**_CLK_SEL**	**GMII_CLK_SEL**											
Type				RW	RW											
Reset				1	1											

Bit(s)	Name	Description
31:26	OSC_1US_DIV	**Oscillator 1 usec Divider** Sets the maximum for the reference clock counter for either a 20 MHz or 40 MHz external XTAL input. The count increments each 1usec (indicating 1 MHz), up to the maximum, before resetting to zero. This counts the frequency of an external XTAL. This count is used to output a 32 KHz frequency to the REFCLK0 pin. 0: Automatically generates a 1 usec system tick regardless of whether XTAL frequency is 20 MHz or 40 MHz. 49: Default value for a reference 50 MHz clock. 39: Default value for an external 40 MHz XTAL. 19: Default value for an external 20 MHz XTAL. Others: Manual mode for tick generation.
12	FE_CLK_SEL	**Frame engine main clock selection** 1: from ETHPLL 500MHz 0: from ETHPLL 250MHz
11	TRGMII_CLK_SEL	**TRGMII Tx clock selection(when TRGMII @362.5MHz, ETHPLL need to fix @500MHz)** 1: from TRGMII 362.5MHz 0: from ETHPLL 250MHz

1B00003C **CLKCFG1** **Clock Configuration Register 1** **200249E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**GP1_CLK_EN**	**GP2_CLK_EN**							
Type								RW	RW							
Reset								1	1							

Bit(s)	Name	Description
8	GP1_CLK_EN	**Giga port 1 clock control** 1: Clock Enable 0: Clock Disable
7	GP2_CLK_EN	**Giga port 2 clock control**

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Bit(s)	Name	Description
		1: Clock Enable 0: Clock Disable

1B000034 RSTCTL **Reset Control Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_RST								GMAC_RST							
Type	RW								RW							
Reset	0								0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										FE_RST				MCM_RST		SYS_RST
Type										RW				RW		W1C
Reset										0				1		0

Bit(s)	Name	Description
31	PPE_RST	**PPE reset control** 1: Reset Assert 0: Reset Deassert
23	GMAC_RST	**GMAC reset control** 1: Reset Assert 0: Reset Deassert
6	FE_RST	**FE reset control** 1: Reset Assert 0: Reset Deassert
2	MCM_RST	**MCM(MT7530) reset control** 1: Reset Assert 0: Reset Deassert
0	SYS_RST	**Whole Sub-System Reset Control** 1: Whole System Reset 0: NA

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1B00006 8 **MEMO0** **Memory0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO1	**Memory0**

1B00006 C **MEMO1** **Memory1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO2	**Memory1**

1B00007 0 **MEMO2** **Memory2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO1	**Memory2**

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1B000074 **MEMO3** **Memory3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO2	**Memory3**

1B000078 **MEMO4** **Memory4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO3	**Memory4**

1B00007C **MEMO5** **Memory5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO4[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO4	**Memory5**

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2 Frame Engine

2.1 Introduction

Frame engine provides a DMA interface to transfer Ethernet packets between CPU and GMACs. Frame engine includes PDAM, QDMA, PSE, PPE, GDM, and CDM. The main features of these functions are list below.

2.2 Feature List

2.2.1 PSE Features

- Wire-speed (1000 Mbps) Ethernet LAN/WAN NAT/NAPT routing
- Egress rate limiting/shaping (by GDM)
- Flow control for no-packet-loss guarantee
- Emulated multicast support for keep-alive (can mirror a Tx packet to CPU)
- IP/TCP/UDP Checksum offload (by GDM)
- IP/TCP/UDP Checksum Generation (by CDM)
- VLAN & PPPOE header insertion (by CDM)
- TCP Segmentation Offload (by CDM)
- Auto-Padding for sub-64 B packets

2.2.2 PPE Features

- IPV4 NAT/NAPT, ipv6 Routing and Tunnel IP (DS-Lite, 6RD)
- 1/2/4/8/16 K flows
- Virtual server, port-triggering & port forwarding
- All types of IPV4 NAT(NAPT, Twice NAT)
- All types of MAC/VLAN/PPPOE/IP/TCP/UDP binding
- 4 VLAN tagging (Q-in-Q)
- VID Swapping
- Support for 65536 PPPOE sessions
- PPPOE pass-through
- Cone-NAT, port-restricted NAT & Symmetric NAT
- Per flow accounting or rate limiting
- DDOS avoidance by rate limiting
- Stateful packet filtering (SPI)
- Patent-pending flow offloading technology for flexible/high performance packet L3/L4 packet processing.
- Multi-WAN load balancing with hardware and software cooperation
- QoS for multimedia traffic
- Within 16 flows, 2 Gbps wire-speed is supported for any packet size.

NOTE: All PPE features mentioned above require software porting to function.

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2.2.3 PDMA/ADMA Features

- Supports 4 Tx descriptor rings and 4 Rx descriptor rings
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8/16/32 32-bit word burst length
- Support LRO(Large Receive Offload) with 1 normal RX ring and 3 LRO RX ring
- Support TSO(TCP Segmentation Offload)

2.2.4 QDMA Features

- Supports 1 Tx descriptor link list from software
- Supports directly Tx packet hardware forwarding from PPE
- Supports 2 Rx descriptor rings
- Configurable 4/8/16/32 32-bit word burst length
- Delayed interrupt
- Support TSO(TCP Segmentation Offload)
- Supports 16 Tx queues
- Per Tx queue forward/drop packet accounting
- Per Tx queue minimum/maximum rate control
- Strict priority arbitration between 16 Tx queues, for under MIN rate traffic
- Round-robin arbitration between 16 Tx queues, for over MIN rate traffic
- 16 Tx queues can be separated into 2 scheduling group
- Supports Random Early Drop with configurable dropping probability
- Tx queue #0~3 support SFQ and DRR scheduling, with virtual queue capability
- Supports up to 1024 virtual queues, those are shared by Tx queue #0~3
- Supports SFQ/DRR hash perturb
- Per virtual queue forward packet / drop packet / forward byte accounting

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2.3 Block Diagram

2.3.1 Frame Engine

2.3.2 PDMA/ADMA

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2.3.3 PDMA, QDMA Descriptor

PDMA Tx Descriptor

SDP : Segment Data Pointer SDL : Segment Data Length LS : Last Segment DDONE : DMA Done. Indicate DMA has transfer the segment pointed by this TX descriptor BURST : when set, the scheduler can not hand-over to other TS queues. Should go on to transmit the next packet	ICO: IP checksum offload enable UCO: UDP checksum offload enable TCO: TCP checksum offload enable TSO:TCP segmentation offload enable FPORT: Force forwarding PSE port INSV: Insert VLAN tag VPRI: VLAN priority tag to be inserted CFI: VLAN Canonical Format Indicator VID: VLAN ID Index

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

SDP0 (32)																															
DDONE	LS0	SDL0 (14)														BURST	LS1	SDL1 (14)													
SDP1 (32)																															
ICO	UCO	TCO	TSO	FPORT (3)			REV (8)								INSV	VPRI (3)			CFI	VID (12)											

PDMA/QDMA Rx Descriptor

SDP : Segment Data Pointer SDL : Segment Data Length (SDL[15:14] PDMA only) LS : Last Segment DDONE : DMA Done. Indicate DMA has transfer the segment pointed by this TX descriptor LRO_AGG_CNT: Final number of aggregated packet in this RX descriptor (PDMA only) LRO_FLUSH_RSN: LRO flush reason (PDMA only) 3'h1 : aggregation timer timout 3'h2 : age timer timout 3'h3 : sequence number out-of-order 3'h4 : timestamp out-of-order 3'h5 : lro rule violation 3'h0 : no flush	VPID: VALN Protocol ID VPRI: VLAN priority tag to be inserted CFI: VLAN Canonical Format Indicator VID: VLAN ID Index FPORT: Force forwarding PSE port PKT_INFO: PacKet Information(6) (when SPORT!=PDMA or QDMA) SPORT: Source Port CRSN: PPE to CPU reason (5'h1F means invalid 5'h1E means PPE bypassed) PPE_Entry: PPE entry number (14'h3FFF means invalid)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

SDP (32)																															
DDONE	LS	SDL[13:0] (14)														TAG	REV (2)		LRO_FLUSH_RSN (PDMA only) (8)			LRO_AGG_CNT(PDMA only) (8)								SDL [15:14] (PDMA only) (2)	
VPID (16)																VPRI (3)			CFI	VID (12)											
FPORT (3)			PKT_INFO (6)					REV	SPORT (3)				CRSN (5)					PPE_ENTRY (14)													

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QDMA Tx Descriptor / Rx Free Descriptor

SDP : Segment Data Pointer NDP: Next Descriptor Pointer SDL : Segment Data Length LS : Last Segment DDONE : Indicate DMA has transfer the segment pointed by thiS TX desc. and change the owner to CPU. BURST : when set, the scheduler can not hand-over to other TS queues. Should go on to transmit the next packet SWC : Desc. From SW forward chain PQID: QDMA TX Physical Queue ID VQID: QDMA TX Virtual Queue ID (VQIDO=0)	PROT: Protocol identification for HW calculating VQ ID (VQIDO=1), (0:L2 bridge /1:IPv4 NAT /2:IPv4 NAPT /3:IPv6 3T /4:IPv6 5T) IPOFST: IP header offset, SDP+IPOFST=pointer to IP header(VQIDO=1) ICO: IP checksum offload enable UCO: UDP checksum offload enable TCO: TCP checksum offload enable TSO:TCP segmentation offload enable FPORT: Force forwarding PSE port VQIDO: VQID offload enable INSV: Insert VLAN tag VPRI: VLAN priority tag to be inserted CFI: VLAN Canonical Format Indicator VID: VLAN ID Index

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	SDP (32)																																desp0
	NDP (32)																																desp1
CPU path VQIDO=0	DDONE	LS	SDL (14)														BURST	SWC	VQID (10)										PQID (4)				desp2
CPU path VQIDO=1	DDONE	LS	SDL (14)														BURST	SWC	IPOFST (7)							PROT (3)			PQID (4)				desp2
HW path	DDONE	LS	SDL (14)														BURST	SWC	PPE_ENTRY[9:0] (10)										PQID (4)				desp2
CPU path	ICO	UCO	TCO	TSO	FPORT (3)			REV (7)							VQIDO	INSV	VPRI (3)			CFI	VID (12)												desp3
HW path	REV (4)				FPORT (3)			REV (25)																									desp3

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2.3.4 QDMA Traffic Shaper Architecture

2.4 Register Definition

Module name: FE Base address: (+1B100000h)

Address	Name	Width	Register Function
1B100000	FE_GLO_CFG	32	Frame Engine Global Configuration
1B100004	FE_RST_GLO	32	Frame Engine Global Reset
1B100008	FE_INT_STATUS	32	Frame Engine Interrupt Status
1B10000C	FE_INT_ENABLE	32	Frame Engine Interrupt Enable
1B100010	FE_FOE_TS_T	32	Frame Engine Time Stamp
1B100014	FE_IPV6_EXT	32	Frame Engine IPv6 Extension Header
1B100018	FE_RATE_COMP	32	Frame Engine Rate Limt Compensation
1B10001C	LRO_ALT_REFRESH_TIMER	32	Reserved
1B100020	FE_INT_GRP	32	Frame Engine Interrupt Group
1B100100	PSE_FQFC_CFG	32	PSE Free Queue Flow Control
1B100108	PSE_IQ_REV1	32	PSE Input Queue Reservation-I
1B10010C	PSE_IQ_REV2	32	PSE Input Queue Reservation-II
1B100110	PSE_IQ_STA1	32	PSE Input Queue Status-I

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1B100114	PSE_IQ_STA2	32	PSE Input Queue Status-II
1B100118	PSE_OQ_STA1	32	PSE Output Queue Status-I
1B10011C	PSE_OQ_STA2	32	PSE Output Queue Status-II
1B100120	PSE_MIR_PORT	32	PSE Mirror Port
1B100124	FE_GLO_MISC	32	
1B100130	FE_GDM_RXID1	32	FE GDM RXID Control 1
1B100134	FE_GDM_RXID2	32	FE GDM RXID Control 2
1B100300	FE_ALT_CF8	32	ALT Entry Base Addr
1B100304	FE_ALT_SGL_CFC	32	ALT Single DW read
1B100308	FE_ALT_SEQ_CFC	32	ALT Sequenctial DW read
1B10030C	FE_ALT_SEQ_CFC_OFS	32	ALT Sequenctial DW read
1B100400	CDMP_IG_CTRL	32	CDM Ingress Control
1B100404	CDMP_EG_CTRL	32	CDM Egress Control
1B100408	CDMP_PPE_GEN	32	CDM PPPoE Generation
1B100500	GDM1_IG_CTRL	32	GDM Ingress Control
1B100504	GDM1_EG_CTRL	32	GDM Egress Control
1B100508	GDM1_MAC_LSB	32	GDM MY_MAC Address LSB
1B10050C	GDM1_MAC_MSB	32	GDM MY_MAC Address MSB
1B100510	GDM1_VLAN_GEN	32	GDM VLAN Generation
1B100800	TX_BASE_PTR_0	32	TX Ring #0 Base Pointer
1B100804	TX_MAX_CNT_0	32	TX Ring #0 Maximum Count
1B100808	TX_CTX_IDX_0	32	TX Ring #0 CPU pointer
1B10080C	TX_DTX_IDX_0	32	TX Ring #0 DMA poitner
1B100810	TX_BASE_PTR_1	32	TX Ring #1 Base Pointer
1B100814	TX_MAX_CNT_1	32	TX Ring #1 Maximum Count
1B100818	TX_CTX_IDX_1	32	TX Ring #1 CPU pointer
1B10081C	TX_DTX_IDX_1	32	TX Ring #1 DMA poitner
1B100820	TX_BASE_PTR_2	32	TX Ring #2 Base Pointer
1B100824	TX_MAX_CNT_2	32	TX Ring #2 Maximum Count
1B100828	TX_CTX_IDX_2	32	TX Ring #2 CPU pointer
1B10082C	TX_DTX_IDX_2	32	TX Ring #2 DMA poitner
1B100830	TX_BASE_PTR_3	32	TX Ring #3 Base Pointer
1B100834	TX_MAX_CNT_3	32	TX Ring #3 Maximum Count
1B100838	TX_CTX_IDX_3	32	TX Ring #3 CPU pointer
1B10083C	TX_DTX_IDX_3	32	TX Ring #3 DMA poitner
1B100900	RX_BASE_PTR_0	32	RX Ring #0 Base Pointer
1B100904	RX_MAX_CNT_0	32	RX Ring #0 Maximum Count
1B100908	RX_CRX_IDX_0	32	RX Ring #0 CPU pointer
1B10090C	RX_DRX_IDX_0	32	RX Ring #0 DMA poitner
1B100910	RX_BASE_PTR_1	32	RX Ring #1 Base Pointer
1B100914	RX_MAX_CNT_1	32	RX Ring #1 Maximum Count
1B100918	RX_CRX_IDX_1	32	RX Ring #1 CPU pointer

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1B10091C	RX_DRX_IDX_1	32	RX Ring #1 DMA poitner
1B100920	RX_BASE_PTR_2	32	RX Ring #2 Base Pointer
1B100924	RX_MAX_CNT_2	32	RX Ring #2 Maximum Count
1B100928	RX_CRX_IDX_2	32	RX Ring #2 CPU pointer
1B10092C	RX_DRX_IDX_2	32	RX Ring #2 DMA poitner
1B100930	RX_BASE_PTR_3	32	RX Ring #3 Base Pointer
1B100934	RX_MAX_CNT_3	32	RX Ring #3 Maximum Count
1B100938	RX_CRX_IDX_3	32	RX Ring #3 CPU pointer
1B10093C	RX_DRX_IDX_3	32	RX Ring #3 DMA poitner
1B100980	ADMA_LRO_CTRL_DW0	32	ADMA Control CRs
1B100984	ADMA_LRO_CTRL_DW1	32	ADMA Control CRs
1B100988	ADMA_LRO_CTRL_DW2	32	ADMA Control CRs
1B10098C	ADMA_LRO_CTRL_DW3	32	ADMA Control CRs
1B100A00	PDMA_INFO	32	PDMA Information
1B100A04	PDMA_GLO_CFG	32	PDMA Global Configuration
1B100A08	PDMA_RST_IDX	32	PDMA Reset Index
1B100A0C	DELAY_INT_CFG	32	Delay Interrupt Configuration
1B100A10	FREEQ_THRES	32	Free Queue Threshold
1B100A20	INT_STATUS	32	Interrupt Status
1B100A28	INT_MASK	32	Interrupt Mask
1B100A30	PDMA_TX_DBG0	32	
1B100A34	PDMA_TX_DBG1	32	
1B100A38	ADMA_RX_DBG0	32	
1B100A3C	ADMA_RX_DBG1	32	
1B100A40	PDMA_INT1_VEC_GRP0	32	PDMA Interrupt Status Group 0
1B100A44	PDMA_INT1_VEC_GRP1	32	PDMA Interrupt Status Group 1
1B100A48	PDMA_INT1_VEC_GRP2	32	PDMA Interrupt Status Group 2
1B100A4C	LRO_ALT_SCORE_DELTA	32	
1B100A50	PDMA_INT_GRP1	32	PDMA Interrupt Group 1 Control
1B100A54	PDMA_INT_GRP2	32	PDMA Interrupt Group 2 Control
1B100A58	LRO_TIMEOUT_FLAG	32	
1B100A5C	LRO_MAX_AGG_TIME	32	max. aggregation time to flush
1B100A60	ADMA_CF8_DBG	32	ADMA debug CFG CF8
1B100A64	ADMA_CFC_RSGL_DBG	32	ADMA debug CFG CFC single
1B100A68	ADMA_CFC_RSEQ_DBG	32	ADMA debug CFG CFC sequential
1B100A6C	ADMA_CF8_CFC	32	ADMA debug offset addr

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	ADDR_DBG		
1B100A70	LRO_RX1_DLY_INT	32	Ring1
1B100A74	LRO_RX2_DLY_INT	32	Ring2
1B100A78	LRO_RX3_DLY_INT	32	Ring3
1B100A7C	LRO_RING_AGG_CNT_INFO	32	
1B100A80	SCH_Q01_CFG	32	Scheduler Configuration for Q0&Q1
1B100A84	SCH_Q23_CFG	32	Scheduler Configuration for Q2&Q3
1B100B00	LRO_RX_RING0_STP_DTP_DW	32	Reserved
1B100B04	LRO_RX_RING0_DIP_DW0	32	Destination IP addr[31:0]
1B100B08	LRO_RX_RING0_DIP_DW1	32	Destination IP addr[63:32]
1B100B0C	LRO_RX_RING0_DIP_DW2	32	Destination IP addr[95:64]
1B100B10	LRO_RX_RING0_DIP_DW3	32	Destination IP addr[127:96]
1B100B2C	LRO_RX_RING0_CTRL_DW2	32	Reserved
1B100B40	LRO_RX_RING1_STP_DTP_DW	32	Source TCP port number
1B100B44	LRO_RX_RING1_DIP_DW0	32	Destination IP addr[31:0]
1B100B48	LRO_RX_RING1_DIP_DW1	32	Destination IP addr[63:32]
1B100B4C	LRO_RX_RING1_DIP_DW2	32	Destination IP addr[95:64]
1B100B50	LRO_RX_RING1_DIP_DW3	32	Destination IP addr[127:96]
1B100B54	LRO_RX_RING1_SIP_DW0	32	Source IP addr[31:0]
1B100B58	LRO_RX_RING1_SIP_DW1	32	Source IP addr[63:32]
1B100B5C	LRO_RX_RING1_SIP_DW2	32	Source IP addr[95:64]
1B100B60	LRO_RX_RING1_SIP_DW3	32	Source IP addr[127:96]
1B100B64	LRO_RX_RING1_CTRL_DW0	32	l2_vlan_vid_l2_l
1B100B68	LRO_RX_RING1_CTRL_DW1	32	RX ring age time[9:0]
1B100B6C	LRO_RX_RING1_CTRL_DW2	32	LRO_MAX_AGGREGATED_CNT_L
1B100B70	LRO_RX_RING1_CTRL_DW3	32	Reserved
1B100B80	LRO_RX_RING2_STP_DTP_DW	32	Source TCP port number
1B100B84	LRO_RX_RING2_DIP_DW0	32	Destination IP addr[31:0]
1B100B88	LRO_RX_RING2_DIP_DW1	32	Destination IP addr[63:32]

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1B100B8C	LRO_RX_RING2_DIP_DW2	32	Destination IP addr[95:64]
1B100B90	LRO_RX_RING2_DIP_DW3	32	Destination IP addr[127:96]
1B100B94	LRO_RX_RING2_SIP_DW0	32	Source IP addr[31:0]
1B100B98	LRO_RX_RING2_SIP_DW1	32	Source IP addr[63:32]
1B100B9C	LRO_RX_RING2_SIP_DW2	32	Source IP addr[95:64]
1B100BA0	LRO_RX_RING2_SIP_DW3	32	Source IP addr[127:96]
1B100BA4	LRO_RX_RING2_CTRL_DW0	32	l2_vlan_vid_l2_l
1B100BA8	LRO_RX_RING2_CTRL_DW1	32	RX ring age time[9:0]
1B100BAC	LRO_RX_RING2_CTRL_DW2	32	LRO_MAX_AGGREGATED_CNT_L
1B100BB0	LRO_RX_RING2_CTRL_DW3	32	Reserved
1B100BC0	LRO_RX_RING3_STP_DTP_DW	32	Source TCP port number
1B100BC4	LRO_RX_RING3_DIP_DW0	32	Destination IP addr[31:0]
1B100BC8	LRO_RX_RING3_DIP_DW1	32	Destination IP addr[63:32]
1B100BCC	LRO_RX_RING3_DIP_DW2	32	Destination IP addr[95:64]
1B100BD0	LRO_RX_RING3_DIP_DW3	32	Destination IP addr[127:96]
1B100BD4	LRO_RX_RING3_SIP_DW0	32	Source IP addr[31:0]
1B100BD8	LRO_RX_RING3_SIP_DW1	32	Source IP addr[63:32]
1B100BDC	LRO_RX_RING3_SIP_DW2	32	Source IP addr[95:64]
1B100BE0	LRO_RX_RING3_SIP_DW3	32	Source IP addr[127:96]
1B100BE4	LRO_RX_RING3_CTRL_DW0	32	l2_vlan_vid_l2_l
1B100BE8	LRO_RX_RING3_CTRL_DW1	32	RX ring age time[9:0]
1B100BEC	LRO_RX_RING3_CTRL_DW2	32	LRO_MAX_AGGREGATED_CNT_L
1B100BF0	LRO_RX_RING3_CTRL_DW3	32	Reserved
1B101400	CDMQ_IG_CTRL	32	CDM VLAN Control
1B101404	CDMQ_EG_CTRL	32	CDM Egress Control
1B101408	CDMQ_PPP_GEN	32	CDM PPPoE Generation
1B101500	GDM2_IG_CTRL	32	GDM Ingress Control
1B101504	GDM2_EG_CTRL	32	GDM Egress Control
1B101508	GDM2_MAC_LSB	32	GDM MY_MAC Address LSB
1B10150C	GDM2_MAC_MSB	32	GDM MY_MAC Address MSB
1B101510	GDM2_VLAN_GE	32	GDM VLAN Generation

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	N		
1B101514	GDM2_FILTER_CRTL	32	GDM Filter Control
1B101518	GDM2_VIDF01	32	GDM VID Filter Control 01
1B10151C	GDM2_VIDF23	32	GDM VID Filter Control 23
1B101800	QTX_CFG_0	32	TX Queue #0 Configuration
1B101804	QTX_SCH_0	32	TX Queue #0 Schedule
1B101808	QTX_HEAD_0	32	TX Queue #0 Head Pointer
1B10180C	QTX_TAIL_0	32	TX Queue #0 Tail Pointer
1B101810	QTX_CFG_1	32	TX Queue #1 Configuration
1B101814	QTX_SCH_1	32	TX Queue #1 Schedule
1B101818	QTX_HEAD_1	32	TX Queue #1 Head Pointer
1B10181C	QTX_TAIL_1	32	TX Queue #1 Tail Pointer
1B101820	QTX_CFG_2	32	TX Queue #2 Configuration
1B101824	QTX_SCH_2	32	TX Queue #2 Schedule
1B101828	QTX_HEAD_2	32	TX Queue #2 Head Pointer
1B10182C	QTX_TAIL_2	32	TX Queue #2 Tail Pointer
1B101830	QTX_CFG_3	32	TX Queue #3 Configuration
1B101834	QTX_SCH_3	32	TX Queue #3 Schedule
1B101838	QTX_HEAD_3	32	TX Queue #3 Head Pointer
1B10183C	QTX_TAIL_3	32	TX Queue #3 Tail Pointer
1B101840	QTX_CFG_4	32	TX Queue #4 Configuration
1B101844	QTX_SCH_4	32	TX Queue #4 Schedule
1B101848	QTX_HEAD_4	32	TX Queue #4 Head Pointer
1B10184C	QTX_TAIL_4	32	TX Queue #4 Tail Pointer
1B101850	QTX_CFG_5	32	TX Queue #5 Configuration
1B101854	QTX_SCH_5	32	TX Queue #5 Schedule
1B101858	QTX_HEAD_5	32	TX Queue #5 Head Pointer
1B10185C	QTX_TAIL_5	32	TX Queue #5 Tail Pointer
1B101860	QTX_CFG_6	32	TX Queue #6 Configuration
1B101864	QTX_SCH_6	32	TX Queue #6 Schedule
1B101868	QTX_HEAD_6	32	TX Queue #6 Head Pointer
1B10186C	QTX_TAIL_6	32	TX Queue #6 Tail Pointer
1B101870	QTX_CFG_7	32	TX Queue #7 Configuration
1B101874	QTX_SCH_7	32	TX Queue #7 Schedule
1B101878	QTX_HEAD_7	32	TX Queue #7 Head Pointer
1B10187C	QTX_TAIL_7	32	TX Queue #7 Tail Pointer
1B101880	QTX_CFG_8	32	TX Queue #8 Configuration
1B101884	QTX_SCH_8	32	TX Queue #8 Schedule
1B101888	QTX_HEAD_8	32	TX Queue #8 Head Pointer
1B10188C	QTX_TAIL_8	32	TX Queue #8 Tail Pointer
1B101890	QTX_CFG_9	32	TX Queue #9 Configuration
1B101894	QTX_SCH_9	32	TX Queue #9 Schedule
1B101898	QTX_HEAD_9	32	TX Queue #9 Head Pointer
1B10189C	QTX_TAIL_9	32	TX Queue #9 Tail Pointer
1B1018A0	QTX_CFG_10	32	TX Queue #10 Configuration
1B1018A4	QTX_SCH_10	32	TX Queue #10 Schedule

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1B1018A8	QTX_HEAD_10	32	TX Queue #10 Head Pointer
1B1018AC	QTX_TAIL_10	32	TX Queue #10 Tail Pointer
1B1018B0	QTX_CFG_11	32	TX Queue #11 Configuration
1B1018B4	QTX_SCH_11	32	TX Queue #11 Schedule
1B1018B8	QTX_HEAD_11	32	TX Queue #11 Head Pointer
1B1018BC	QTX_TAIL_11	32	TX Queue #11 Tail Pointer
1B1018C0	QTX_CFG_12	32	TX Queue #12 Configuration
1B1018C4	QTX_SCH_12	32	TX Queue #12 Schedule
1B1018C8	QTX_HEAD_12	32	TX Queue #12 Head Pointer
1B1018CC	QTX_TAIL_12	32	TX Queue #12 Tail Pointer
1B1018D0	QTX_CFG_13	32	TX Queue #13 Configuration
1B1018D4	QTX_SCH_13	32	TX Queue #13 Schedule
1B1018D8	QTX_HEAD_13	32	TX Queue #13 Head Pointer
1B1018DC	QTX_TAIL_13	32	TX Queue #13 Tail Pointer
1B1018E0	QTX_CFG_14	32	TX Queue #14 Configuration
1B1018E4	QTX_SCH_14	32	TX Queue #14 Schedule
1B1018E8	QTX_HEAD_14	32	TX Queue #14 Head Pointer
1B1018EC	QTX_TAIL_14	32	TX Queue #14 Tail Pointer
1B1018F0	QTX_CFG_15	32	TX Queue #15 Configuration
1B1018F4	QTX_SCH_15	32	TX Queue #15 Schedule
1B1018F8	QTX_HEAD_15	32	TX Queue #15 Head Pointer
1B1018FC	QTX_TAIL_15	32	TX Queue #15 Tail Pointer
1B101900	QRX_BASE_PTR_0	32	RX Ring #0 Base Pointer
1B101904	QRX_MAX_CNT_0	32	RX Ring #0 Maximum Count
1B101908	QRX_CRX_IDX_0	32	RX Ring #0 CPU pointer
1B10190C	QRX_DRX_IDX_0	32	RX Ring #0 DMA poitner
1B101910	QRX_BASE_PTR_1	32	RX Ring #1 Base Pointer
1B101914	QRX_MAX_CNT_1	32	RX Ring #1 Maximum Count
1B101918	QRX_CRX_IDX_1	32	RX Ring #1 CPU pointer
1B10191C	QRX_DRX_IDX_1	32	RX Ring #1 DMA poitner
1B101980	VQTX_TB_BASE_0	32	TX Virtual Queue Table #0 Base Address
1B101984	VQTX_TB_BASE_1	32	TX Virtual Queue Table #1 Base Address
1B101988	VQTX_TB_BASE_2	32	TX Virtual Queue Table #2 Base Address
1B10198C	VQTX_TB_BASE_3	32	TX Virtual Queue Table #3 Base Address
1B101A00	QDMA_INFO	32	QDMA Information
1B101A04	QDMA_GLO_CFG	32	QDMA Global Configuration
1B101A08	QDMA_RST_IDX	32	QDMA Reset Index
1B101A0C	QDMA_DELAY_INT	32	Delay Interrupt Configuration
1B101A10	QDMA_FC_THRES	32	Flow ControlThreshold

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1B101A14	QDMA_TX_SCH	32	TX Scheduler Rate Control
1B101A18	QDMA_INT_STS	32	Interrupt Status
1B101A1C	QDMA_INT_MASK	32	Interrupt Mask
1B101A20	QDMA_INT_GRP1	32	QDMA Interrupt Group 1 Control
1B101A24	QDMA_INT_GRP2	32	QDMA Interrupt Group 2 Control
1B101A2C	QDMA_DROP_PREC	32	QDMA Drop by FFA Percentage Control
1B101A30	QDMA_TEST	32	Test Mode
1B101A34	QDMA_DMA	32	QDMA DMA FSM
1B101A38	QDMA_BMU	32	QDMA BMU FSM
1B101A3C	QDMA_MON	32	QDMA Monitor for Error Interrupt Event
1B101A40	QDMA_HRED1	32	QDMA HW RED Distribution - I
1B101A44	QDMA_HRED2	32	QDMA HW RED Distribution - II
1B101A48	QDMA_SRED1	32	QDMA SW RED Distribution - I
1B101A4C	QDMA_SRED2	32	QDMA SW RED Distribution - II
1B101A50	QTX_Q0MIN_BK	32	QDMA Queue #0 Min. Bucket
1B101A54	QTX_Q1MIN_BK	32	QDMA Queue #1 Min. Bucket
1B101A58	QTX_Q2MIN_BK	32	QDMA Queue #2 Min. Bucket
1B101A5C	QTX_Q3MIN_BK	32	QDMA Queue #3 Min. Bucket
1B101A60	QTX_Q0MAX_BK	32	QDMA Queue #0 Max. Bucket
1B101A64	QTX_Q1MAX_BK	32	QDMA Queue #1 Max. Bucket
1B101A68	QTX_Q2MAX_BK	32	QDMA Queue #2 Max. Bucket
1B101A6C	QTX_Q3MAX_BK	32	QDMA Queue #3 Max. Bucket
1B101A70	QDMA_INT_STS_G0	32	QDMA Interrupt Status Group 0
1B101A74	QDMA_INT_STS_G1	32	QDMA Interrupt Status Group 1
1B101A78	QDMA_INT_STS_G2	32	QDMA Interrupt Status Group 2
1B101A80	VQTX_GLO	32	TX Virtual Queue Global Configuration
1B101A8C	VQTX_INVLD_PTR	32	TX Virtual Queue Invalid Pointer
1B101A90	VQTX_NUM	32	Number of TX Virtual Queue Configuration
1B101A98	VQTX_SCH	32	TX Virtual Queue Schedule Configuration
1B101AA0	VQTX_HASH_CFG	32	TX Virtual Queue Hash Configuration
1B101AA4	VQTX_HASH_SD	32	TX Virtual Queue Hash Seed
1B101AB0	VQTX_VLD_CFG	32	TX Virtual Queue Valid Configuration
1B101ABC	VQTX_MIB_IF	32	TX Virtual Queue MIB Interface
1B101AC0	VQTX_MIB_PCNT	32	TX Virtual Queue MIB Packet Count
1B101AC4	VQTX_MIB_BCNT0	32	TX Virtual Queue MIB Byte Count 0
1B101AC8	VQTX_MIB_BCNT1	32	TX Virtual Queue MIB Byte Count 1
1B101ACC	VQTX_MIB_DPCNT	32	TX Virtual Queue MIB Drop Packet Count
1B101AD0	QTX_MIB_PCNT	32	TX Queue MIB Forward Packet Count

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1B101AD4	QTX_MIB_DPCNT	32	**TX Queue MIB Dropped Packet Count**
1B101B00	QTX_CTX_PTR	32	**TX Forward CPU Pointer**
1B101B04	QTX_DTX_PTR	32	**TX Forward DMA Pointer**
1B101B08	QTX_FWD_CNT	32	**TX Forward DMA Counter**
1B101B10	QTX_CRX_PTR	32	**TX Release CPU Pointer**
1B101B14	QTX_DRX_PTR	32	**TX Release DMA Pointer**
1B101B18	QTX_RLS_CNT	32	**TX Release DMA Counter**
1B101B20	QDMA_FQ_HEAD	32	**Free Page Head Pointer**
1B101B24	QDMA_FQ_TAIL	32	**Free Page Tail Pointer**
1B101B28	QDMA_FQ_CNT	32	**Free Page Counter**
1B101B2C	QDMA_FQ_BLEN	32	**Free Page Buffer Length**
1B101B80	QDMA_RATE_EXP0	32	**QDMA Scheduler Rate Exponent 0**
1B101B84	QDMA_RATE_EXP1	32	**QDMA Scheduler Rate Exponent 1**
1B101B88	QDMA_RATE_EXP2	32	**QDMA Scheduler Rate Exponent 2**
1B101B8C	QDMA_RATE_EXP3	32	**QDMA Scheduler Rate Exponent 3**
1B101B90	QDMA_RATE_EXP4	32	**QDMA Scheduler Rate Exponent 4**
1B101B94	QDMA_RATE_EXP5	32	**QDMA Scheduler Rate Exponent 5**
1B101BA0	VQTX_DEP_TH	32	**QDMA Virtual Queue Depth Threshold**
1B101BA8	VQTX_DEP_TH2	32	**QDMA Virtual Queue Depth Threshold**

1B100000 FE_GLO_CFG Frame Engine Global Configuration 810000B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXT_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINK_DWN								L2_SPACE				INF_SPACE			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:16	EXT_TPID	**Extended VLAN TPID** User-defined TPID except for 0x8100, 0x88a8. [note] This TPID field is used by CDM/GDM RX direction.
15:8	LINK_DWN	**Disable PSE Port** When PSE port is not valid on the Frame Engine, user is suggested to disable the corresponding port.
7:4	L2_SPACE	**L2 space** The space unit is 8 bytes.
3:0	INF_SPACE	**PKT_INFO space** The space unit is 8 bytes. [Note1*] Per received packet has already occupied 8 bytes(1 unit) by default. The actual PKT_INFO space is equal to (INF_SPACE + 1)

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Bit(s)	Name	Description
		[Note2*] (L2_SPACE + INF_SPACE + 1) <= 0xF

1B100004 FE_RST_GLO Frame Engine Global Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0[28:13]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0[12:0]													PSE_RAM	PSE_MEM_EN	PSE_RESET
Type	DC													RW	RW	W1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	RESV0	**Reserved**
2	PSE_RAM	**PSE accessable RAM mode** [note*1] when this bit is reset, PSE packet memory is only accessable by Pbus (0xA000~0xDFFF). [note*2] when this bit is set, PSE packet memory is only accessable by Pbus (0x8000~0xDFFF) 0: Only 8KB PSE memory is left for iNIC initialization. 1: Make the whole PSE memory be used for Pbus access
1	PSE_MEM_EN	**PSE access enable** 0: disable 1: Enable PSE memory is accessable by PBUs
0	PSE_RESET	**PSE soft reset (self-cleared)** [note*1] Whenever SW set this bit, PSE will be initialized again and enter the normal mode. 0: invalid 1: Write 1 to reset PSE

1B100008 FE_INT_STATUS Frame Engine Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	REV1		MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	W1C	DC	W1C	W1C	DC		W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON							
Type	DC	W1C	W1C	W1C	DC		W1C	W1C	W1C							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	**MIB counter is almost full on PPE**

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Bit(s)	Name	Description
30	REV0	**Reserved**
29	GDM2_AF	**MIB counter is almost full on GDM2**
28	GDM1_AF	**MIB counter is almost full on GDM1**
27:26	REV1	**Reserved**
25	MAC2_LINK	**Link Status Change on MAC2**
24	MAC1_LINK	**Link Status Change on MAC1**
23	GDM2_ERR	**Packet error (checksum, length, ..etc) on GDM2** Includign FIFO overflow, checksum error, undersize, oversize
22	GDM2_CRC	**Packet CRC error on GDM2**
21	GDM1_ERR	**Packet error (checksum, length, ..etc) on GDM1** Includign FIFO overflow, checksum error, undersize, oversize
20	GDM1_CRC	**Packet CRC error on GDM1**
19	RFIFO_UF	**Ring FIFO Underrun Defect**
18	RFIFO_OV	**Ring FIFO Overflow Defect**
17	INFIFO_GET_ERR	**IN FIFO Get Defect**
16	AFIFO_GET_ERR	**ASYNC FIFO Get Defect**
15	REV2	**Reserved**
14	CDM_TSO_ALIGN	**Detect EOF Alignment**
13	CDM_TSO_ILLEGAL	**Ignored illegal packet on CDM TSO**
12	CDM_TSO_FAIL	**TSO Fail on CDM**
11:10	REV3	**Reserved**
9	PSE_DROP	**Packet drop by PSE**
8	FQ_EMPTY	**PSE free queue is empty**
7:0	PSE_FC_ON	**PSE PORT flow control is asserted** PSE port[n] enables the flow control.

1B10000C **FE_INT_ENABLE** **Frame Engine Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	REV1		MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON							
Type	RW	RW	RW	RW	RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	
30	REV0	
29	GDM2_AF	

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Bit(s)	Name	Description
28	GDM1_AF	
27:26	REV1	
25	MAC2_LINK	
24	MAC1_LINK	
23	GDM2_ERR	
22	GDM2_CRC	
21	GDM1_ERR	
20	GDM1_CRC	
19	RFIFO_UF	
18	RFIFO_OV	
17	INFIFO_GET_ERR	
16	AFIFO_GET_ERR	
15	REV2	
14	CDM_TSO_ALIGN	
13	CDM_TSO_ILLEGAL	
12	CDM_TSO_FAIL	
11:10	REV3	
9	PSE_DROP	
8	FQ_EMPTY	
7:0	PSE_FC_ON	

1B100010 FE_FOE_TS_T Frame Engine Time Stamp 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FOE_TS_T															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RESV0	**Reserved**
15:0	FOE_TS_T	**Time stamp** Time stamp unit is 1 sec. [Note] This timer is drived by free-running 125MHz clock

1B100014 FE_IPV6_EXT Frame Engine IPv6 Extension Header 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IP6_EXT3								IP6_EXT2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IP6_EXT1								IP6_EXT0							
Type	RW								RW							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	IP6_EXT3	**IPv6 extension header #3**
23:16	IP6_EXT2	**IPv6 extension header #2**
15:8	IP6_EXT1	**IPv6 extension header #1**
7:0	IP6_EXT0	**IPv6 extension header #0**

1B100018 FE_RATE_COMP Frame Engine Rate Limt Compensation 00001818

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_RATE_MINUS	DMA_RATE_BYTE							PSE_RATE_MINUS	PSE_RATE_BYTE						
Type	RW	RW							RW	RW						
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15	DMA_RATE_MINUS	1'b0: a specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE 1'b1: a specific byte count is subtracted from the incoming frame length.
14:8	DMA_RATE_BYTE	**Byte number for rate control** The byte number should be subtraced while calculating the rate limit.
7	PSE_RATE_MINUS	1'b0: a specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE 1'b1: a specific byte count is subtracted from the incoming frame length.
6:0	PSE_RATE_BYTE	**Byte number for rate control** The byte number should be subtraced while calculating the rate limit.

1B10001C LRO_ALT_REFRESH_TIMER Reserved 001FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0											LRO_ALT_TICK_TIMER				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LRO_ALT_RFSH_TIMER															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:21	REV0	**Reserved**
20:16	LRO_ALT_TICK_TIME	**An internal gernerated timout timer based on top's 25us tick_time. When**

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Bit(s)	Name	Description
	R	**timeout, it will trigger a tick to LRO_ATL_REFRESH_TIMER to count forward.** If set to all zero : timer is disabled and the trigger is the copy of raw 25us time_tick instead.
15:0	LRO_ALT_RFSH_TIMER	**An internal gernerated timout timer based on time_tick from internal gernerated timer LRO_ALT_TICK_TIMER. When timeout, it will trigger a timeout signal to reset both tables and at the same time open a replacement allowable window to give new flow to compete with existed flows to win the RX ring for LRO.** If set to all zeros : timer is disabled and replacement allowable window is always opened for new flows.

1B100020 FE_INT_GRP Frame Engine Interrupt Group 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_G2_ASG				QDMA_INT_G1_ASG				QDMA_INT_G0_ASG				PDMA_INT_G2_ASG			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_G1_ASG				PDMA_INT_G0_ASG								FE_MISC_INT_ASG			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
31:28	QDMA_INT_G2_ASG	**QDMA group 2 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
27:24	QDMA_INT_G1_ASG	**QDMA group 1 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
23:20	QDMA_INT_G0_ASG	**QDMA group 0 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
19:16	PDMA_INT_G2_ASG	**PDMA group 2 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
15:12	PDMA_INT_G1_ASG	**PDMA group 1 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved
11:8	PDMA_INT_G0_ASG	**PDMA group 0 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved

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Bit(s)	Name	Description
3:0	FE_MISC_INT_ASG	**Frame engine misc. interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] Others: Reserved

1B100100 PSE_FQFC_CFG PSE Free Queue Flow Control 6060000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_PCNT								FQ_MAX_PCNT							
Type	RO								RW							
Reset	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PPE_VIQ								PPE_LTH							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31:24	FQ_PCNT	**Free queue page count**
23:16	FQ_MAX_PCNT	**Maximum free Q page count.** Please reset PSE after re-programming this register
15:8	PPE_VIQ	**PPE virtual input queue depth** This value is equal to SUM(P[n]_IQ_PCNT - P[n]_IQ_RES).
7:0	PPE_LTH	**Page count low threshold for PPE port** When the page count of PPE port is lower than PPE_LTH, PSE will disable flow control.

1B100108 PSE_IQ_REV1 PSE Input Queue Reservation-I 000C0C08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P2_IQ_RES							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_IQ_RES								P0_IQ_RES							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:16	P2_IQ_RES	**Port 2 virtual input Q reservation** [note*] After the flow control of GDM1/GDM2 is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
15:8	P1_IQ_RES	**Port 1 virtual input Q reservation** [note*] After the flow control of GDM1/GDM2 is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
7:0	P0_IQ_RES	**Port 0 virtual input Q reservation** When (PPE_VIQ > PPE_HTH) and P[n]_IQ_PCNT > P[n]_IQ_RES), the corresponding port will enable the flow control.

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1B10010C PSE_IQ_REV2 PSE Input Queue Reservation-II 10080818

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FREE_DROP								P6_IQ_RES							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_IQ_RES								PPE_HTH							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:24	FREE_DROP	**Free Buffer Drop Threshold**
23:16	P6_IQ_RES	**Port 6 virtual input Q reservation**
15:8	P5_IQ_RES	**Port 5 virtual input Q reservation**
7:0	PPE_HTH	**Page count reservation for PPE port** When PPE_VIQ is bigger than PPE_HTH, PSE will check per port input queue depth to enable flow control.

1B100110 PSE_IQ_STA1 PSE Input Queue Status-I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P2_IQ_PCNT							
Type	DC								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_IQ_PCNT								P0_IQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:16	P2_IQ_PCNT	**Port 2 virtual input Q page count**
15:8	P1_IQ_PCNT	**Port 1 virtual input Q page count**
7:0	P0_IQ_PCNT	**Port 0 virtual input Q page count**

1B100114 PSE_IQ_STA2 PSE Input Queue Status-II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P6_IQ_PCNT							
Type	DC								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_IQ_PCNT								REV1							
Type	RO								DC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**

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Bit(s)	Name	Description
23:16	P6_IQ_PCNT	**Port 6 virtual input Q page count**
15:8	P5_IQ_PCNT	**Port 5 virtual input Q page count**
7:0	REV1	**Reserved**

1B100118 PSE_OQ_STA1 PSE Output Queue Status-I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P2_OQ_PCNT							
Type	DC								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1_OQ_PCNT								P0_OQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:16	P2_OQ_PCNT	**Port 2 output Q page count**
15:8	P1_OQ_PCNT	**Port 1 output Q page count**
7:0	P0_OQ_PCNT	**Port 0 output Q page count**

1B10011C PSE_OQ_STA2 PSE Output Queue Status-II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								REV1							
Type	DC								DC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5_IQ_PCNT								PPE_OQ_PCNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:16	REV1	**Reserved**
15:8	P5_IQ_PCNT	**Port 5 output Q page count**
7:0	PPE_OQ_PCNT	**PPE output Q page count**

1B100120 PSE_MIR_PORT PSE Mirror Port 00777777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								P5_MIR_PX				REV1			
Type	DC								RW				DC			
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2				P2_MIR_PX				P1_MIR_PX				P0_MIR_PX			
Type	DC				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

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Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:20	P5_MIR_PX	**Port 5 Mirror Port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
19:16	REV1	**Reserved**
15:12	REV2	**Reserved**
11:8	P2_MIR_PX	**Port 2 Mirror Port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
7:4	P1_MIR_PX	**Port 1 Mirror Port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
3:0	P0_MIR_PX	**Port 0 Mirror Port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved

1B100124 FE_GLO_MISC **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[29:14]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[13:0]														LRO_ALT_LRU_TBL_MISC_C	CDM_LRO_FS_FSM_PAUSE

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															TRL_EN	
Type	RW														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:2	REV0	**Reserved**
1	LRO_ALT_LRU_TBL_MISC_CTRL_EN	1: disable ineligible flow to update LRU table, 0: enable
0	CDM_LRO_FS_FSM_PAUSE	**pause cdm_lro_fs_fsm to process next packet from PSE** 1: pause cdm_lro_fs_fsm to process next packet from PSE

1B100130 FE_GDM_RXID1 FE GDM RXID Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_VLAN_PRI7_RXID_SEL		GDM_VLAN_PRI6_RXID_SEL		GDM_VLAN_PRI5_RXID_SEL		GDM_VLAN_PRI4_RXID_SEL		GDM_VLAN_PRI3_RXID_SEL		GDM_VLAN_PRI2_RXID_SEL		GDM_VLAN_PRI1_RXID_SEL		GDM_VLAN_PRI0_RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV										GDM_TCP_ACK_RXID_SEL		GDM_TCP_ACK_WZPC	GDM_RXID_PRI_SEL		
Type	DC										RW		RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	GDM_VLAN_PRI7_RXID_SEL	**GDM RXID Select for VLAN Priority = 7** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
29:28	GDM_VLAN_PRI6_RXID_SEL	**GDM RXID Select for VLAN Priority = 6** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
27:26	GDM_VLAN_PRI5_RXID_SEL	**GDM RXID Select for VLAN Priority = 5** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
25:24	GDM_VLAN_PRI4_RXID_SEL	**GDM RXID Select for VLAN Priority = 4** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
23:22	GDM_VLAN_PRI3_RXID_SEL	**GDM RXID Select for VLAN Priority = 3** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
21:20	GDM_VLAN_PRI2_RX	**GDM RXID Select for VLAN Priority = 2**

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Bit(s)	Name	Description
	ID_SEL	2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
19:18	GDM_VLAN_PRI1_RX ID_SEL	**GDM RXID Select for VLAN Priority = 1** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
17:16	GDM_VLAN_PRI0_RX ID_SEL	**GDM RXID Select for VLAN Priority = 0** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
15:6	REV	
5:4	GDM_TCP_ACK_RXI D_SEL	**GDM RXID Select for TCP ACK** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
3	GDM_TCP_ACK_WZ PC	**GDM TCP ACK with zero payload check (L3 payload = L4 header)**
2:0	GDM_RXID_PRI_SEL	**GDM RXID Select Priority Setting** Select Priority by PID/STAG, VLAD_PRI, and TCP_ACK 3'b000: PID/STAG 3'b001: VLAN_PRI --> PID/STAG 3'b010: TCP_ACK --> PID/STAG 3'b011: VLAN_PRI --> TCP_ACK --> PID/STAG 3'b100: TCP_ACK --> VLAN_PRI --> PID/STAG

1B100134 FE_GDM_RXID2 FE GDM RXID Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_STAG7 _RXID_SEL		GDM_STAG6 _RXID_SEL		GDM_STAG5 _RXID_SEL		GDM_STAG4 _RXID_SEL		GDM_STAG3 _RXID_SEL		GDM_STAG2 _RXID_SEL		GDM_STAG1 _RXID_SEL		GDM_STAG0 _RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV												GDM_PID2_R XID_SEL		GDM_PID1_ RXID_SEL	
Type	DC												RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	GDM_STAG7_RXID_ SEL	**GDM RXID Select for STAG = 7** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
29:28	GDM_STAG6_RXID_ SEL	**GDM RXID Select for STAG = 6** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)

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Bit(s)	Name	Description
27:26	GDM_STAG5_RXID_SEL	**GDM RXID Select for STAG = 5** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
25:24	GDM_STAG4_RXID_SEL	**GDM RXID Select for STAG = 4** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
23:22	GDM_STAG3_RXID_SEL	**GDM RXID Select for STAG = 3** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
21:20	GDM_STAG2_RXID_SEL	**GDM RXID Select for STAG = 2** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
19:18	GDM_STAG1_RXID_SEL	**GDM RXID Select for STAG = 1** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
17:16	GDM_STAG0_RXID_SEL	**GDM RXID Select for STAG = 0** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
15:4	REV	
3:2	GDM_PID2_RXID_SEL	**GDM RXID Select for GDM2 (Port ID = 2)** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)
1:0	GDM_PID1_RXID_SEL	**GDM RXID Select for GDM1 (Port ID = 1)** 2'b00: Select PDMA RX Ring 0 (RXID=0) 2'b01: Select PDMA RX Ring 1 (RXID=1) 2'b10: Select PDMA RX Ring 2 (RXID=2) 2'b11: Select PDMA RX Ring 3 (RXID=3)

1B100300 FE_ALT_CF8 ALT Entry Base Addr 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FE_ALT_CF8_DBG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_ALT_CF8_DBG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	FE_ALT_CF8_DBG	**Set base address to read Auto-Learn Table double words.**

1B100304 FE_ALT_SGL_CFC ALT Single DW read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FE_ALT_CFC_RSGL_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_ALT_CFC_RSGL_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FE_ALT_CFC_RSGL_DBG	**read 1 DW of Auto-Learn Table from address set in CF8 double words.**

1B100308 FE_ALT_SEQ_CFC ALT Sequenctial DW read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FE_ALT_CFC_RSEQ_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_ALT_CFC_RSEQ_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FE_ALT_CFC_RSEQ_DBG	**read 1 DW of Auto-Learn Table from address set in CF8 double words for the first time and offset 1 DW to base address for getting next DW by read SEQ_CFC without re-configuring CF8.**

1B10030C FE_ALT_SEQ_CFC_OFS ALT Sequenctial DW read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FE_ALT_CFC_RSEQ_OFS_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_ALT_CFC_RSEQ_OFS_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FE_ALT_CFC_RSEQ_OFS_DBG	**{8'h0, {cfc_rsgl_dw_addr, 1'b0}, {cfc_rseg_dw_addr, 1'b0}, {cf8_raddr_dw_offset, 1'b0}}**

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1B100400 CDMP_IG_CTRL CDM Ingress Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0															STAG_EN
Type	DC															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
15:1	REV0	**Reserved**
0	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from CPU . 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.

1B100404 CDMP_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[30:15]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[14:0]															UNTAG_EN
Type	DC															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:1	REV0	**Reserved**
0	UNTAG_EN	**VLAN untag** Untag the egress packets which are transmitted from CDM to CPU 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged

1B100408 CDMP_PPE_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															PPP_INS
Type	DC															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	REV0	**Reserved**
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

1B100500 GDM1_IG_CTRL GDM Ingress Control 00717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0						INSV_EN	STAG_EN	REV1	GDM_ICS_EN	GDM_TCS_EN	GDM_UCS_EN	DROP_256B	REV2		STRP_CRC
Type	DC						RW	RW	DC	RW	RW	RW	RW	DC		RW
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:26	REV0	**Reserved**
25	INSV_EN	**VLAN insertion** Insert Port VID on the received packets on the corresponding GDM port. 0: disable 1: Insert 4-byte VLAN tag after Source Address
24	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from GDM port. 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.
23	REV1	**Reserved**
22	GDM_ICS_EN	**IPv4 header checksum error drop** 0: checksum error status reported on RX descriptor (IP4F) 1: checksum error packet will be dropped
21	GDM_TCS_EN	**TCP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
20	GDM_UCS_EN	**UDP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
19	DROP_256B	**A special mode to drop packets with payload > 256-bytes** 0: Drop packets according to the standard Ethernet frame length limitation. 1: Dopr packets with payloa > 256 bytes
18:17	REV2	**Reserved**
16	STRP_CRC	**GDM RX CRC Stripping** 1'b: Disable GDM RX CRC stripping 1'b1: Enable GDM RX CRC stripping
15:12	MYMAC_DP	**MY_MAC frames destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved

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Bit(s)	Name	Description
		4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
11:8	BC_DP	**Broadcast frame destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
7:4	MC_DP	**Multicast frame destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
3:0	UN_DP	**Other frame destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved

1B100504 GDM1_EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	UNTAG_EN	DIS_PAD	DIS_CRC	REV1			SHPR_EN	BK_SIZE							
Type	DC	RW	RW	RW	DC			RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK	REV2	TK_RATE													
Type	RW	DC	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	
30	UNTAG_EN	**VLAN untagging** Untagg the egress packets which are transmitted from GDM. 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged

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Bit(s)	Name	Description
29	DIS_PAD	**GMAC Tx padding fucntion** 1'b0: Enable GMAC Tx padding 1'b1: Disable GMAC Tx padding
28	DIS_CRC	**GMAC TX CRC generation** 1'b0: Enable GMAC Tx CRC generation 1'b1: Disable GMAC Tx CRC generation
27:25	REV1	**Reserved**
24	SHPR_EN	**GDM output shaper enable** 1'b0: Disable 1'b1: Enable
23:16	BK_SIZE	**GDM output shaper bucket size.** This unit is 1K-byte
15	TK_TICK	**GDM shaper token period** 1'b0: GDM shaper add token every 1ms 1'b1: GDM shaper add token every 20us
14	REV2	**Reserved**
13:0	TK_RATE	**GDM output shaper token rate** The unit is 8-Byte/ms or 8-Byte/20us according to TK_TICK.

1B100508 GDM1_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	**MY_MAC Address [31:0]**

1B10050C GDM1_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RESV0	**Reserved**
15:0	MAC_ADR	**MY_MAC Address [47:32]**

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1B100510 GDM1_VLAN_GEN GDM VLAN Generation 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	**Inserted VLAN TPID**
15:13	GDM_PRI	**Inserted PRI**
12	GDM_CFI	**Inserted CFI**
11:0	GDM_VID	**Inserted VLAN ID**

1B100800 TX_BASE_PTR0 TX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100804 TX_MAX_CNT_0 TX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

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1B100808 TX_CTX_IDX_0 TX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_CTX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1B10080C TX_DTX_IDX_0 TX Ring #0 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_DTX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

1B100810 TX_BASE_PTR_1 TX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100814 TX_MAX_CNT_1 TX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**TX_MAX_CNT**											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

1B100818 TX_CTX_IDX_1 TX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**TX_CTX_IDX**											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1B10081C TX_DTX_IDX_1 TX Ring #1 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**TX_DTX_IDX**											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

1B100820 TX_BASE_PTR_2 TX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX_BASE_PTR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_BASE_PTR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100824 TX_MAX_CNT_2 TX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

1B100828 TX_CTX_IDX_2 TX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_CTX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1B10082C TX_DTX_IDX_2 TX Ring #2 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_DTX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

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1B100830 TX_BASE_PTR_3 TX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

1B100834 TX_MAX_CNT_3 TX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

1B100838 TX_CTX_IDX_3 TX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				TX_CTX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1B10083C TX_DTX_IDX_3 TX Ring #3 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**TX_DTX_IDX**											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

1B100900 RX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RX_BASE_PTR[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_BASE_PTR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #0 (4-DW aligned address)**

1B100904 RX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**RX_MAX_CNT**											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #0**

1B100908 RX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**RX_CRX_IDX**											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10090C RX_DRX_IDX_0 RX Ring #0 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_DRX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

1B100910 RX_BASE_PTR_1 RX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #0 (4-DW aligned address)**

1B100914 RX_MAX_CNT_1 RX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**

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Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #0**

1B100918 RX_CRX_IDX_1 RX Ring #1 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_CRX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10091C RX_DRX_IDX_1 RX Ring #1 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_DRX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

1B100920 RX_BASE_PTR_2 RX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #2 (4-DW aligned address)**

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1B100924 RX_MAX_CNT_2 RX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #0**

1B100928 RX_CRX_IDX_2 RX Ring #2 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_CRX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10092C RX_DRX_IDX_2 RX Ring #2 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_DRX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

1B100930 RX_BASE_PTR_3 RX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR[31:16]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX_BASE_PTR[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #3 (4-DW aligned address)**

1B100934 RX_MAX_CNT_3 RX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**RX_MAX_CNT**											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #0**

1B100938 RX_CRX_IDX_3 RX Ring #3 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**RX_CRX_IDX**											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10093C RX_DRX_IDX_3 RX Ring #3 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REV[19:4]**															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[3:0]**				**RX_DRX_IDX**											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

1B100980 **ADMA_LRO_CTRL_DW0** **ADMA Control CRs** **00800080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_RING_RELINGUISH_DONE			LRO_RING_RELINGUISH_REQ			REV0		cr_lro_l4_ctrl_psh_en	cr_lro_alt_rplc_mode	cr_lro_alt_score_mode	first_ineligible_pkt_redirect_en	REV1[11:8]			
Type	RO			RW			RW		RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1[7:0]								L3_CKS_UPD_EN	LRO_CRSN_BNW	LRO_DLY_INT_EN	RXD_PREFETCH_EN	MULTIPLE_RXD_PREFETCH_EN	MULTIPLE_NON_LRO_RX_RING_EN	LRO_IPv6_EN	LRO_EN
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	LRO_RING_RELINGUISH_DONE	**it represent adma has relinguished ring3/ring2/ ring1**
28:26	LRO_RING_RELINGUISH_REQ	**{ring3, ring2, ring1}, FW need to flush aggregated packets if any, self-cleared by "LRO ring relinguish"**
25:24	REV0	**to adjust each lro_auto_learn ring's packet count in adma**
23	cr_lro_l4_ctrl_psh_en	0: disable l4 psh lro elilgibility check, 1 : push asserted is lro ineligible
22	cr_lro_alt_rplc_mode	0: replace driven by timeout, 1 : replace driven by new packet
21	cr_lro_alt_score_mode	0: thruput(byte count) 1: packet count
20	first_ineligible_pkt_redirect_en	**In order to save one LRO RXD with large sdl0(64KB), it is better to redirect ineligible pkt into Normal ring when the hit LRO ring is clean and empty without existed aggregated pkts.**
19:8	REV1	**to adjust each lro_auto_learn ring's packet count in auto_learn table located in CDM**
7	L3_CKS_UPD_EN	**ipv4 checksum update enable** 1: enable, 0: disable
6	LRO_CRSN_BNW	**lro_crsn_bnw** 1: black list, 0 : white list
5	LRO_DLY_INT_EN	**delayed interrupt enable for lro ring1,2,3** 1: enable, 0: disable
4	RXD_PREFETCH_EN	**enable bit to activate adma RX descriptor prefetch feature** 0: adma rxd prefetch disable 1: adma rxd prefetch enable
3	MULTIPLE_RXD_PREFETCH_EN	**enable bit to activate adma single/multiple RX descriptor prefetch feature** 0: adma rxd prefetch single

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Bit(s)	Name	Description
		1: adma rxd prefetch multiple
2	MULTIPLE_NON_LRO_RX_RING_EN	**To enable multiple non-lro rx-rings** 0: multiple non-lro rx-ring disable 1: multiple non-lro rx-ring enable
1	LRO_IPv6_EN	**enable bit for IPv6 packet lro** 0: disable lro to IPv6 flow 1: enable lro to IPv6 flow
0	LRO_EN	**enable bit to activate adma RX lro feature** 0: disable lro 1: enable lro

1B100984 **ADMA_LRO_CTRL_DW1** **ADMA Control CRs** **1F1E1F1E**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_CPU_REASON[31:16]															
Type	RW															
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LRO_CPU_REASON[15:0]															
Type	RW															
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:0	LRO_CPU_REASON	

1B100988 **ADMA_LRO_CTRL_DW2** **ADMA Control CRs** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTO_LEARN_LRO_ELIGIBLE_THRESHOLD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTO_LEARN_LRO_ELIGIBLE_THRESHOLD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AUTO_LEARN_LRO_ELIGIBLE_THRESHOLD	**min threshold to become a candicate for lro aggregation**

1B10098C **ADMA_LRO_CTRL_DW3** **ADMA Control CRs** **05F28F40**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_MIN_RXD_SDL0															
Type	RW															
Reset	0	0	0	0	0	1	0	1	1	1	1	1	0	0	1	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_MODE	ADMA_FW_RSTN_REQ	LRO_VLAN_VID_CMP_DEPTH		LRO_VLAN_EN				LRO_MAX_AGGREGATED_CNT							
Type	RW	WO	RW		RW				RW							
Reset	1	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	LRO_MIN_RXD_SDL0	**The least remaining room of SDL0 in RXD for lro aggregation.** It should be greater than the max. size of packet which RX MAC can accept without dropping. That is, LRO_MIN_RXD_SDL0 MUST be equal or greater than MAX_RX_JUMBO/MAC_RX_PKT_LEN fields in CR MAC_P*_MCR(addr : 1B11_0100)
15	ADMA_MODE	**to switch between legacy pdma rx and new adma for lro** 0: legacy pdma rx 1: new adma rx (default)
14	ADMA_FW_RSTN_REQ	
13:12	LRO_VLAN_VID_CMP_DEPTH	**determine how many depth of vlan id need to be compared**
11:8	LRO_VLAN_EN	**support max 4-depth vlan for lro**
7:0	LRO_MAX_AGGREGATED_CNT	**to limit max aggregated packets**

1B100A00 PDMA_INFO PDMA Information 2C000204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV				INDEX_WIDTH				BASE_PTR_WIDTH							
Type	RO				RO				RO							
Reset	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_RING_NUM							
Type	RO								RO							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	REV	**Reserved**
27:24	INDEX_WIDTH	**Point to the next RXD CPU wants to use**
23:16	BASE_PTR_WIDTH	**Base pointer width, x** Base_addr[31:32-x] is shared with all ring base adderss. Only ring #0 base address[31:32-x] field Is writabl. [note]: "0" means no bit of base_address is shared.
15:8	RX_RING_NUM	**Rx ring number**
7:0	TX_RING_NUM	**Tx ring number**

1B100A04 PDMA_GLO_CFG PDMA Global Configuration 40001450

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OF	CSR_CLKG	BYTE_SWA	REV0[15:3]												

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	FSET	ATE_BYP	P													
Type	RW	RW	RW	DC												
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[2:0]			ADMA_RX_BT_SIZE		MULTI_EN	EXT_FIFO_EN	DESC_32B_E	BIG_ENDIAN	TX_WB_DDONE	PDMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type	DC			RW		RW	RW	RW	RW	RW	RW		RO	RW	RO	RW
Reset	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	**2-Byte offset** 0: Rx-buffer will be 4-byte offset 1: Rx-buffer will be 2-byte offset
30	CSR_CLKGATE_BYP	**Clock gated Bypass** 1: PDMA clock is free-running 0: PDMA clock is gating as idle
29	BYTE_SWAP	**Byte Swap** 0: PDMA will not do byte swapping for TX/RX packet descriptor 1: PDMA will do byte swaping for TX/RX packet descriptor
28:13	REV0	**Reserved**
12:11	ADMA_RX_BT_SIZE	**The burst size of ADMA RX** 0: 4 DWORDs (16-bytes) 1: 8 DWORDs (32-bytes) 2: 16 DWORDs (64-bytes) 3: 32 DWORDs (128-bytes)
10	MULTI_EN	**Enable Multi-burst DMA transfer** 0: disabled 1: Multi-burst DMA enabled
9	EXT_FIFO_EN	**Enable multi-burst DMA transfer for the external FIFO.** 0: Only check internal FIFO 1: Check both internal/external FIFO
8	DESC_32B_E	**Enable 32-Byte Descriptor Length** 0: PDMA will fetch the next TX/RX descriptor by addign 16-Byte 1: PDMA will fetch the next TX/RX descriptor by addign 32-Byte
7	BIG_ENDIAN	**Big endian** 0: PDMA will not do byte swapping for TX/RX packet header and payload 1: PDMA will do byte swaping for TX/RX packet header and payload
6	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD 1: Enable TX_DMA writing back DDONE into TXD
5:4	PDMA_BT_SIZE	**The burst size of PDMA** 0: 4 DWORDs (16-bytes) 1: 8 DWORDs (32-bytes) 2: 16 DWORDs (64-bytes) 3: Reserved
3	RX_DMA_BUSY	0: RX_DMA is not busy 1: RX_DMA is busy
2	RX_DMA_EN	0: Diable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop) 1: Enable RX_DMA
1	TX_DMA_BUSY	0: TX_DMA is not busy 1: TX_DMA is busy
0	TX_DMA_EN	0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop)

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Bit(s)	Name	Description
		1: Enable TX_DMA

1B100A08 PDMA_RST_IDX PDMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0														RST_DRX_IDX1	RST_DRX_IDX0
Type	DC														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												RST_DTX_IDX3	RST_DTX_IDX2	RST_DTX_IDX1	RST_DTX_IDX0
Type	DC												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	REV0	**Reserved**
17	RST_DRX_IDX1	**Write 1 to reset RX_DMA RX_IDX1 to 0**
16	RST_DRX_IDX0	**Write 1 to reset RX_DMA RX_IDX0 to 0**
15:4	REV1	**Reserved**
3	RST_DTX_IDX3	**Write 1 to reset TX_DMA TX_IDX3 to 0**
2	RST_DTX_IDX2	**Write 1 to reset TX_DMA TX_IDX2 to 0**
1	RST_DTX_IDX1	**Write 1 to reset TX_DMA TX_IDX1 to 0**
0	RST_DTX_IDX0	**Write 1 to reset TX_DMA TX_IDX0 to 0**

1B100A0C DELAY_INT_CFG Delay Interrupt Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXDLY_INT_EN	TXMAX_PINT							TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TXDLY_INT_EN	**Delay interrupt mechanism** 0: Disable TX delayed interrupt mechanism 1: Enable Tx delayed interrupt mechanism
30:24	TXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final TX_DLY_INT is generated.

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Bit(s)	Name	Description
		[Note] reset to 0 can disable pending interrupt count check.
23:16	TXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than TXMAX_PTIME x 20us or the number of pended TX_DONE is equal or greater than TXMAX_PINT 9see above), an final TX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.
15	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
14:8	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), an finalRX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

1B100A10 FREEQ_THRES Free Queue Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV1[27:12]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1[11:0]												FREEQ_THRES			
Type	DC												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	REV1	**Reserved**
3:0	FREEQ_THRES	**Rx free queue threshold** PDMA will stop DMA interface when left RX descriptors reach this threshold

1B100A20 INT_STATUS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT	RING3_RX_DLY_INT	RING2_RX_DLY_INT	RING1_RX_DLY_INT	RXD_ERROR	ALT_RPLC_INT3	ALT_RPLC_INT2	ALT_RPLC_INT1	REV0	RX_DONE_INT3	RX_DONE_INT2	RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	DC	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												TX_DONE_INT3	TX_DONE_INT2	TX_DONE_INT1	TX_DONE_INT0
Type	DC												W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31	RX_COHERENT	**RX_DMA finds data coherent event while checking ddone bit.**
30	RX_DLY_INT	**Summary of the whole PDMA Rx related interrupts.**
29	TX_COHERENT	**TX_DMA finds data coherent event while checking ddone bit.**
28	TX_DLY_INT	**Summary of the whole PDMA Tx related interrupts.**
27	RING3_RX_DLY_INT	**Rx ring #3 packet receive interrupt**
26	RING2_RX_DLY_INT	**Rx ring #2 packet receive interrupt**
25	RING1_RX_DLY_INT	**Rx ring #1 packet receive interrupt**
24	RXD_ERROR	**Rx descriptor SDL0 error interrupt**
23	ALT_RPLC_INT3	**Auto-learn otg3 replacement interrupt**
22	ALT_RPLC_INT2	**Auto-learn otg2 replacement interrupt**
21	ALT_RPLC_INT1	**Auto-learn otg1 replacement interrupt**
20	REV0	**Reserved**
19	RX_DONE_INT3	**Rx ring #3 packet receive interrupt**
18	RX_DONE_INT2	**Rx ring #2 packet receive interrupt**
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt**
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt**
15:4	REV1	**Reserved**
3	TX_DONE_INT3	**Tx ring #3 packet transmit interrupt**
2	TX_DONE_INT2	**Tx ring #2 packet transmit interrupt**
1	TX_DONE_INT1	**Tx ring #1 packet transmit interrupt**
0	TX_DONE_INT0	**Tx ring #0 packet transmit interrupt**

1B100A28 INT_MASK Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT	REV0										RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	W1C	DC										RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1												TX_DONE_INT3	TX_DONE_INT2	TX_DONE_INT1	TX_DONE_INT0
Type	DC												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_COHERENT	**Interrupt enable for RX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
30	RX_DLY_INT	**Summary of the whole PDMA Rx related interrupts.** 0: Disable interrupt 1: Enable interrupt
29	TX_COHERENT	**Interrupt enable for TX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
28	TX_DLY_INT	**Summary of the whole PDMA Tx related interrupts.**

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Bit(s)	Name	Description
		0: Disable interrupt 1: Enable interrupt
27:18	REV0	**Reserved** 0: Disable interrupt 1: Enable interrupt
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
15:4	REV1	**Reserved** 0: Disable interrupt 1: Enable interrupt
3	TX_DONE_INT3	**Tx ring #3 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt
2	TX_DONE_INT2	**Tx ring #2 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt
1	TX_DONE_INT1	**Tx ring #1 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt
0	TX_DONE_INT0	**Tx ring #0 packet transmit interrupt** 0: Disable interrupt 1: Enable interrupt

1B100A30 **PDMA_TX_DBG0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_TX_DBG0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_TX_DBG0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_TX_DBG0	**TX part debug information**

1B100A34 **PDMA_TX_DBG1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_TX_DBG1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	PDMA_TX_DBG1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_TX_DBG1	**TX part debug information**

1B100A38 ADMA_RX_DBG0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_RX_DBG0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_RX_DBG0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_RX_DBG0	

1B100A3C ADMA_RX_DBG1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_RX_DBG1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_RX_DBG1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_RX_DBG1	

1B100A40 PDMA_INT1_VEC_GRP0 PDMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT1_VEC_GRP0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT1_VEC_GRP0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	PDMA_INT1_VEC_GRP0	**Interrupt group 0 status, this information already "and" with "~PDMA_INT_GRP1 & ~PDMA_INT_GRP2"** Each bit definition is same as "INT_STATUS"

1B100A44 PDMA_INT1_VEC_GRP1 PDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT1_VEC_GRP1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT1_VEC_GRP1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT1_VEC_GRP1	**Interrupt group 1 status, this information already "and" with "PDMA_INT_GRP1"** Each bit definition is same as "INT_STATUS"

1B100A48 PDMA_INT1_VEC_GRP2 PDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT1_VEC_GRP2[23:8]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT1_VEC_GRP2[7:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0								

Bit(s)	Name	Description
31:8	PDMA_INT1_VEC_GRP2	**Interrupt group 2 status, this information already "and" with "PDMA_INT_GRP2"** Each bit definition is same as "INT_STATUS"

1B100A4C LRO_ALT_SCORE_DELTA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_ALT_SCORE_DELTA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LRO_ALT_SCORE_DELTA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	LRO_ALT_SCORE_DELTA	**To add a delta before determine whether replace or not!**

1B100A50 PDMA_INT_GRP1 PDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT_GRP1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_GRP1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT_GRP1	**Interrupt group 1 assignment.** Each bit's definition is same as "INT_STATUS" 0: Leave to ADMA int group 0, if (PDMA_INT_GRP1[n]==0 & PDMA_INT_GRP2[n]==0) 1: Assign to PDMA int group 1

1B100A54 PDMA_INT_GRP2 PDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PDMA_INT_GRP2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_GRP2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PDMA_INT_GRP2	**Interrupt group 2 assignment.** Each bit's definition is same as "INT_STATUS" 0: Leave to ADMA int group 0, if (PDMA_INT_GRP1[n]==0 & PDMA_INT_GRP2[n]==0) 1: Assign to PDMA int group 2

1B100A58 LRO_TIMEOUT_FLAG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[23:8]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[7:0]								AGE_TIMEOUT			REV1	AGG_TIMEOUT			REV2
Type	RO								RC			RO	RC			RO

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	REV0	
7:5	AGE_TIMEOUT	**{ring3, ring2, ring1},** read to clear after pbus address which is decoded to CR chip- select is changed!! That is we should read/write other CRs before read this flag to verify whether it is cleard ot not!
4	REV1	
3:1	AGG_TIMEOUT	**{ring3, ring2, ring1},** read to clear after pbus address which is decoded to CR chip- select is changed!! That is we should read/write other CRs before read this flag to verify whether it is cleard ot not!
0	REV2	

1B100A5C LRO_MAX_AGG_TIME max. aggregation time to flush 000FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0											LRO_ROFFSET_THRESHOLD				
Type	RO											RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:21	REV0	**Reserved**
20:16	LRO_ROFFSET_THRESHOLD	**roffset[4:0] limitation of roffset[5:0]**
15:0	MAX_AGG_TIME	**max. aggregation time to flush**

1B100A60 ADMA_CF8_DBG ADMA debug CFG CF8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_CF8_DBG[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_CF8_DBG[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_CF8_DBG	**Refer to legacy pci cf8/cfc mechanism**

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1B100A64 **ADMA_CFC_RSGL_DBG** **ADMA debug CFG CFC single** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_CFC_RSGL_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_CFC_RSGL_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_CFC_RSGL_DBG	**Refer to legacy pci cf8/cfc mechanism, single read.**

1B100A68 **ADMA_CFC_RSEQ_DBG** **ADMA debug CFG CFC sequential** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_CFC_RSEQ_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_CFC_RSEQ_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_CFC_RSEQ_DBG	**Refer to legacy pci cf8/cfc mechanism, sequential read and 512 bytes wrap-around**

1B100A6C **ADMA_CF8_CFC_ADDR_DBG** **ADMA debug offset addr** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_CFC_RSEQ_OFS_DBG[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_CFC_RSEQ_OFS_DBG[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_CFC_RSEQ_OFS_DBG	**{8'h0, {cfc_rsgl_dw_addr, 1'b0}, {cfc_rseg_dw_addr, 1'b0}, {cf8_raddr_dw_offset, 1'b0}}**

1B100A70 **LRO_RX1_DLY_INT** **Ring1** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	REV	
15	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
14:8	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), an finalRX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

1B100A74 **LRO_RX2_DLY_INT** **Ring2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	REV	
15	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
14:8	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), an finalRX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

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1B100A78 **LRO_RX3_DLY_INT** **Ring3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	REV	
15	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
14:8	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), an finalRX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

1B100A7C **LRO_RING_AGG_CNT_INFO** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV					RING3_AGG_CNT_ZERO	RING2_AGG_CNT_ZERO	RING1_AGG_CNT_ZERO	RING3_AGG_CNT							
Type	RW					RO	RO	RO	RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_AGG_CNT								RING1_AGG_CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	REV	
26	RING3_AGG_CNT_ZERO	1'b1: no any aggregated packet 1'b0: already have aggregated packets
25	RING2_AGG_CNT_ZERO	1'b1: no any aggregated packet 1'b0: already have aggregated packets
24	RING1_AGG_CNT_ZERO	1'b1: no any aggregated packet 1'b0: already have aggregated packets
23:16	RING3_AGG_CNT	**current aggregated packet count number**

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Bit(s)	Name	Description
15:8	RING2_AGG_CNT	**current aggregated packet count number**
7:0	RING1_AGG_CNT	**current aggregated packet count number**

1B100A80 SCH_Q01_CFG Scheduler Configuration for Q0&Q1 1C000C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE1	MAX_RATE_ULMT1	MAX_WEIGHT1		MIN_RATE_RATIO1		MAX_RATE1									
Type	RW	RW	RW		RW		RW									
Reset	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE0	MAX_RATE_ULMT0	MAX_WEIGHT0		MIN_RATE_RATIO0		MAX_RATE0									
Type	RW	RW	RW		RW		RW									
Reset	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE1	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
30	MAX_RATE_ULMT1	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
29:28	MAX_WEIGHT1	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes
27:26	MIN_RATE_RATIO1	**Define the guaranteed Min rate based on MAX_RATE** 2'b00: MIN_RATE3 = MAX_RATE3 2'b01: MIN_RATE3 = 1/2 MAX_RATE3 2'b10: MIN_RATE3 = 1/4 MAX_RATE3 2'b11: MIN_RATE3 = 0
25:16	MAX_RATE1	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps
15	MAX_BKT_SIZE0	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min.

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Bit(s)	Name	Description
		rate per 125us + 2048 bytes.
14	MAX_RATE_ULMT0	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
13:12	MAX_WEIGHT0	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes
11:10	MIN_RATE_RATIO0	**Define the guaranteed Min rate based on MAX_RATE** 2'b00: MIN_RATE3 = MAX_RATE3 2'b01: MIN_RATE3 = 1/2 MAX_RATE3 2'b10: MIN_RATE3 = 1/4 MAX_RATE3 2'b11: MIN_RATE3 = 0
9:0	MAX_RATE0	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps

1B100A84 SCH_Q23_CFG Scheduler Configuration for Q2&Q3 3C001C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BKT_SIZE3	MAX_RATE_ULMT3	MAX_WEIGHT3		MIN_RATE_RATIO3		MAX_RATE3									
Type	RW	RW	RW		RW		RW									
Reset	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BKT_SIZE2	MAX_RATE_ULMT2	MAX_WEIGHT2		MIN_RATE_RATIO2		MAX_RATE2									
Type	RW	RW	RW		RW		RW									
Reset	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_BKT_SIZE3	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
30	MAX_RATE_ULMT3	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
29:28	MAX_WEIGHT3	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue**

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Bit(s)	Name	Description
		2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes
27:26	MIN_RATE_RATIO3	**Define the guaranteed Min rate based on MAX_RATE** 2'b00: MIN_RATE3 = MAX_RATE3 2'b01: MIN_RATE3 = 1/2 MAX_RATE3 2'b10: MIN_RATE3 = 1/4 MAX_RATE3 2'b11: MIN_RATE3 = 0
25:16	MAX_RATE3	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps
15	MAX_BKT_SIZE2	**Maximum bucket size** 0: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us. 1: the maximum bucket size (burst size allowed) for both max. and min. buckets are equal to one maximum size packet + the associated max. or min. rate per 125us + 2048 bytes.
14	MAX_RATE_ULMT2	**Maximum rate limitation** 0: the maximum rate limitation function for queue is enabled. The maximum rate for queue is defined by MAX_RATE. 1: the maximum rate limitation function for queue is disabled or unlimited. The scheduler would allocate bandwidth to queue based on MAX_WEIGHT.
13:12	MAX_WEIGHT2	**Define the auto-reload bucket size if MAX_RATE_ULMT is set to 1. It is also served as excess bandwidth allocation ratio for servicing queue** 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes
11:10	MIN_RATE_RATIO2	**Define the guaranteed Min rate based on MAX_RATE** 2'b00: MIN_RATE3 = MAX_RATE3 2'b01: MIN_RATE3 = 1/2 MAX_RATE3 2'b10: MIN_RATE3 = 1/4 MAX_RATE3 2'b11: MIN_RATE3 = 0
9:0	MAX_RATE2	**Define the limited Max rate for queue if MAX_RATE_ULMT is 0.** The value specified represents the amount of 4-byte quota to be added into the queue #1 bucket per 125us. For example: If 512 is programmed, then the max rate limited is : 512 * 4 bytes/125us = 16.384M bytes/sec or 131Mbps

1B100B00 **LRO_RX_RING0_STP_DTP_DW** **Reserved** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[31:16]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[15:0]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	REV0	

1B100B04 **LRO_RX_RING0_DIP_DW0** **Destination IP addr[31:0]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING0_DIP_DW0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_DIP_DW0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING0_DIP_DW0	**Destination IP addr[31:0]**

1B100B08 **LRO_RX_RING0_DIP_DW1** **Destination IP addr[63:32]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING0_DIP_DW1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_DIP_DW1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING0_DIP_DW1	**Destination IP addr[63:32]**

1B100B0C **LRO_RX_RING0_DIP_DW2** **Destination IP addr[95:64]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING0_DIP_DW2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_DIP_DW2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING0_DIP_DW2	**Destination IP addr[95:64]**

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1B100B10 **LRO_RX_RING0_DIP_DW3** **Destination IP addr[127:96]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING0_DIP_DW3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_DIP_DW3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING0_DIP_DW3	**Destination IP addr[127:96]**

1B100B2C **LRO_RX_RING0_CTRL_DW2** **Reserved** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[21:6]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[5:0]						RING0_MYIP_VLD	RING0_VLD	REV1							
Type	DC						RW	RW	DC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:10	REV0	
9	RING0_MYIP_VLD	**To validate programmed DIP information**
8	RING0_VLD	**To validate programmed flow information**
7:0	REV1	

1B100B40 **LRO_RX_RING1_STP_DTP_DW** **Source TCP port number** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RING1_STP	**Source TCP port number**
15:0	RING1_DTP	**Destination TCP port number**

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1B100B44 **LRO_RX_RING1_DIP_DW0** **Destination IP addr[31:0]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_DIP_DW0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_DIP_DW0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_DIP_DW0	**Destination IP addr[31:0]**

1B100B48 **LRO_RX_RING1_DIP_DW1** **Destination IP addr[63:32]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_DIP_DW1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_DIP_DW1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_DIP_DW1	**Destination IP addr[63:32]**

1B100B4C **LRO_RX_RING1_DIP_DW2** **Destination IP addr[95:64]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_DIP_DW2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_DIP_DW2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_DIP_DW2	**Destination IP addr[95:64]**

1B100B50 **LRO_RX_RING1_DIP_DW3** **Destination IP addr[127:96]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_DIP_DW3[31:16]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING1_DIP_DW3[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_DIP_DW3	**Destination IP addr[127:96]**

1B100B54 LRO_RX_RING1_SIP_DW0 Source IP addr[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING1_SIP_DW0[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING1_SIP_DW0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_SIP_DW0	**Source IP addr[31:0]**

1B100B58 LRO_RX_RING1_SIP_DW1 Source IP addr[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING1_SIP_DW1[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING1_SIP_DW1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_SIP_DW1	**Source IP addr[63:32]**

1B100B5C LRO_RX_RING1_SIP_DW2 Source IP addr[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING1_SIP_DW2[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING1_SIP_DW2[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RING1_SIP_DW2	**Source IP addr[95:64]**

1B100B60 LRO_RX_RING1_SIP_DW3 Source IP addr[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_SIP_DW3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_SIP_DW3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING1_SIP_DW3	**Source IP addr[127:96]**

1B100B64 LRO_RX_RING1_CTRL_DW0 l2_vlan_vid_l2_l 00004006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_VLAN_VID_L2_L						RING1_VLAN_VID_L1[11:2]									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_VLAN_VID_L1[1:0]		RING1_VLAN_VID_L0												RING1_FRCP_IPV4_EN	RING1_FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:26	RING1_VLAN_VID_L2_L	**vlan vid of four forced_port lro rings**
25:14	RING1_VLAN_VID_L1	**To validate IPv4 flow of forced_port lro ring**
13:2	RING1_VLAN_VID_L0	**To validate IPv4 flow of forced_port lro ring**
1	RING1_FRCP_IPV4_EN	**To validate IPv4 flow of forced_port lro ring**
0	RING1_FRCP_IPV6_EN	**To validate IPv6 flow of forced_port lro ring**

1B100B68 LRO_RX_RING1_CTRL_DW1 RX ring age time[9:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_AGE_TIME_L										RING1_VLAN_VLD_L3	RING1_VLAN_VLD_L2	RING1_VLAN_VLD_L1	RING1_VLAN_VLD_L0	RING1_VLAN_VID_L3[11:10]	

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Type	RW										RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING1_VLAN_VID_L3[9:0]										RING1_VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	RING1_AGE_TIME_L	**age time to flush for auto-learn lro ring**
21	RING1_VLAN_VLD_L3	**valid bit of vlan vid for four forced_port lro ring**
20	RING1_VLAN_VLD_L2	**valid bit of vlan vid for four forced_port lro ring**
19	RING1_VLAN_VLD_L1	**valid bit of vlan vid for four forced_port lro ring**
18	RING1_VLAN_VLD_L0	**valid bit of vlan vid for four forced_port lro ring**
17:6	RING1_VLAN_VID_L3	**vlan vid of four forced_port lro rings**
5:0	RING1_VLAN_VID_L2_H	**vlan vid of four forced_port lro rings**

1B100B6C **LRO_RX_RING1_CTRL_DW2** **LRO_MAX_AGGREGATED_CNT_L** **03FFFCBF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_MAX_AGGREGATED_CNT_L						MAX_AGG_TIME[15:6]									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME[5:0]						RING1_MYIP_VLD	RING1_VLD	RING1_OP_MODE		RING1_AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	LRO_MAX_AGGREGATED_CNT_L	**to limit max aggregated packets**
25:10	MAX_AGG_TIME	**max. aggregation time to flush**
9	RING1_MYIP_VLD	**To validate programmed DIP information**
8	RING1_VLD	**To validate programmed flow information**
7:6	RING1_OP_MODE	**00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	RING1_AGE_TIME_H	**age time to flush for auto-learn lro ring, configure all-ones to disable age timeout timer!!**

1B100B70 **LRO_RX_RING1_CTRL_DW3** **Reserved** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[29:14]															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REV[13:0]**														**LRO_MAX_AGGREGATED_CNT_H**	
Type	RW														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**to limit max aggregated packets**
1:0	LRO_MAX_AGGREGATED_CNT_H	**to limit max aggregated packets**

1B100B80 LRO_RX_RING2_STP_DTP_DW Source TCP port number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING2_STP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING2_DTP**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RING2_STP	**Source TCP port number**
15:0	RING2_DTP	**Destination TCP port number**

1B100B84 LRO_RX_RING2_DIP_DW0 Destination IP addr[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING2_DIP_DW0[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING2_DIP_DW0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_DIP_DW0	**Destination IP addr[31:0]**

1B100B88 LRO_RX_RING2_DIP_DW1 Destination IP addr[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING2_DIP_DW1[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_DIP_DW1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_DIP_DW1	**Destination IP addr[63:32]**

1B100B8C **LRO_RX_RING2_DIP_DW2** **Destination IP addr[95:64]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_DIP_DW2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_DIP_DW2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_DIP_DW2	**Destination IP addr[95:64]**

1B100B90 **LRO_RX_RING2_DIP_DW3** **Destination IP addr[127:96]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_DIP_DW3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_DIP_DW3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_DIP_DW3	**Destination IP addr[127:96]**

1B100B94 **LRO_RX_RING2_SIP_DW0** **Source IP addr[31:0]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_SIP_DW0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_SIP_DW0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	RING2_SIP_DW0	**Source IP addr[31:0]**

1B100B98 **LRO_RX_RING2_SIP_DW1** **Source IP addr[63:32]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_SIP_DW1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_SIP_DW1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_SIP_DW1	**Source IP addr[63:32]**

1B100B9C **LRO_RX_RING2_SIP_DW2** **Source IP addr[95:64]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_SIP_DW2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_SIP_DW2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_SIP_DW2	**Source IP addr[95:64]**

1B100BA0 **LRO_RX_RING2_SIP_DW3** **Source IP addr[127:96]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_SIP_DW3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_SIP_DW3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING2_SIP_DW3	**Source IP addr[127:96]**

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1B100BA4 **LRO_RX_RING2_CTRL_DW0** **l2_vlan_vid_l2_l** **00004006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_VLAN_VID_L2_L						RING2_VLAN_VID_L1[11:2]									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_VLAN_VID_L1[1:0]		RING2_VLAN_VID_L0												RING2_FRCP_IPV4_EN	RING2_FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:26	RING2_VLAN_VID_L2_L	**vlan vid of four forced_port lro rings**
25:14	RING2_VLAN_VID_L1	**To validate IPv4 flow of forced_port lro ring**
13:2	RING2_VLAN_VID_L0	**To validate IPv4 flow of forced_port lro ring**
1	RING2_FRCP_IPV4_EN	**To validate IPv4 flow of forced_port lro ring**
0	RING2_FRCP_IPV6_EN	**To validate IPv6 flow of forced_port lro ring**

1B100BA8 **LRO_RX_RING2_CTRL_DW1** **RX ring age time[9:0]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING2_AGE_TIME_L										RING2_VLAN_VLD_L3	RING2_VLAN_VLD_L2	RING2_VLAN_VLD_L1	RING2_VLAN_VLD_L0	RING2_VLAN_VID_L3[11:10]	
Type	RW										RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_VLAN_VID_L3[9:0]										RING2_VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	RING2_AGE_TIME_L	**age time to flush for auto-learn lro ring**
21	RING2_VLAN_VLD_L3	**valid bit of vlan vid for four forced_port lro ring**
20	RING2_VLAN_VLD_L2	**valid bit of vlan vid for four forced_port lro ring**
19	RING2_VLAN_VLD_L1	**valid bit of vlan vid for four forced_port lro ring**
18	RING2_VLAN_VLD_L0	**valid bit of vlan vid for four forced_port lro ring**
17:6	RING2_VLAN_VID_L3	**vlan vid of four forced_port lro rings**
5:0	RING2_VLAN_VID_L2_H	**vlan vid of four forced_port lro rings**

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1B100BAC **LRO_RX_RING2_CTRL_DW2** **LRO_MAX_AGGREGATED_CNT_L** **03FFFCBF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_MAX_AGGREGATED_CNT_L						MAX_AGG_TIME[15:6]									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME[5:0]						RING2_MYIP_VLD	RING2_VLD	RING2_OP_MODE		RING2_AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	LRO_MAX_AGGREGATED_CNT_L	**to limit max aggregated packets**
25:10	MAX_AGG_TIME	**max. aggregation time to flush**
9	RING2_MYIP_VLD	**To validate programmed DIP information**
8	RING2_VLD	**To validate programmed flow information**
7:6	RING2_OP_MODE	**00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	RING2_AGE_TIME_H	**age time to flush for auto-learn lro ring, configure all-ones to disable age timeout timer!!**

1B100BB0 **LRO_RX_RING2_CTRL_DW3** **Reserved** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[29:14]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[13:0]														LRO_MAX_AGGREGATED_CNT_H	
Type	RW														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**to limit max aggregated packets**
1:0	LRO_MAX_AGGREGATED_CNT_H	**to limit max aggregated packets**

1B100BC0 **LRO_RX_RING3_STP_DTP_DW** **Source TCP port number** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_DTP															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RING3_STP	**Source TCP port number**
15:0	RING3_DTP	**Destination TCP port number**

1B100BC4 LRO_RX_RING3_DIP_DW0 Destination IP addr[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING3_DIP_DW0[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING3_DIP_DW0[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_DIP_DW0	**Destination IP addr[31:0]**

1B100BC8 LRO_RX_RING3_DIP_DW1 Destination IP addr[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING3_DIP_DW1[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING3_DIP_DW1[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_DIP_DW1	**Destination IP addr[63:32]**

1B100BCC LRO_RX_RING3_DIP_DW2 Destination IP addr[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RING3_DIP_DW2[31:16]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RING3_DIP_DW2[15:0]**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	RING3_DIP_DW2	**Destination IP addr[95:64]**

1B100BD0 LRO_RX_RING3_DIP_DW3 Destination IP addr[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_DIP_DW3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_DIP_DW3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_DIP_DW3	**Destination IP addr[127:96]**

1B100BD4 LRO_RX_RING3_SIP_DW0 Source IP addr[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_SIP_DW0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_SIP_DW0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_SIP_DW0	**Source IP addr[31:0]**

1B100BD8 LRO_RX_RING3_SIP_DW1 Source IP addr[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_SIP_DW1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_SIP_DW1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_SIP_DW1	**Source IP addr[63:32]**

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1B100BDC **LRO_RX_RING3_SIP_DW2** **Source IP addr[95:64]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_SIP_DW2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_SIP_DW2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_SIP_DW2	**Source IP addr[95:64]**

1B100BE0 **LRO_RX_RING3_SIP_DW3** **Source IP addr[127:96]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_SIP_DW3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_SIP_DW3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RING3_SIP_DW3	**Source IP addr[127:96]**

1B100BE4 **LRO_RX_RING3_CTRL_DW0** **l2_vlan_vid_l2_l** **00004006**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_VLAN_VID_L2_L						RING3_VLAN_VID_L1[11:2]									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_VLAN_VID_L1[1:0]		RING3_VLAN_VID_L0												RING3_FRCP_IPV4_EN	RING3_FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:26	RING3_VLAN_VID_L2_L	**vlan vid of four forced_port lro rings**
25:14	RING3_VLAN_VID_L1	**To validate IPv4 flow of forced_port lro ring**
13:2	RING3_VLAN_VID_L0	**To validate IPv4 flow of forced_port lro ring**
1	RING3_FRCP_IPV4_EN	**To validate IPv4 flow of forced_port lro ring**

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Bit(s)	Name	Description
0	RING3_FRCP_IPV6_EN	**To validate IPv6 flow of forced_port lro ring**

1B100BE8 **LRO_RX_RING3_CTRL_DW1** **RX ring age time[9:0]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_AGE_TIME_L										RING3_VLAN_VLD_L3	RING3_VLAN_VLD_L2	RING3_VLAN_VLD_L1	RING3_VLAN_VLD_L0	RING3_VLAN_VID_L3[11:10]	
Type	RW										RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING3_VLAN_VID_L3[9:0]										RING3_VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	RING3_AGE_TIME_L	**age time to flush for auto-learn lro ring**
21	RING3_VLAN_VLD_L3	**valid bit of vlan vid for four forced_port lro ring**
20	RING3_VLAN_VLD_L2	**valid bit of vlan vid for four forced_port lro ring**
19	RING3_VLAN_VLD_L1	**valid bit of vlan vid for four forced_port lro ring**
18	RING3_VLAN_VLD_L0	**valid bit of vlan vid for four forced_port lro ring**
17:6	RING3_VLAN_VID_L3	**vlan vid of four forced_port lro rings**
5:0	RING3_VLAN_VID_L2_H	**vlan vid of four forced_port lro rings**

1B100BEC **LRO_RX_RING3_CTRL_DW2** **LRO_MAX_AGGREGATED_CNT_L** **03FFFCBF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_MAX_AGGREGATED_CNT_L						MAX_AGG_TIME[15:6]									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME[5:0]						RING3_MYIP_VLD	RING3_VLD	RING3_OP_MODE		RING3_AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	LRO_MAX_AGGREGATED_CNT_L	**to limit max aggregated packets**
25:10	MAX_AGG_TIME	**max. aggregation time to flush**
9	RING3_MYIP_VLD	**To validate programmed DIP information**

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Bit(s)	Name	Description
8	RING3_VLD	**To validate programmed flow information**
7:6	RING3_OP_MODE	**00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	RING3_AGE_TIME_H	**age time to flush for auto-learn lro ring, configure all-ones to disable age timeout timer!!**

1B100BF0 **LRO_RX_RING3_CTRL_DW3** **Reserved** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[29:14]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[13:0]														LRO_MAX_AGGREGATED_CNT_H	
Type	RW														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**to limit max aggregated packets**
1:0	LRO_MAX_AGGREGATED_CNT_H	**to limit max aggregated packets**

1B101400 **CDMQ_IG_CTRL** **CDM VLAN Control** **81000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0														UNTAG_EN	STAG_EN
Type	DC														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
15:2	REV0	**Reserved**
1	UNTAG_EN	**VLAN untagging** Untagg the egress packets which are transmitted from CDM 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged
0	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from CPU . 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.

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1B101404 CDMQ_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[30:15]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[14:0]															UNTAG_EN
Type	DC															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:1	REV0	**Reserved**
0	UNTAG_EN	**VLAN untag** Untag the egress packets which are transmitted from CDM to CPU 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged

1B101408 CDMQ_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															PPP_INS
Type	DC															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	REV0	**Reserved**
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

1B101500 GDM2_IG_CTRL GDM Ingress Control 00717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0						INSV_EN	STAG_EN	REV1	GDM_ICS_EN	GDM_TCS_EN	GDM_UCS_EN	DROP_256B	REV2		STRP_CRC
Type	DC						RW	RW	DC	RW	RW	RW	RW	DC		RW
Reset	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:26	REV0	**Reserved**

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Bit(s)	Name	Description
25	INSV_EN	**VLAN insertion** Insert Port VID on the received packets on the corresponding GDM port. 0: disable 1: Insert 4-byte VLAN tag after Source Address
24	STAG_EN	**Special tag indication** Indicate that the received packets is carrying the special tag from GDM port. 0: no special tag inserted. 1: The first 2-byte after Source Address is the special tag.
23	REV1	**Reserved**
22	GDM_ICS_EN	**IPv4 header checksum error drop** 0: checksum error status reported on RX descriptor (IP4F) 1: checksum error packet will be dropped
21	GDM_TCS_EN	**TCP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
20	GDM_UCS_EN	**UDP checksum error drop** 0: checksum error status reported on RX descriptor (L4F) 1: checksum error packet will be dropped
19	DROP_256B	**A special mode to drop packets with payload > 256-bytes** 1'b0: Drop packets according to the standard Ethernet frame length limitation. 1'b1: Dopr packets with payloa > 256 bytes
18:17	REV2	**Reserved**
16	STRP_CRC	**GDM RX CRC Stripping** 1'b: Disable GDM RX CRC stripping 1'b1: Enable GDM RX CRC stripping
15:12	MYMAC_DP	**MY_MAC frames destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
11:8	BC_DP	**Broadcast frame destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved
7:4	MC_DP	**Multicast frame destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved

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Bit(s)	Name	Description
3:0	UN_DP	**Other frame destination port** 4'b0000: PDMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: Reserved 4'b0100: PPE 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1xxx: Reserved

1B101504 **GDM2_EG_CTRL** **GDM Egress Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	UNTAG_EN	DIS_PAD	DIS_CRC	REV1			SHPR_EN	BK_SIZE							
Type	DC	RW	RW	RW	DC			RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK	REV2	TK_RATE													
Type	RW	DC	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	
30	UNTAG_EN	**VLAN untagging** Untagg the egress packets which are transmitted from GDM. 0: disable 1: The first 4-bytes VLAN tag after Source Address will be untagged
29	DIS_PAD	**GMAC Tx padding fucntion** 1'b0: Enable GMAC Tx padding 1'b1: Disable GMAC Tx padding
28	DIS_CRC	**GMAC TX CRC generation** 1'b0: Enable GMAC Tx CRC generation 1'b1: Disable GMAC Tx CRC generation
27:25	REV1	**Reserved**
24	SHPR_EN	**GDM output shaper enable** 1'b0: Disable 1'b1: Enable
23:16	BK_SIZE	**GDM output shaper bucket size.** This unit is 1K-byte
15	TK_TICK	**GDM shaper token period** 1'b0: GDM shaper add token every 1ms 1'b1: GDM shaper add token every 20us
14	REV2	**Reserved**
13:0	TK_RATE	**GDM output shaper token rate** The unit is 8-Byte/ms or 8-Byte/20us according to TK_TICK.

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1B101508 GDM2_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	**MY_MAC Address [31:0]**

1B10150C GDM2_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RESV0	**Reserved**
15:0	MAC_ADR	**MY_MAC Address [47:32]**

1B101510 GDM2_VLAN_GEN GDM VLAN Generation 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	**Inserted VLAN TPID**
15:13	GDM_PRI	**Inserted PRI**
12	GDM_CFI	**Inserted CFI**
11:0	GDM_VID	**Inserted VLAN ID**

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1B101514 GDM2_FILTER_CRTL GDM Filter Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[27:12]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[11:0]												GDM_VIDF_EN	GMD_HASH_ALG	GDM_DAF_MODE	
Type	DC												RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	REV0	
3	GDM_VIDF_EN	**GDM VLAN ID filter enable**
2	GMD_HASH_ALG	**Hash Algorithm setting** 0: Direct map - Using DA40 and DA 7~0 as hash key. Receive packet if corresponding bit is set. 1: CRC32 - Using 32 bit CRC bit 8~0 of DA as hash key. Receive packet if corresponding bit is set.
1:0	GDM_DAF_MODE	**Receive packet with DA Filter function** 0: Promisculous mode - Receive all packets. 1: Filter packet by MAC_MAC/Broadcast/Hash table 2: Filter packet by MAC_MAC/Broadcast 3: Reserved

1B101518 GDM2_VIDF01 GDM VID Filter Control 01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID1_VLD	REV1			GDM2_VID1											
Type	RW	DC			RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID0_VLD	REV0			GDM2_VID0											
Type	RW	DC			RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID1_VLD	**VLAN ID #1 valid bit**
30:28	REV1	
27:16	GDM2_VID1	**VLAN ID #1**
15	GDM2_VID0_VLD	**VLAN ID #0 valid bit**
14:12	REV0	
11:0	GDM2_VID0	**VLAN ID #0**

1B10151C GDM2_VIDF23 GDM VID Filter Control 23 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID3_VLD	REV1			GDM2_VID3											
Type	RW	DC			RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID2_VLD	REV0			GDM2_VID2											
Type	RW	DC			RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID3_VLD	**VLAN ID #3 valid bit**
30:28	REV1	
27:16	GDM2_VID3	**VLAN ID #3**
15	GDM2_VID2_VLD	**VLAN ID #2 valid bit**
14:12	REV0	
11:0	GDM2_VID2	**VLAN ID #2**

1B101800 QTX_CFG_0 TX Queue #0 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

1B101804 QTX_SCH_0 TX Queue #0 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Leaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz. 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable.** [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz. 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101808 QTX_HEAD_0 TX Queue #0 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_DES_HEAD[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10180C QTX_TAIL_0 TX Queue #0 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX_DES_TAIL[31:16]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX_DES_TAIL[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101810 QTX_CFG_1 TX Queue #1 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX_DES_CNT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**HW_RESV_CNT**								**SW_RESV_CNT**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

1B101814 QTX_SCH_1 TX Queue #1 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX_SCH_SEL**	**LEAKY_BK**	**BUCKET_DEP**		**MIN_RATE_EN**	**MIN_RATE_MAN**							**MIN_RATE_EXP**			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz. 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable.** [Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz. 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

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1B101818 QTX_HEAD_1 TX Queue #1 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10181C QTX_TAIL_1 TX Queue #1 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101820 QTX_CFG_2 TX Queue #2 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

1B101824 QTX_SCH_2 TX Queue #2 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_S	LEAKY_BK	BUCKET_DEP		MIN_RATE_E	MIN_RATE_MAN							MIN_RATE_EXP			

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	EL				N											
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**MAX_RATE_WGHT**				**MAX_RATE_EN**	**MAX_RATE_MAN**							**MAX_RATE_EXP**			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

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1B101828 QTX_HEAD_2 TX Queue #2 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10182C QTX_TAIL_2 TX Queue #2 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101830 QTX_CFG_3 TX Queue #3 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

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1B101834 QTX_SCH_3 TX Queue #3 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps)

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Bit(s)	Name	Description
		5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101838 QTX_HEAD_3 TX Queue #3 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10183C QTX_TAIL_3 TX Queue #3 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101840 QTX_CFG_4 TX Queue #4 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

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Bit(s)	Name	Description
		0: No reserved buffer 1: Buffer Reserved

1B101844 **QTX_SCH_4** **TX Queue #4 Schedule** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127

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Bit(s)	Name	Description
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101848 QTX_HEAD_4 TX Queue #4 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10184C QTX_TAIL_4 TX Queue #4 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101850 QTX_CFG_5 TX Queue #5 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101854 QTX_SCH_5 TX Queue #5 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n

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Bit(s)	Name	Description
		15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101858 QTX_HEAD_5 TX Queue #5 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10185C QTX_TAIL_5 TX Queue #5 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101860 QTX_CFG_6 TX Queue #6 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101864 QTX_SCH_6 TX Queue #6 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps)

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Bit(s)	Name	Description
		Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101868 QTX_HEAD_6 TX Queue #6 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10186C QTX_TAIL_6 TX Queue #6 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

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1B101870 QTX_CFG_7 TX Queue #7 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101874 QTX_SCH_7 TX Queue #7 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection

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Bit(s)	Name	Description
		0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101878 QTX_HEAD_7 TX Queue #7 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10187C QTX_TAIL_7 TX Queue #7 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101880 QTX_CFG_8 TX Queue #8 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101884 QTX_SCH_8 TX Queue #8 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper

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Bit(s)	Name	Description
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101888 QTX_HEAD_8 TX Queue #8 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B10188C QTX_TAIL_8 TX Queue #8 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101890 QTX_CFG_9 TX Queue #9 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B101894 QTX_SCH_9 TX Queue #9 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB

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Bit(s)	Name	Description
		2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101898 QTX_HEAD_9 TX Queue #9 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

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1B10189C QTX_TAIL_9 TX Queue #9 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018A0 QTX_CFG_10 TX Queue #10 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018A4 QTX_SCH_10 TX Queue #10 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler

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Bit(s)	Name	Description
		1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B1018A8 QTX_HEAD_10 TX Queue #10 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018AC QTX_TAIL_10 TX Queue #10 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018B0 QTX_CFG_11 TX Queue #11 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018B4 QTX_SCH_11 TX Queue #11 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B1018B8 QTX_HEAD_11 TX Queue #11 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018BC QTX_TAIL_11 TX Queue #11 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018C0 QTX_CFG_12 TX Queue #12 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018C4 QTX_SCH_12 TX Queue #12 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B1018C8 QTX_HEAD_12 TX Queue #12 Head Pointer 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018CC QTX_TAIL_12 TX Queue #12 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018D0 QTX_CFG_13 TX Queue #13 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

1B1018D4 QTX_SCH_13 TX Queue #13 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

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1B1018D8 QTX_HEAD_13 TX Queue #13 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018DC QTX_TAIL_13 TX Queue #13 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018E0 QTX_CFG_14 TX Queue #14 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

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1B1018E4 QTX_SCH_14 TX Queue #14 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps)

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Bit(s)	Name	Description
		5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B1018E8 QTX_HEAD_14 TX Queue #14 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018EC QTX_TAIL_14 TX Queue #14 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B1018F0 QTX_CFG_15 TX Queue #15 Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

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Bit(s)	Name	Description
		0: No reserved buffer 1: Buffer Reserved

1B1018F4 QTX_SCH_15 TX Queue #15 Schedule 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL	LEAKY_BK	BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler
30	LEAKY_BK	**Eleaky Bucket Select**
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	MIN_RATE_EN	**TX Queue min. rate control enable** 0: disable. When disable, shaper will always let the pakcet pass(infinite rate) 1: enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the min. rate control of the TX queue #** value rang: 0 .. 127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**TX Queue max. rate control enable**
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** value rang: 0 .. 127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** value selection

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Bit(s)	Name	Description
		0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B1018F8 QTX_HEAD_15 TX Queue #15 Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1B1018FC QTX_TAIL_15 TX Queue #15 Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

1B101900 QRX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring # (4-DW aligned address)**

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1B101904 QRX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #**

1B101908 QRX_CRX_IDX_0 RX Ring #0 CPU pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_CRX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10190C QRX_DRX_IDX_0 RX Ring #0 DMA poitner 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_DRX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

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1B101910 **QRX_BASE_PTR_1** **RX Ring #1 Base Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring # (4-DW aligned address)**

1B101914 **QRX_MAX_CNT_1** **RX Ring #1 Maximum Count** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_MAX_CNT											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #**

1B101918 **QRX_CRX_IDX_1** **RX Ring #1 CPU pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_CRX_IDX											
Type	DC				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1B10191C **QRX_DRX_IDX_1** **RX Ring #1 DMA poitner** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	REV[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV[3:0]				RX_DRX_IDX											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:12	REV	**Reserved**
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

1B101980 VQTX_TB_BASE_0 TX Virtual Queue Table #0 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_0	**Base address of TX Virtual Queue Table #0** This virtual queue table belongs to physical TX queue #0

1B101984 VQTX_TB_BASE_1 TX Virtual Queue Table #1 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_1	**Base address of TX Virtual Queue Table #1** This virtual queue table belongs to physical TX queue #1

1B101988 VQTX_TB_BASE_2 TX Virtual Queue Table #2 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_2	**Base address of TX Virtual Queue Table #2** This virtual queue table belongs to physical TX queue #2

1B10198C VQTX_TB_BASE_3 TX Virtual Queue Table #3 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_3	**Base address of TX Virtual Queue Table #3** This virtual queue table belongs to physical TX queue #3

1B101A00 QDMA_INFO QDMA Information 000C0210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV				INDEX_WIDTH											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_QUE_NUM							
Type	RO								RO							
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV	**QDMA revision**
27:16	INDEX_WIDTH	**Ring index width**
15:8	RX_RING_NUM	**Rx ring number**
7:0	TX_QUE_NUM	**Tx queue number**

1B101A04 QDMA_GLO_CFG QDMA Global Configuration 40000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLKGATE	BYTE_SWAP										RBUS_CO_PRO			
Type	RW	RW	RW										RW			
Reset	0	1	0										0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						NDP_CO_PRO	BKTCLK_CTRL	DESC_32B_E	BIG_ENDIAN	TX_WB_DDONE	QDMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type						RW	RW	RW	RW	RW	RW		RO	RW	RO	RW
Reset						0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	**2-Byte offset** 0: Rx-buffer will be 4-byte offset 1: Rx-buffer will be 2-byte offset
30	CSR_CLKGATE	**Clock gated** 0: QDMA clock is free-running 1: QDMA clock is gating as idle
29	BYTE_SWAP	**Byte Swap** 0: QDMA will not do byte swapping for TX/RX packet descriptor 1: QDMA will do byte swaping for TX/RX packet descriptor
19:16	RBUS_CO_PRO	**Rbus Coherence Protection** 4'b0000: Disable Rbus Coherence Protection, read request of QDMA rbus interface will be assertted back to back. 4'b1000: Read request will be postponed till all past write complete. 4'b1001: Read request will be postponed till all past write complete + extra 1*16 system clock cycles. 4'b1010: Read request will be postponed till all past write complete + extra 2*16 system clock cycles. 4'b1111: Read request will be postponed till all past write complete + extra 7*16 system clock cycles.
10	NDP_CO_PRO	**Next Descriptor Pointer Coherence Protection** 0: Disable the NDP coherence protection 1: Enable the NDP coherence protection. Before de-queue a packet, QDMA TX will check that descriptor's NDP[0] already be set as 1 by Forwarding agent.
9	BKTCLK_CTRL	**Scheduler bucket clock control** 0: Scheduler bucket clock is 125Mhz 1: Scheduler bucket clock is 62.5Mhz
8	DESC_32B_E	**Enable 32-Byte RX Descriptor Length** 0: PDMA will fetch the next RX descriptor by addign 16-Byte 1: PDMA will fetch the next RX descriptor by addign 32-Byte
7	BIG_ENDIAN	**Big endian** 0: QDMA will not do byte swapping for TX/RX packet header and payload 1: QDMA will do byte swaping for TX/RX packet header and payload
6	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD 1: Enable TX_DMA writing back DDONE into TXD
5:4	QDMA_BT_SIZE	**The burst size of QDMA** 0: 4 DWORDs (16-bytes) 1: 8 DWORDs (32-bytes) 2: 16 DWORDs (64-bytes) 3: Reserved
3	RX_DMA_BUSY	0: RX_DMA is not busy 1: RX_DMA is busy
2	RX_DMA_EN	0: Diable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop) 1: Enable RX_DMA
1	TX_DMA_BUSY	0: TX_DMA is not busy 1: TX_DNA is busy

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Bit(s)	Name	Description
0	TX_DMA_EN	0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop) 1: Enable TX_DMA

1B101A08 QDMA_RST_IDX QDMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0														RST_DRX_IDX1	RST_DRX_IDX0
Type	DC														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST_TX_IDX15	RST_TX_IDX14	RST_TX_IDX13	RST_TX_IDX12	RST_TX_IDX11	RST_TX_IDX10	RST_TX_IDX9	RST_TX_IDX8	RST_TX_IDX7	RST_TX_IDX6	RST_TX_IDX5	RST_TX_IDX4	RST_TX_IDX3	RST_TX_IDX2	RST_TX_IDX1	RST_TX_IDX0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	REV0	**Reserved**
17	RST_DRX_IDX1	**Write 1 to reset RX_DMA RX_IDX1 to 0**
16	RST_DRX_IDX0	**Write 1 to reset RX_DMA RX_IDX0 to 0**
15	RST_TX_IDX15	**Write 1 to reset TX_DMA TX_IDX15 to 0**
14	RST_TX_IDX14	**Write 1 to reset TX_DMA TX_IDX14 to 0**
13	RST_TX_IDX13	**Write 1 to reset TX_DMA TX_IDX13 to 0**
12	RST_TX_IDX12	**Write 1 to reset TX_DMA TX_IDX12 to 0**
11	RST_TX_IDX11	**Write 1 to reset TX_DMA TX_IDX11 to 0**
10	RST_TX_IDX10	**Write 1 to reset TX_DMA TX_IDX10 to 0**
9	RST_TX_IDX9	**Write 1 to reset TX_DMA TX_IDX9 to 0**
8	RST_TX_IDX8	**Write 1 to reset TX_DMA TX_IDX8 to 0**
7	RST_TX_IDX7	**Write 1 to reset TX_DMA TX_IDX7 to 0**
6	RST_TX_IDX6	**Write 1 to reset TX_DMA TX_IDX6 to 0**
5	RST_TX_IDX5	**Write 1 to reset TX_DMA TX_IDX5 to 0**
4	RST_TX_IDX4	**Write 1 to reset TX_DMA TX_IDX4 to 0**
3	RST_TX_IDX3	**Write 1 to reset TX_DMA TX_IDX3 to 0**
2	RST_TX_IDX2	**Write 1 to reset TX_DMA TX_IDX2 to 0**
1	RST_TX_IDX1	**Write 1 to reset TX_DMA TX_IDX1 to 0**
0	RST_TX_IDX0	**Write 1 to reset TX_DMA TX_IDX0 to 0**

1B101A0C QDMA_DELAY_INT Delay Interrupt Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DINT_EN	RLS_MAX_PINT							RLS_MAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism 1: Enable Rx delayed interrupt mechanism
30:24	RXMAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final RX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
23:16	RXMAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RXMAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RXMAX_PINT 9see above), an finalRX_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.
15	RLS_DINT_EN	0: Disable RLS delayed interrupt mechanism 1: Enable RLS delayed interrupt mechanism
14:8	RLS_MAX_PINT	**Specified Max. number of pended interrupts** When the number of pended interrupts is equal or greater than the value specified here or interupt pending time reach the limit (see below), an final RLS_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt count check.
7:0	RLS_MAX_PTIME	**Specified Max. pended time** When the pending time is equal or greater than RLS_MAX_PTIME x 20us or the number of pended RX_DONE is equal or greater than RLS_MAX_PINT (see above), an final RLS_DLY_INT is generated. [Note] reset to 0 can disable pending interrupt time check.

1B101A10 QDMA_FC_THRES Flow ControlThreshold 90904444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_FSTVQ_MODE		SW_DROP_MODE		SW_DROP_FSTVQ		SW_DROP_FFA	SW_DROP_EN	HW_DROP_FSTVQ_MODE		HW_DROP_MODE		HW_DROP_FSTVQ		HW_DROP_FFA	HW_DROP_EN
Type	RW		RW		RW		RW	RW	RW		RW		RW		RW	RW
Reset	1	0	0	1	0		0	0	1	0	0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SHARE_SW_TH				SHARE_HW_TH				FREE_TH				RING_TH			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit(s)	Name	Description
31:30	SW_DROP_FSTVQ_MODE	**SW drop condition on fullest virtual queue** If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the enqueuing packet to fullest VQ will be drop depends on the usage of SW free-for-all buffer. 2'b00: FFA usage >= 0% 2'b01: FFA usage >= 25%

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Bit(s)	Name	Description
		2'b10: FFA usage >= 50% 2'b11: FFA usage >= 75%
29:28	SW_DROP_MODE	**Drop Distribution Mode for SW Drop** 2'b00: 50/25/0/0 2'b01: 75/50/25/0 2'b10: 100/75/50/25 2'b11: 100/100/75/50
27	SW_DROP_FSTVQ	**SW drop enqueuing packet on fullest virtual queue**
25	SW_DROP_FFA	**Flow Control Drop** QDMA asserts FC when FFA is equal to 0 and egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit. 0: QDMA deassert FC when the egress queue count is less than the reserved queu count. 1: QDMA deassert FC when FFA is bigger than 0 or the egress queue count is less than the reserved queue count.
24	SW_DROP_EN	**Enable Flow Control for SW buffer pool** QDMA drop packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.
23:22	HW_DROP_FSTVQ_MODE	**HW drop condition on fullest virtual queue** If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the enqueuing packet to fullest VQ will be drop depends on the usage of HW free-for-all buffer. 2'b00: FFA usage >= 0% 2'b01: FFA usage >= 25% 2'b10: FFA usage >= 50% 2'b11: FFA usage >= 75%
21:20	HW_DROP_MODE	**Drop Distribution Mode for HW Drop** 2'b00: 50/25/0/0 2'b01: 75/50/25/0 2'b10: 100/75/50/25 2'b11: 100/100/75/50
19	HW_DROP_FSTVQ	**HW drop enqueuing packet on fullest virtual queue**
17	HW_DROP_FFA	**Flow Control Drop** QDMA asserts FC when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit. 0: QDMA deassert FC when the egress queue count is less than the reserved queu count. 1: QDMA deassert FC when FFA is bigger than 0 or the egress queue count is less than the reserved queue count.
16	HW_DROP_EN	**Enable Flow Control for HW buffer pool** QDMA drop packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.
15:12	SHARE_SW_TH	**SW Shared buffer threshold** QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
11:8	SHARE_HW_TH	**HW Shared buffer threshold** QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
7:4	FREE_TH	**Rx free buffer threshold** QDMA will pause RXDMA interface when the left free buffer descriptors reach this threshold
3:0	RING_TH	**Rx Ring threshold**

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Bit(s)	Name	Description
		QDMA will pause RXDMA interface when the left RX ring descriptors reach this threshold

1B101A14 QDMA_TX_SCH TX Scheduler Rate Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	SCH2_LEAKY_BK	SCH2_BUCKET_DEP		SCH2_RATE_EN	SCH2_RATE_MAN							SCH2_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	SCH1_LEAKY_BK	SCH1_BUCKET_DEP		SCH1_RATE_EN	SCH1_RATE_MAN							SCH1_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	SCH2_LEAKY_BK	**Leaky Bucket Select**
29:28	SCH2_BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
27	SCH2_RATE_EN	**TX SCH2 max. rate control enable**
26:20	SCH2_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH2** value rang: 0 .. 127
19:16	SCH2_RATE_EXP	**Exponent part of the max. rate control of the TX SCH2** value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15	REV1	**Reserved**
14	SCH1_LEAKY_BK	**Leaky Bucket Select**
13:12	SCH1_BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3: 16KB
11	SCH1_RATE_EN	**TX SCH1 max. rate control enable**
10:4	SCH1_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH1** value rang: 0 .. 127
3:0	SCH1_RATE_EXP	**Exponent part of the max. rate control of the TX SCH2** value selection 0: QDMA_RATE_EXP0 (default: 1kbps)

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Bit(s)	Name	Description
		1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

1B101A18 QDMA_INT_STS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT	REV3										RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C	DC										W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0	REV2			FWD_FIFO_OV	REV1			QTX_REQ_EMP_VQ	REV0			RLS_DONE_INT
Type	W1C	W1C	W1C	W1C	DC			W1C	DC			W1C	DC			W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_COHERENT	**RX_DMA finds data coherent event while checking ddone bit.**
30	RX_DLY_INT	**Summary of the whole QDMA Rx related interrupts.**
29	RLS_COHERENT	**TX_DMA finds data coherent event while checking ddone bit.**
28	RLS_DLY_INT	**Summary of the whole QDMA Tx related interrupts.**
27:18	REV3	**Reserved**
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt**
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt**
15	VQDEP_DEQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ not empty yet after de-queuing, but the remainder vq_depth>=1
14	VQDEP_DEQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ becomes empty after de-queuing but the remainder vq_depth=0
13	VQDEP_ENQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ be en-queued the first packet descirptor, but the vq_depth already >=1.
12	VQDEP_ENQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ be en-queued a packet descirptor, but the vq_depth already full = 16'hffff.
11:9	REV2	**Reserved**
8	FWD_FIFO_OV	**Forwarding engine FIFO overflow interrupt**
7:5	REV1	**Reserved**
4	QTX_REQ_EMP_VQ	**QDMA TX request to transmit an empty VQ**
3:1	REV0	**Reserved**
0	RLS_DONE_INT	**CPU enqueue transmitted packet interrupt**

1B101A1C QDMA_INT_MA Interrupt Mask 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT	REV3										RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	W1C	DC										RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0	REV2			FWD_FIFO_OV	REV1			QTX_REQ_EMP_VQ	REV0			RLS_DONE_INT
Type	RW	RW	RW	RW	DC			RW	DC			W1C	DC			RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_COHERENT	**Interrupt enable for RX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
30	RX_DLY_INT	**Summary of the whole QDMA Rx related interrupts.** 0: Disable interrupt 1: Enable interrupt
29	RLS_COHERENT	**Interrupt enable for TX_DMA data coherent vent** 0: Disable interrupt 1: Enable interrupt
28	RLS_DLY_INT	**Summary of the whole QDMA Tx related interrupts.** 0: Disable interrupt 1: Enable interrupt
27:18	REV3	**Reserved** 0: Disable interrupt 1: Enable interrupt
17	RX_DONE_INT1	**Rx ring #1 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
16	RX_DONE_INT0	**Rx ring #0 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
15	VQDEP_DEQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ not empty yet after de-queuing, but the remainder vq_depth>=1 0: Disable interrupt 1: Enable interrupt
14	VQDEP_DEQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ becomes empty after de-queuing but the remainder vq_depth=0 0: Disable interrupt 1: Enable interrupt
13	VQDEP_ENQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ be en-queued the first packet descirptor, but the vq_depth already >=1. 0: Disable interrupt 1: Enable interrupt
12	VQDEP_ENQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ be en-queued a packet descirptor, but the vq_depth already full = 16'hffff. 0: Disable interrupt 1: Enable interrupt
11:9	REV2	**Reserved**

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Bit(s)	Name	Description
8	FWD_FIFO_OV	**Forwarding engine FIFO overflow interrupt** 0: Disable interrupt 1: Enable interrupt
7:5	REV1	**Reserved**
4	QTX_REQ_EMP_VQ	**QDMA TX request to transmit an empty VQ**
3:1	REV0	**Reserved**
0	RLS_DONE_INT	**CPU release transmitted packet interrupt** 0: Disable interrupt 1: Enable interrupt

1B101A20 QDMA_INT_GRP1 QDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP1	**Interrupt group 1 assignment.** Each bit's definition is same as "QDMA_INT_STS" 0: Leave to QDMA int group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0) 1: Assign to QDMA int group 1

1B101A24 QDMA_INT_GRP2 QDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP2	**Interrupt group 2 assignment.** Each bit's definition is same as "QDMA_INT_STS" 0: Leave to QDMA int group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0) 1: Assign to QDMA int group 2

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1B101A2C **QDMA_DROP_PREC** **QDMA Drop by FFA Percentage Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SW_DROP_PREC	**QDMA SW Drop by FFA Percentage Control** QDMA drop packets based on the full percertage of Free-for-All [31:16] = [PQ#15:PQ#0] 0: Disable drop by FFA percentage 1: Enable drop by FFA percentage
15:0	HW_DROP_PREC	**QDMA HW Drop by FFA Percentage Control** QDMA drop packets based on the full percertage of Free-for-All [15:0] = [PQ#15:PQ#0] 0: Disable drop by FFA percentage 1: Enable drop by FFA percentage

1B101A30 **QDMA_TEST** **Test Mode** **80000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQID_VLD_DLY		CLR_EVQVLD	MONITOR_LAST	VQTB_DIS	FREE_DIS	RLS_DIS	FWD_DIS	DBG_SEL			LP_MODE			FORCE_VQUE[9:8]	
Type	RW		RW	RW	RW	RW	RW	RW	RW			RW			RW	
Reset	1	0	0	0	0	0	0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_VQUE[7:0]								FORCE_SOURCE	FORCE_PORT			FORCE_QUE			
Type	RW								RW	RW			RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	VQID_VLD_DLY	**VQID valid extra cycle delay** Virtual queue selection circuit is timing critical path, may need to be set as multi-cycle path for high frequency timing closure. User can adjust this setting to fit the multi-cycle timing. 0: Select VQ from VQ valid pool in 1 cycle 1: Select VQ from VQ valid pool in 2 cycle 2: Select VQ from VQ valid pool in 3 cycle 3: Select VQ from VQ valid pool in 4 cycle
29	CLR_EVQVLD	**Enable the clear error VQ valid bit map procedure, when QDMA TX request to transmit an empty virtual queue.** 0: not clear the corresponding VQ valid bit map of hardware 1: clear the corresponding VQ valid bit map of hardware
28	MONITOR_LAST	**Control the QDMA_MONITOR mode** 0: Record the first error interrupt event's information into QDMA_MONITOR 1: Record the first error interrupt event's information into QDMA_MONITOR
27	VQTB_DIS	**Disable QDMA Virtual Queue Table Engine**

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Bit(s)	Name	Description
		0: normal 1: disable QDMA virtual queue table engine
26	FREE_DIS	**Disable QDMA Free Engine** 0: normal 1: disable QDMA free engine
25	RLS_DIS	**Disable QDMA Release Engine** 0: normal 1: disable QDMA release engine
24	FWD_DIS	**Disable QDMA Forward Engine** 0: normal 1: disable QDMA forward engine
23:21	DBG_SEL	**Debug probe signals selection**
20	LP_MODE	**QDMA HW loop-back mode enable** When this bit is set, FORCE_PCD, FORCE_PORT, and FORCE_QUE is used instead of the TX_INFO in TX descriptor. 0: normal 1: loop-back test mode
17:8	FORCE_VQUE	**QDMA HW loop-back virtual queue**
7	FORCE_SOURCE	**QDMA HW loop-back to source port**
6:4	FORCE_PORT	**QDMA HW loop-back destination PSE port**
3:0	FORCE_QUE	**QDMA HW loop-back queue**

1B101A34 QDMA_DMA QDMA DMA FSM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				VQTB_FSM				REV1				FQ_FSM			
Type	RO				RO				DC				RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2				TX_FSM				REV3				RX_FSM			
Type	DC				RO				DC				RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	
27:24	VQTB_FSM	**QDMA Virtual Queue Table Engine FSM**
23:20	REV1	
19:16	FQ_FSM	**QDMA Free Queue FSM**
15:12	REV2	
11:8	TX_FSM	**QDMA TX FSM**
7:5	REV3	
4:0	RX_FSM	**QDMA RX FSM**

1B101A38 QDMA_BMU QDMA BMU FSM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0					RLS_FSM										
Type	RO					RO										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	FWD_FSM														
Type	DC	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:27	REV0	
26:16	RLS_FSM	**QDMA Release FSM**
15	REV1	
14:0	FWD_FSM	**QDMA Forward FSM**

1B101A3C QDMA_MON QDMA Monitor for Error Interrupt Event 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QTX_ID			
Type													W1C			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VQTX_ID									
Type							W1C									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	QTX_ID	**The physical queue ID for the error interrupt event**
9:0	VQTX_ID	**The virtual queue ID for the error interrupt event**

1B101A40 QDMA_HRED1 QDMA HW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	**Low Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	**Middle Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

1B101A44 QDMA_HRED2 QDMA HW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															FFA_UTIL_

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																SEL
Type	DC															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_HIGH_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REV0	**Reserved**
16	FFA_UTIL_SEL	**Manually Set FFA Utilization** When the bit is set, FFA Utilization will be configurable for user.
15:0	FFA_HIGH_UTIL	**High Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

1B101A48 QDMA_SRED1 QDMA SW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	**Low Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	**Middle Utilization of FFA on CPU path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

1B101A4C QDMA_SRED2 QDMA SW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															FFA_UTIL_SEL
Type	DC															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REV0	**Reserved**
16	FFA_UTIL_SEL	**Manually Set FFA Utilization** When the bit is set, FFA Utilization will be configurable for user.

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Bit(s)	Name	Description
15:0	FFA_MIDDLE_UTIL	**High Utilization of FFA on CPU path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

1B101A50 QTX_Q0MIN_BKQDMA Queue #0 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIN_BUCKET	**The Token Value of the MIN Bucket.**

1B101A54 QTX_Q1MIN_BKQDMA Queue #1 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIN_BUCKET	**The Token Value of the MIN Bucket.**

1B101A58 QTX_Q2MIN_BKQDMA Queue #2 Min. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIN_BUCKET	**The Token Value of the MIN Bucket.**

1B101A5C QTX_Q3MIN_BKQDMA Queue #3 Min. Bucket 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MIN_BUCKET	**The Token Value of the MIN Bucket.**

1B101A60 QTX_Q0MAX_BK QDMA Queue #0 Max. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAX_BUCKET	**The Token Value of the MAX Bucket.**

1B101A64 QTX_Q1MAX_BK QDMA Queue #1 Max. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAX_BUCKET	**The Token Value of the MAX Bucket.**

1B101A68 QTX_Q2MAX_BK QDMA Queue #2 Max. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BUCKET[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAX_BUCKET	**The Token Value of the MAX Bucket.**

1B101A6C QTX_Q3MAX_BK QDMA Queue #3 Max. Bucket 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_BUCKET[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_BUCKET[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAX_BUCKET	**The Token Value of the MAX Bucket.**

1B101A70 QDMA_INT_STS_G0 QDMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G0	**Interrupt group 0 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is same as "QDMA_INT_STS"

1B101A74 QDMA_INT_STS_G1 QDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	QDMA_INT_STS_G1	**Interrupt group 1 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is same as "QDMA_INT_STS"

1B101A78 QDMA_INT_STS_G2 QDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G2	**Interrupt group 2 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is same as "QDMA_INT_STS"

1B101A80 VQTX_GLO TX Virtual Queue Global Configuration 000005EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															VQTB_MIB_EN	
Type															RW	
Reset															0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_GQTUM														
Type		RW														
Reset		0	0	0	0	1	0	1	1	1	1	0	1	0	1	0

Bit(s)	Name	Description
17	VQTB_MIB_EN	**Configuration for the MIB packet/byte counter field of virtual queue table** 0: Disable MIB counter field, each virtual table entry is 16bytes 1: Enable MIB counter field, each virtual table entry extends to 32bytes, to record the amount of transmitted byte and packet count for each virtual queue
14:0	VQTX_GQTUM	**Amount of bytes a virtual queue is allowed to de-queue before the scheduler moves to the next virtual queue. Defaults to the MTU of the interface. The minimum value is 1.**

1B101A8C VQTX_INVLD_PTR TX Virtual Queue Invalid Pointer DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_INVLD_PTR[31:16]															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	VQTX_INVLD_PTR[15:0]															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	VQTX_INVLD_PTR	**The pointer address indicates a invalid virtual queue head/tail pointer.** Either "VQHPTR" or "VQTPTR" of VQ table is equal to this invalid pointer VQTX_INVLD_PTR, which means there is no valid packet in this virtual queue.

1B101A90 VQTX_NUM Number of TX Virtual Queue Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_NUM_3				VQTX_NUM_2				VQTX_NUM_1				VQTX_NUM_0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	VQTX_NUM_3	**Number of virtual queues in physical queue #3**
10:8	VQTX_NUM_2	**Number of virtual queues in physical queue #2**
6:4	VQTX_NUM_1	**Number of virtual queues in physical queue #1**
2:0	VQTX_NUM_0	**Number of virtual queues in physical queue #0** 0: disable virtual queue function 1: 32 2: 64 3: 128 4: 256 5: 512 6: 1024 7: reserved

1B101A98 VQTX_SCH TX Virtual Queue Schedule Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VQTX_SCH_3				VQTX_SCH_2				VQTX_SCH_1				VQTX_SCH_0	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
13:12	VQTX_SCH_3	**Virtual queues scheduling strategy for physical queue #3**
9:8	VQTX_SCH_2	**Virtual queues scheduling strategy for physical queue #2**
5:4	VQTX_SCH_1	**Virtual queues scheduling strategy for physical queue #1**
1:0	VQTX_SCH_0	**Virtual queues scheduling strategy for physical queue #0**

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Bit(s)	Name	Description
		0: SFQ (packet base round robin) 1: DRR (deficit round robin) 2: Reserved 3: Reserved

1B101AA0 **VQTX_HASH_CFG** **TX Virtual Queue Hash Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HASH_PTB_MODE_EN_3	HASH_PTB_MODE_EN_2	HASH_PTB_MODE_EN_1	HASH_PTB_MODE_EN_0			HASH_ST_MODE					HASH_PTB_PRD[16:16]
Type					RW	RW	RW	RW			RW					RW
Reset					0	0	0	0			0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_PTB_PRD[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	HASH_PTB_MODE_EN_3	**Enable "Exclusive with CRC32" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**
26	HASH_PTB_MODE_EN_2	**Enable "Exclusive with (B^(A&~C))" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**
25	HASH_PTB_MODE_EN_1	**Enable "Exclusive with (A&B)|(~A&C)" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.**
24	HASH_PTB_MODE_EN_0	**Enable "Exclusive with HASH_SEED" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PTB_PRD!=0.** (If HASH_PTB_MODE_EN_0~3 are all "0", hash will be forced on "Exclusive with HASH_SEED" mode.)
21:20	HASH_ST_MODE	**Hash scrambled mode selection, for static hash virtual queue index generating.** This field only valid when HASH_PTB_PRD=0 3: Exclusive with CRC32 2: Exclusive with (B^(A&~C)) 1: Exclusive with (A&B)|(~A&C) 0: Exclusive with HASH_SEED
16:0	HASH_PTB_PRD	**If HASH_PTB_PRD = 0, means operating in static hash mode, never changing the hash algorithm periodically.** Otherwise, operating in perturb hash mode when HASH_PTB_PRD != 0. HASH_PERTURB_PRD Indicates the period to change the hash algorithm for virtual queue index generating, in 1ms unit.

1B101AA4 **VQTX_HASH_SD** **TX Virtual Queue Hash Seed** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_SD[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_SD[15:0]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HASH_SD	**Hash seed for "Exclusive with HASH_SEED" mode.**

1B101AB0 VQTX_VLD_CFG TX Virtual Queue Valid Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_VLD_STRG_3				VQTX_VLD_STRG_2				VQTX_VLD_STRG_1				VQTX_VLD_STRG_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	VQTX_VLD_STRG_3	**Physical Queue#3: Virtual queue valid bit map starting group number.**
11:8	VQTX_VLD_STRG_2	**Physical Queue#2: Virtual queue valid bit map starting group number.**
7:4	VQTX_VLD_STRG_1	**Physical Queue#1: Virtual queue valid bit map starting group number.**
3:0	VQTX_VLD_STRG_0	**Physical Queue#0: Virtual queue valid bit map starting group number.** 1 VQ valid group comprises 64 bit map. The number of VQ valid groups for 1 PQ depends on the setting of "VQTX_NUM_#", and hardware allocates groups for each PQ automatically. 4'h0: VQ valid bit map starting from group#0 4'h1: VQ valid bit map starting from group#1 4'h15: VQ valid bit map starting from group#15

1B101ABC VQTX_MIB_IF TX Virtual Queue MIB Interface 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VQTB_MIB_RC_DIS	VQTX_MIB_EN				MIB_PQ_SHW_SEP					VQTX_MIB_QID			
Type			RW	W1				RW					RW			
Reset			0	0				0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VQTX_MIB_VQID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	VQTB_MIB_RC_DIS	**Disable the clear action during MIB reading** Invalid when VQTB_MIB_EN = 0 0: After MIB reading done, the target VQ MIB counter will be clear to 0 1: Keeps the value of target VQ MIB counter after MIB reading
28	VQTX_MIB_EN	**Enable VQTB MIB read procedure** 0: After MIB accessing done, HW will clear this bit to 0 and put the result in VQTX_MIB_PCNT, VQTX_MIB_BCNT0, VQTX_MIB_BCNT1

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Bit(s)	Name	Description
		1: Enable MIB accessing procedure
24	MIB_PQ_SHW_SEP	**Seperate the PQ's HW/SW MIB counter of QTX_MIB_PCNT and QTX_MIB_DPCNT** 0: Use whole 32bits as one MIB counter, which accumulates SW and HW packet count 1: Separate the SW and HW MIB counter
19:16	VQTX_MIB_QID	**Physical queue ID for VQTB MIB accessing**
9:0	VQTX_MIB_VQID	**Virtual queue ID for VQTB MIB accessing**

1B101AC0 VQTX_MIB_PCNT TX Virtual Queue MIB Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_PCNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_PCNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_PCNT	**Packet count of virtual queue table, according to VQTX_MIB_QID and VQTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101AC4 VQTX_MIB_BCNT0 TX Virtual Queue MIB Byte Count 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNT0[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNT0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNT0	**Byte count [31:0] of virtual queue table, according to VQTX_MIB_QID and VQTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101AC8 VQTX_MIB_BCNT1 TX Virtual Queue MIB Byte Count 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNT1[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNT1[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNT1	**Byte count [63:32] of virtual queue table, according to VQTX_MIB_QID and VQTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101ACC VQTX_MIB_DPCNT TX Virtual Queue MIB Drop Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_DPCNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_DPCNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_DPCNT	**Dropped packet count of virtual queue table, according to VQTX_MIB_QID and VQTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

1B101AD0 QTX_MIB_PCNT TX Queue MIB Forward Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_PCNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_PCNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_PCNT	**Accumulated forwarded packet count, according to VQTX_MIB_QID.** If MIB_PQ_SHW_SEP = 1, this counter will be seperated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

1B101AD4 QTX_MIB_DPCNT TX Queue MIB Dropped Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_DPCNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	QTX_MIB_DPCNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_DPCNT	**Accumulated dropped packet count, according to VQTX_MIB_QID.** If MIB_PQ_SHW_SEP = 1, this counter will be seperated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

1B101B00 QTX_CTX_PTR TX Forward CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_CTX_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_CTX_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_CTX_PTR	**TX forward chain CPU pointer**

1B101B04 QTX_DTX_PTR TX Forward DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_DTX_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_DTX_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_DTX_PTR	**Tx forward chain DMA pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B08 QTX_FWD_CNT TX Forward DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACC_HW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_SW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:16	ACC_HW_CNT	**Accumulated HW forwarded counter**
15:0	ACC_SW_CNT	**Accumulated SW forwarded counter**

1B101B10 QTX_CRX_PTR TX Release CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_CRX_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_CRX_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_CRX_PTR	**TX release chain CPU pointer**

1B101B14 QTX_DRX_PTR TX Release DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_DRX_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DRX_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_DRX_PTR	**Tx release chain DMA pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B18 QTX_RLS_CNT TX Release DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_RLS_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:0	ACC_RLS_CNT	**Accumulated TX released descriptor count**

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1B101B20 QDMA_FQ_HEAD Free Page Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_HEAD_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_HEAD_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_HEAD_PTR	**Free buffer head pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B24 QDMA_FQ_TAIL Free Page Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_TAIL_PTR[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_TAIL_PTR[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_TAIL_PTR	**Free buffer tail pointer** When QDMA TX is diabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

1B101B28 QDMA_FQ_CNT Free Page Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SWFQ_CNT	**Free buffer on CPU Pool** Initial free buffer count on CPU pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.
15:0	HWFQ_CNT	**Free buffer on HW Pool** Initial free buffer count on HW pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.

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1B101B2C QDMA_FQ_BLEN Free Page Buffer Length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		FQ_BUF_BLEN													
Type	DC		RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	
29:16	FQ_BUF_BLEN	**Free buffer byte length** Configured free buffer length, QDMA RX will fetch the length info to decide the payload length on one descriptor/buffer.
15:0	REV1	

1B101B80 QDMA_RATE_EXP0 QDMA Scheduler Rate Exponent 0 000F4240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QDMA_RATE_EXP0[19:16]			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_RATE_EXP0[15:0]															
Type	RW															
Reset	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
19:0	QDMA_RATE_EXP0	**Exponent part of the QDMA scheduler rate control** Rate(bps) = clock_frequency*8*(RATE_MAN/RATE_EXP) Bucket clock frequency is based on the setting of BKTCLK_ASYNC. BKTCLK_ASYNC = 0, bucket clock is system bus clock BKTCLK_ASYNC = 1, bucket clock is a dedicated 125Mhz clock 20'hF4240: Provide 1kbps rate control (default setting with BKTCLK_ASYNC=1 and RATE_MAN=1)

1B101B84 QDMA_RATE_EXP1 QDMA Scheduler Rate Exponent 1 000186A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QDMA_RATE_EXP1[19:16]			
Type													RW			
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_RATE_EXP1[15:0]															
Type	RW															
Reset	1	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0

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Bit(s)	Name	Description
19:0	QDMA_RATE_EXP1	**Exponent part of the QDMA scheduler rate control** 20'h186A0: Provide 10kbps rate control (default setting with BKTCLK_ASYNC=1 and RATE_MAN=1)

1B101B88 QDMA_RATE_EXP2 QDMA Scheduler Rate Exponent 2 00002710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QDMA_RATE_EXP2[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_RATE_EXP2[15:0]															
Type	RW															
Reset	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
19:0	QDMA_RATE_EXP2	**Exponent part of the QDMA scheduler rate control** 20'h02710: Provide 100kbps rate control (default setting with BKTCLK_ASYNC=1 and RATE_MAN=1)

1B101B8C QDMA_RATE_EXP3 QDMA Scheduler Rate Exponent 3 000003E8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QDMA_RATE_EXP3[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_RATE_EXP3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0

Bit(s)	Name	Description
19:0	QDMA_RATE_EXP3	**Exponent part of the QDMA scheduler rate control** 20'h003E8: Provide 1Mbps rate control (default setting with BKTCLK_ASYNC=1 and RATE_MAN=1)

1B101B90 QDMA_RATE_EXP4 QDMA Scheduler Rate Exponent 4 00000064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QDMA_RATE_EXP4[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_RATE_EXP4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

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Bit(s)	Name	Description
19:0	QDMA_RATE_EXP4	**Exponent part of the QDMA scheduler rate control** 20'h00064: Provide 10Mbps rate control (default setting with BKTCLK_ASYNC=1 and RATE_MAN=1)

1B101B94 QDMA_RATE_EXP5 QDMA Scheduler Rate Exponent 5 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													QDMA_RATE_EXP5[19:16]			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_RATE_EXP5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
19:0	QDMA_RATE_EXP5	**Exponent part of the QDMA scheduler rate control** 20'h0000A: Provide 100Mbps rate control (default setting with BKTCLK_ASYNC=1 and RATE_MAN=1)

1B101BA0 VQTX_DEP_TH QDMA Virtual Queue Depth Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_DEP_TH_3								VQTX_DEP_TH_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_DEP_TH_1								VQTX_DEP_TH_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	VQTX_DEP_TH_3	**Per virtual queue depth threshold in physical queue #3**
23:16	VQTX_DEP_TH_2	**Per virtual queue depth threshold in physical queue #2**
15:8	VQTX_DEP_TH_1	**Per virtual queue depth threshold in physical queue #1**
7:0	VQTX_DEP_TH_0	**Per virtual queue depth threshold in physical queue #0** 0: disable virtual queue depth threshold Others: discard packet when virtual queue depth reachs this threshold value

1B101BA8 VQTX_DEP_TH2 QDMA Virtual Queue Depth Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_DEP_TH_3								VQTX_DEP_TH_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_DEP_TH_1								VQTX_DEP_TH_0							
Type	RW								RW							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	VQTX_DEP_TH_3	**Per virtual queue depth threshold in physical queue #3**
23:16	VQTX_DEP_TH_2	**Per virtual queue depth threshold in physical queue #2**
15:8	VQTX_DEP_TH_1	**Per virtual queue depth threshold in physical queue #1**
7:0	VQTX_DEP_TH_0	**Per virtual queue depth threshold in physical queue #0** 0: disable virtual queue depth threshold Others: discard packet when virtual queue depth reachs this threshold value

2.4.1 Frame Engine MIB Counters

Base Address: 1B00_0000 (ex: PPE_AC_BCNT0 address is 1B00_2000)

Counter Table			
Offset	**Name**	**Width**	**Description**
0x2000	**PPE_AC_BCNT0**	**64**	**PPE Accounting Group #0 Byte Counter**
0x2008	**PPE_AC_PCNT0**	**32**	**PPE Accounting Group #0 Packet Counter**
0x200C	**PPE_MTR_CNT0**	**32**	**PPE Meter Group #0**
0x2010	**PPE_AC_BCNT1**	**64**	**PPE Accounting Group #1 Byte Counter**
0x2018	**PPE_AC_PCNT1**	**32**	**PPE Accounting Group #1 Packet Counter**
0x201C	**PPE_MTR_CNT1**	**32**	**PPE Meter Group #1**
…..	**…..**		
0x23F0	**PPE_AC_BCNT63**	**64**	**PPE Accounting Group #63 Byte Counter**
0x23F8	**PPE_AC_PCNT63**	**32**	**PPE Accounting Group #63 Packet Counter**
0x23FC	**PPE_MTR_CNT63**	**32**	**PPE Meter Group #63**
0x2400	**GDM1_RX_GBCNT**	**64**	**Received good byte count for GDM1**
0x2408	**GDM1_RX_GPCNT**	**32**	**Received good packet count for GDM1**
0x240C	**-**	**32**	**Reserved**
0x2410	**GDM1_RX_OERCNT**	**32**	**Recevied overflow error packet count for GDM1**
0x2414	**GDM1_RX_FERCNT**	**32**	**Recevied FCS error packet count for GDM1**
0x2418	**GDM1_RX_SERCNT**	**32**	**Recevied too short error packet count for GDM1**
0x241C	**GDM1_RX_LERCNT**	**32**	**Recevied too long error packet count for GDM1**
0x2420	**GDM1_RX_CERCNT**	**32**	**Recevied IP/TCP/UDP checksum error packet count for GDM1**
0x2424	**GDM1_RX_FCCNT**	**32**	**Recevied flow control packet count for GDM1**
0x2428	**GDM1_TX_SKIPCNT**	**32**	**Transmit abort count for GDM1**
0x242C	**GDM1_TX_COLCNT**	**32**	**Transmit collision count for GDM1**
0x2430	**GDM1_TX_GBCNT**	**64**	**Trasnmit good byte count for GDM1**
0x2438	**GDM1_TX_GPCNT**	**32**	**Transmit good packet count for GDM1 (exlcude flow control frames)**
0x243C	**-**	**32**	**Reserved**

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Bit(s)	Name	Description	
0x2440	GDM2_RX_GBCNT	64	Received good byte count for GDM2
0x2448	GDM2_RX_GPCNT	32	Received good packet count for GDM2
0x244C	-	32	Reserved
0x2450	GDM2_RX_OERCNT	32	Recevied overflow error packet count for GDM2
0x2454	GDM2_RX_FERCNT	32	Recevied FCS error packet count for GDM2
0x2458	GDM2_RX_SERCNT	32	Recevied too short error packet count for GDM2
0x245C	GDM2_RX_LERCNT	32	Recevied too long error packet count for GDM2
0x2460	GDM2_RX_CERCNT	32	Recevied IP/TCP/UDP checksum error packet count for GDM2
0x2464	GDM2_RX_FCCNT	32	Recevied flow control packet count for GDM2
0x2468	GDM2_TX_SKIPCNT	32	Transmit abort count for GDM2
0x246C	GDM2_TX_COLCNT	32	Transmit collision count for GDM2
0x2470	GDM2_TX_GBCNT	64	Trasnmit good byte count for GDM2
0x2478	GDM2_TX_GPCNT	32	Transmit good packet count for GDM2 (exlcude flow control frames)
0x247C	-	32	Reserved

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3 GMAC

3.1 Introduction

Gigabit Ethernet is constructured by a single, compact component with two full-integrated Gigabit Media Access Control (GMAC) ports.The two GMAC ports are connected to the Frame Engine to perform the wire-speed NAT process between LAN and WAN domain. To communicate with the external GePHY, GMAC also provide the Serial Management Interface running up to 12.5MHz.

3.2 Feature List

- Follow IEEE Std. 802.3 MAC layer protocol
- VLAN support compliant with IEEE Std 802.1Q specifiction
- Supports 802.3x flow control for full duplex operation and backpressure flow control for half duplex operation.
- Energy Efficient Ethernet (EEE) support compliant with IEEE Std 802.3az
- Support Wake-on-Lan or Interrupt by the Magic packet
- Support the flexible PHY interfaces - MII/RMII/RGMII and TRGMII (GMAC1 only)
- Support Clause 22 and 45 MDIO access and GePHY auto-polling on SMI master.

3.3 Block Diagram

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3.4 Register Definition

Module name: GMAC Base address: (+1b110000h)

Address	Name	Width	Register Function
1b110000	MAC_PPSC	32	PHY Polling and SMI Master Control
1b110004	MAC_PIAC	32	PHY Indirect Access Control
1b110008	MAC_GPC	32	GIGA MAC Port Control
1b110100	MAC_P1_MCR	32	Port 1 MAC Control
1b110104	MAC_P1_EEE	32	Port 1 EEE Control
1b110108	MAC_P1_SR	32	Port 1 MAC Status
1b11010c	MAC_P1_FSM	32	Port 1 FSM
1b110200	MAC_P2_MCR	32	Port 2 MAC Control
1b110204	MAC_P2_EEE	32	Port 2 EEE Control
1b110208	MAC_P2_SR	32	Port 2 MAC Status
1b11020c	MAC_P2_FSM	32	Port 2 FSM
1b110210	MAC_P2_WOL	32	Port 2 WOL

1B110000 MAC_PPSC PHY Polling and SMI Master Control 05000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_AP_EN	PHY_PRE_EN	PHY_MDC_CFG						RESV0			MDC_TURBO	RESV1		EE_AN_EN	
Type	RW	RW	RW						DC			RW	DC		RW	
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV2			PHY_END_ADDR					RESV3			PHY_START_ADDR				
Type	DC			RW					DC			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PHY_AP_EN	**PHY auto polling enable** Indicate all PHY's status will be updated to PHY's status regsiters by PHY polling process.
30	PHY_PRE_EN	**PHY preample enable** Indicates SMI master will send preamble bits (32-bits) at each MDIO read/write transaction. [note] This bit will affect both PHY polling mode and PHY indirect access mode.
29:24	PHY_MDC_CFG	**PHY MDC clock configuration** Used to configure the divider N for MDC clock frequency. MDC clock is sourced from 12.5MHz system clock and divided by N. [note] MDC clock is gated or disabled when PHY_MDC_CFG is

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Bit(s)	Name	Description
		set to 0.
23:21	RESV0	**Reserved**
20	MDC_TURBO	**MDC clock Turbo mode** When this bit is set, MDC clock is sourced from 25MHz system clock and divided by PHY_MDC_CFG.
19:18	RESV1	**Reserved**
17:16	EE_AN_EN	**PHY EEE auto-polling enable**
15:13	RESV2	**Reserved**
12:8	PHY_END_ADDR	**PHY Ppolling end address** Indicate the end of PHY address of PHY auto-polling process. [note] The difference between and start and end must be 1.
7:5	RESV3	**Reserved**
4:0	PHY_START_ADDR	**PHY Ppolling start address** Indicate the start of PHY address of PHY auto-polling process.

1B110004 MAC_PIAC PHY Indirect Access Control 00090000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_ACS_ST	RESV0	MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		NMDIO_ST	
Type	W1C	DC	RW					RW					RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDIO_RW_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PHY_ACS_ST	**PHY access start** Start to indirect access PHY's register. While PHY's register access is complete, this bit will be self-cleared to 0. 0: Idle or indirect access complete

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Bit(s)	Name	Description
		1: Start PHY access
30	RESV0	**Reserved**
29:25	MDIO_REG_ADDR	**Register Address (Clause 22) or Device Address (Clause 45)**
24:20	MDIO_PHY_ADDR	**PHY Address (Clause 22) or Port Address (Clause 45)**
19:18	MDIO_CMD	**MDIO command** 2'b00: Address (Clause 45) 2'b01: MDIO write 2'b10: MDIO read (Clause 22) / Read inc (Clause 45) 2'b11: MDIO read (Clause 45)
17:16	NMDIO_ST	**MDIO Start Field** 2'b00: Start (Clause 45) 2'b01: Start (Clause 22) other: Reserved
15:0	MDIO_RW_DATA	**MDIO Read/Write data** This is used as MDIO data field for read/write data access. When MDIO write command is activated, this is used as MDIO write data field. When MDIO read command is activated, this is used as MDIO read data field for read access only.

1B110008 MAC_GPC GIGA MAC Port Control 000C000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0						P2_RMII_CKRX	P2_RMII_CKIN	RESV1		P2_TMII_FREQ	P2_TMII_MODE	P2_TX_CLK_MODE	P2_RX_CLK_MODE	P2_RX_SKEW	
Type	DC						RW	RW	RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV2										P1_TMII_FREQ	P1_TMII_MODE	P1_TX_CLK_MODE	P1_RX_CLK_MODE	P1_RX_SKEW	
Type	DC										RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

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Bit(s)	Name	Description
31:26	RESV0	**Reserved**
25	P2_RMII_CKRX	**RMII Reference Clock Pin Selection** 0: TXC 1: RXC
24	P2_RMII_CKIN	**RMII Reference Clock Direction** 0: Output 1: Input
23:22	RESV1	**Reserved**
21	P2_TMII_FREQ	
20	P2_TMII_MODE	**TMII mode** Switch to Turbot MII mode
19	P2_TX_CLK_MODE	**P2 TX clcok control** 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data is 90 degree offset)
18	P2_RX_CLK_MODE	**P2 RX clock control** 0: delay 2ns on input rx_clk 1: no delay
17:16	P2_RX_SKEW	**P2 RX clock skew control** 2'b00: no dealy 2'b01: delay 150ps 2'b10: dealy 300ps 2'b11: clock inversion
15:6	RESV2	**Reserved**
5	P1_TMII_FREQ	
4	P1_TMII_MODE	**TMII mode** Switch to Turbot MII mode
3	P1_TX_CLK_MODE	**P1 TX clcok control** 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data is 90 degree offset)
2	P1_RX_CLK_MODE	**P1 RX clock control** 0: delay 2ns on input rx_clk

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Bit(s)	Name	Description
		1: no delay
1:0	P1_RX_SKEW	**P1 RX clock skew control** 2'b00: no dealy 2'b01: delay 150ps 2'b10: dealy 300ps 2'b11: clock inversion

1B110100 MAC_P1_MCR Port 1 MAC Control 20006300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_RX_JUMBO				RESV0		MAC_RX_PKT_LEN		MTCC_LMT				IPG_CFG		RESV1	
Type	RW				DC		RW		RW				RW		DC	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE	MAC_TX_EN	MAC_RX_EN	RESV2		PRMBL_LMT_EN	BKOFF_EN	BACKPR_EN	FORCE_EEE1G	FORCE_EEE100	FORCE_RX_FC	FORCE_TX_FC	FORCE_SPD		FORCE_DPX	FORCE_LINK
Type	RW	RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_RX_JUMBO	**Maximum received jumbo packet length** 4'h0, 4'h1: Reserved 4'h2: 2 Kbytes (maxi. length on FE/GDM) 4'h3 .. 4'hF: Reserved
27:26	RESV0	
25:24	MAC_RX_PKT_LEN	**Maximum received packet length** Sets the maximum length of ingress packets including CRC that can be received by MAC. 00: 1518 bytes for untagged frames; 1522 bytes for tagged frames 01: 1536 bytes 10: 1552 bytes 11: MAX_RX_JUMBO

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Bit(s)	Name	Description
23:20	MTCC_LMT	**MTCC limit** Maximum transmit collision count limitation. 0: Disable TX collision abort function, send packet until successfully 1 ~ 15: Maximum transmit collision count
19:18	IPG_CFG	**Inter-Frame Gap Shrink** 2'b00: normal 96-bits IFG 2'b01: Transmit 96-bits IFG with short IFG in random behavior. 2'b10: shrink 64-bits IFG 2'b11: When any output queue inside the port is congested, shrink 64-bits IFG will be enabled; otherwise, normal 96-bits IFG will be the default.
17:16	RESV1	**Reserved**
15	FORCE_MODE	**Force MAC Mode** 0: force mode off (MAC status is decided by PHY auto-polling) 1: force mode on (MAC status is determined by FORCE_XXX register)
14	MAC_TX_EN	**TX MAC Enable** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN	**RX MAC Enable** 0: RX MAC function is disabled 1: RX MAC function is enabled
12:11	RESV2	**Reserved**
10	PRMBL_LMT_EN	**Preamble Limit Enable** 0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble. 1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD.
9	BKOFF_EN	**Back-off Enable** 0: disabled 1: Let MAC follow the back-off mechanism when collision happens
8	BACKPR_EN	**Back-Pressure enable** 0: disabled

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Bit(s)	Name	Description
		1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on
7	FORCE_EEE1G	**Force LPI mode for 1000m link speed** When (FORCE_MODE= 1), these bits are used to control MAC EEE mode 0: Donot have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	FORCE_EEE100	**Force LPI mode for 100m link speed** When (FORCE_MODE= 1), these bits are used to control MAC EEE mode 0: Donot have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	FORCE_RX_FC	**Force RX flow cotnrol** When (FORCE_MODE= 1), these bits are used to control MAC RX flow control 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	FORCE_TX_FC	**Force Tx flow cotnrol** When (FORCE_MODE= 1), these bits are used to control MAC TX flow control 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	FORCE_SPD	**Force link speed** When (FORCE_MODE= 1), these bits are used to control MAC link speed 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: reserved
1	FORCE_DPX	**Force duplex** When (FORCE_MODE= 1), these bits are used to control MAC link duplex 0: Half-duplex 1: Full-duplex
0	FORCE_LINK	**Force link state** When (FORCE_MODE= 1), these bits are used to control MAC link state 0: Link down

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Bit(s)	Name	Description
		1: Link up

1B110104 MAC_P1_EEE Port 1 EEE Control 111E1E02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000								WAKEUP_TIME_100							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_TXIDLE_THD								RESV0				CKG_TXIDLE	CKG_RXLPI	TX_DOWN_REQ	LPI_MODE
Type	RW								RW				RW	RW	RW	RW
Reset	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000	**Wake up time for 1000mbps LIP mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
23:16	WAKEUP_TIME_100	**Wake up time for 100mbps LIP mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
15:8	LPI_TXIDLE_THD	**TX IDLE timer to enter LPI mode** When there is no packet to be transmitted and exceeds time period specified by LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner Time unit: 1ms
7:4	RESV0	**Reserved**
3	CKG_TXIDLE	**TX Clock Power Down** 0: disable 1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.
2	CKG_RXLPI	**RX Clock Power Down** 0: disable 1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.

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Bit(s)	Name	Description
1	TX_DOWN_REQ	**TX DMA Request** Keep TX request when this port is linked down 0: No TX request 1: Keep TX request when this port is linked down.
0	LPI_MODE	**LPI mode activated** 0: DIsable 1: Let the system enter LPI mode immediatedly and send EEE LPI frame to the link partner

1B110108 MAC_P1_SR Port 1 MAC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0								EEE1G_STATUS	EEE100_STATUS	RX_FC_STATUS	TX_FC_STATUS	SPD_STATUS		DPX_STATUS	LINK_STATUS
Type	DC								RO	RO	RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV0	**Reserved**
7	EEE1G_STATUS	**LPI mode for 1000m link speed** 0: Donot have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	EEE100_STATUS	**LPI mode for 100m link speed** 0: Donot have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	RX_FC_STATUS	**RX flow cotnrol status** 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex

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Bit(s)	Name	Description
		mode and flow-control is on
4	TX_FC_STATUS	**TX flow cotnrol status** 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	SPD_STATUS	**Link speed status** 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: reserved
1	DPX_STATUS	**Duplex status** 0: Half-duplex 1: Full-duplex
0	LINK_STATUS	**Link state** 0: Link down 1: Link up

1B11010C MAC_P1_FSM Port 1 FSM 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FE2SW_FSM								SW2FE_FSM							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MAC_FSM								TX_MAC_FSM							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	FE2SW_FSM	**FrameEngine-to-Switch Finite State Machine**
23:16	SW2FE_FSM	**Switch-to-FrameEngine Finite State Machine**
15:8	RX_MAC_FSM	**RX MAC Finite State Machine**
7:0	TX_MAC_FSM	**TX MAC Finite State Machine**

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Bit(s)	Name	Description

1B110200 MAC_P2_MCR Port 2 MAC Control 20006300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_RX_JUMBO				RESV0		MAC_RX_PKT_LEN		MTCC_LMT				IPG_CFG		RESV1	
Type	RW				DC		RW		RW				RW		DC	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE	MAC_TX_EN	MAC_RX_EN	RESV2		PRMBL_LMT_EN	BKOFF_EN	BACKPR_EN	FORCE_EEE1G	FORCE_EEE10	FORCE_RX_FC	FORCE_TX_FC	FORCE_SPD		FORCE_DPX	FORCE_LINK
Type	RW	RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_RX_JUMBO	**Maximum received jumbo packet length** 4'h0, 4'h1: Reserved 4'h2: 2 Kbytes (maxi. length on FE/GDM) 4'h3 .. 4'hF: Reserved
27:26	RESV0	
25:24	MAC_RX_PKT_LEN	**Maximum received packet length** Sets the maximum length of ingress packets including CRC that can be received by MAC. 00: 1518 bytes for untagged frames;1522 bytes for tagged frames 01: 1536 bytes 10: 1552 bytes 11: MAX_RX_JUMBO
23:20	MTCC_LMT	**MTCC limit** Maximum transmit collision count limitation. 0: Disable TX collision abort function, send packet until successfully 1 ~ 15: Maximum transmit collision count
19:18	IPG_CFG	**Inter-Frame Gap Shrink**

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Bit(s)	Name	Description
		2'b00: normal 96-bits IFG 2'b01: Transmit 96-bits IFG with short IFG in random behavior. 2'b10: shrink 64-bits IFG 2'b11: When any output queue inside the port is congested, shrink 64-bits IFG will be enabled; otherwise, normal 96-bits IFG will be the default.
17:16	RESV1	**Reserved**
15	FORCE_MODE	**Force MAC Mode** 0: force mode off (MAC status is decided by PHY auto-polling) 1: force mode on (MAC status is determined by FORCE_XXX register)
14	MAC_TX_EN	**TX MAC Enable** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN	**RX MAC Enable** 0: RX MAC function is disabled 1: RX MAC function is enabled
12:11	RESV2	**Reserved**
10	PRMBL_LMT_EN	**Preamble Limit Enable** 0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble. 1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD.
9	BKOFF_EN	**Back-off Enable** 0: disabled 1: Let MAC follow the back-off mechanism when collision happens
8	BACKPR_EN	**Back-Pressure enable** 0: disabled 1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on
7	FORCE_EEE1G	**Force LPI mode for 1000m link speed** When (FORCE_MODE= 1), these bits are used to control MAC EEE mode 0: Donot have the ability of entering EEE low power idle mode for

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Bit(s)	Name	Description
		1000m link speed 1: Have the ability of entering EEE low power idle mode
6	FORCE_EEE100	**Force LPI mode for 100m link speed** When (FORCE_MODE= 1), these bits are used to control MAC EEE mode 0: Donot have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	FORCE_RX_FC	**Force RX flow cotnrol** When (FORCE_MODE= 1), these bits are used to control MAC RX flow control 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	FORCE_TX_FC	**Force Tx flow cotnrol** When (FORCE_MODE= 1), these bits are used to control MAC TX flow control 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	FORCE_SPD	**Force link speed** When (FORCE_MODE= 1), these bits are used to control MAC link speed 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: reserved
1	FORCE_DPX	**Force duplex** When (FORCE_MODE= 1), these bits are used to control MAC link duplex 0: Half-duplex 1: Full-duplex
0	FORCE_LINK	**Force link state** When (FORCE_MODE= 1), these bits are used to control MAC link state 0: Link down 1: Link up

1B110204 MAC_P2_EEE Port 2 EEE Control 00001E02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	WAKEUP_TIME_1000								WAKEUP_TIME_100							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_TXIDLE_THD								RESV0				CKG_TXIDLE	CKG_RXLPI	TX_DOWN_REQ	LPI_MODE
Type	RW								DC				RW	RW	RW	RW
Reset	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000	**Wake up time for 1000mbps LIP mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
23:16	WAKEUP_TIME_100	**Wake up time for 100mbps LIP mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up Time unit: 1us
15:8	LPI_TXIDLE_THD	**TX IDLE timer to enter LPI mode** When there is no packet to be transmitted and exceeds time period specified by LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner Time unit: 1ms
7:4	RESV0	**Reserved**
3	CKG_TXIDLE	**TX Clock Power Down** 0: disable 1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.
2	CKG_RXLPI	**RX Clock Power Down** 0: disable 1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.
1	TX_DOWN_REQ	**TX DMA Request** Keep TX request when this port is linked down 0: No TX request 1: Keep TX request when this port is linked down.
0	LPI_MODE	**LPI mode activated** 0: Disable

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Bit(s)	Name	Description
		1: Let the system enter LPI mode immediatedly and send EEE LPI frame to the link partner

1B110208 MAC_P2_SR Port 2 MAC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0								EEE1G_STATUS	EEE100_STATUS	RX_FC_STATUS	TX_FC_STATUS	SPD_STATUS		DPX_STATUS	LINK_STATUS
Type	DC								RO	RO	RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV0	**Reserved**
7	EEE1G_STATUS	**LPI mode for 1000m link speed** 0: Donot have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	EEE100_STATUS	**LPI mode for 100m link speed** 0: Donot have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	RX_FC_STATUS	**RX flow cotnrol status** 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	TX_FC_STATUS	**TX flow cotnrol status** 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	SPD_STATUS	**Link speed status**

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Bit(s)	Name	Description
		2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: reserved
1	DPX_STATUS	**Duplex status** 0: Half-duplex 1: Full-duplex
0	LINK_STATUS	**Link state** 0: Link down 1: Link up

1B11020C MAC_P2_FSM Port 2 FSM 01010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FE2SW_FSM								SW2FE_FSM							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MAC_FSM								TX_MAC_FSM							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	FE2SW_FSM	**FrameEngine-to-Switch Finite State Machine**
23:16	SW2FE_FSM	**Switch-to-FrameEngine Finite State Machine**
15:8	RX_MAC_FSM	**RX MAC Finite State Machine**
7:0	TX_MAC_FSM	**TX MAC Finite State Machine**

1B110210 MAC_P2_WOL Port 2 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_INT_CLR	WOL_STS

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Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0												SNP_PKT	CRC_DIS	WOL_INT_EN	WOL_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	**GMAC2 Wake-up On Lan Debug Signals**
17	WOL_INT_CLR	**GMAC2 Wake-up On Lan Interrupt Status**
16	WOL_STS	**GMAC2 Wake-up On Lan Status** If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet. 0: Normal State 1: Listen State and detect magic packet
15:4	RESV0	
3	SNP_PKT	**GMAC2 Wake-up On Lan with snoopy packet**
2	CRC_DIS	**GMAC2 Wake-up On Lan with CRC Check Disable**
1	WOL_INT_EN	**GMAC2 Wake-up On Lan Interrupt Enable**
0	WOL_EN	**GMAC2 Wake-up On Lan Function Enable**

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4 TRGMII

4.1 Introduction

Turbo RGMII (TRGMII) interface translates GMII signals from/to GMAC to/from RGMII signals. It provides a high speed RGMII interface. The maximum clock rate is 325 MHz. Besides, the interface can support RGMII 125 MHz. The TRGMII interface insists of delay line for TX/RX path. The delay taps can be configured.

4.2 Features

- The clock speed range is from 125MHz ~ 325 MHz.
- The delay taps of RX path can be set through SW calibration.

4.3 Block Diagram

Below figures show TRGMII I/F between FE and Giga Switch. And also show the block diagram of TRGMII.

4.4 Register Definition

Module name: TRGMII_REG Base address: (+1b110000h)

Address	Name	Width	Register Function
1b110300	TRGMII_RCK_CTRL	32	TRGMII RXC CONTROL REGISTER

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Address	Name	Width	Register Function
1b110304	TRGMII_RCK_RTT	32	TRGMII RXC ODT REGISTER
1b110310	TRGMII_RD0	32	TRGMII RD0 CONTROL REGISTER
1b110314	TRGMII_RD0_RTT	32	TRGMII RD0 RTT REGISTER
1b110318	TRGMII_RD1	32	TRGMII RD1 CONTROL REGISTER
1b11031c	TRGMII_RD1_RTT	32	TRGMII RD1 RTT REGISTER
1b110320	TRGMII_RD2	32	TRGMII RD2 CONTROL REGISTER
1b110324	TRGMII_RD2_RTT	32	TRGMII RD2 RTT REGISTER
1b110328	TRGMII_RD3	32	TRGMII RD3 CONTROL REGISTER
1b11032c	TRGMII_RD3_RTT	32	TRGMII RD3 RTT REGISTER
1b110330	TRGMII_RXCTL	32	TRGMII RXCTL CONTROL REGISTER
1b110334	TRGMII_RXCTL_RTT	32	TRGMII RXCTL RTT REGISTER
1b110340	TRGMII_TXCTRL	32	TRGMII TX CONTROL REGISTER
1b110350	TRGMII_TD0_CTRL	32	TRGMII TD0 CTRL REGISTER
1b110354	TRGMII_TD0_ODT	32	TRGMII TD0 ODT REGISTER
1b110358	TRGMII_TD1_CTRL	32	TRGMII TD1 CTRL REGISTER
1b11035c	TRGMII_TD1_ODT	32	TRGMII TD1 ODT REGISTER
1b110360	TRGMII_TD2_CTRL	32	TRGMII TD2 CTRL REGISTER
1b110364	TRGMII_TD2_ODT	32	TRGMII TD2 ODT REGISTER
1b110368	TRGMII_TD3_CTRL	32	TRGMII TD3 CTRL REGISTER
1b11036c	TRGMII_TD3_ODT	32	TRGMII TD3 ODT REGISTER
1b110370	TRGMII_TXCTL_CTRL	32	TRGMII TXCTL CTRL REGISTER
1b110374	TRGMII_TXCTL_ODT	32	TRGMII TXCTL ODT REGISTER
1b110378	TRGMII_TCK_CTRL	32	TRGMII TCK CTRL REGISTER
1b11037c	TRGMII_TCK_ODT	32	TRGMII TCK ODT REGISTER
1b110380	MCM_IOTEST	32	MCM IO TEST
1b110384	Loopback test	32	LOOPBACK TEST
1b110390	INTF_MODE	32	Interface Mode Register
1b110600	DEBUG_PROBE_SEL	32	Probe select
1b110610	DEBUG	32	DEBUG

1B110300 TRGMII_RCK_CTRL TRGMII RXC CONTROL REGISTER 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_RST	RXC_DQSISEL		BSLIP_SHIFT_RXDV	BSLIP_SHIFT_RXD									RXCTL_DMWTLAT		

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Type	RW	RW		RW	RW									RW		
Reset	0	0		0	0	0	0	0						0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQSI1_TAP								DQSI0_TAP						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_RST	**Reset of RX.** 0: reset is released. 1: reset is asserted.
30	RXC_DQSISEL	**DQS selection for receiving RXD and RXDV.** 0: DQS0 1: DQS1
28	BSLIP_SHIFT_RXDV	**Edge selection for receiving LSB.** 0: LSB is received at rising edge. 1: LSB is received at falling edge.
27:24	BSLIP_SHIFT_RXD	**Edge selection for receiving LSB.** 0: LSB is received at rising edge. 1: LSB is received at falling edge.
18:16	RXCTL_DMWTLAT	**RX Latency Adjustment**
14:8	DQSI1_TAP	**This is the delay tap of DQSI1. To modify the delay tap, it should be increased or decreased by 1.**
6:0	DQSI0_TAP	**This is the delay tap of DQSI0. To modify the delay tap, it should be increased or decreased by 1.**

1B110304 TRGMII_RCK_RTT TRGMII RXC ODT REGISTER C0000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS1_GATE	DQS0_GATE	RCK_RDSEL						RCK_EXIST			RCK_RTTBN	RCK_RTTBPJ	RCK_RTT		
Type	RW	RW	RW						RO			RW	RW	RW		
Reset	1	1	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam		RCK_ODTN				RCK_ODT			RCK_DRVN				RCK_DRVP			

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e						**P**										
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DQS1_GATE	**Clock gating of DQS1.** 0: DQS1 is disabled. 1: DQS1 is enabled.
30	DQS0_GATE	**Clock gating of DQS0.** 0: DQS0 is disabled. 1: DQS0 is enabled.
29:24	RCK_RDSEL	**RX duty select**
23	RCK_EXIST	**Clock detection of RXCLK.** 0: RXCLK is not existed. 1: RXCLK is existed.
20	RCK_RTTBN	**Termination Pull-down Base Resistor (Base NMOS) OFF control. (Reserved)**
19	RCK_RTTBPJ	**Termination Pull-up Base Resistor (Base PMOS) OFF control. (Reserved)**
18:16	RCK_RTT	**On-Die-Termination.** 000: disabled.
14:12	RCK_ODTN	**programmable termination control for linear pull-down resistor.**
10:8	RCK_ODTP	**programmable termination control for linear pull-up resistor.**
7:4	RCK_DRVN	**Pull-Down Driving Strength Control.**
3:0	RCK_DRVP	**Pull-Up Driving Strength Control.**

1B110310 TRGMII_RD0 TRGMII RD0 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BSLIP_EN**	**EDGE_CHK**		**EDGE_CHK_PAT**	**BSLIP_INIT**				**RD0_WD**							
Type	RW	RW		RW	RW				RO							

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Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD0_ERRCNT					RD0_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To triger a bitslip operation, this bit should be written as 1. This bit is toggled when written as 1.** 1: bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks. The comparison error was stored in ERRCNT. This bit is toggled when written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: training pattern is toggling pattern. 1: training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.**
23:16	RD0_WD	**This register holds the received word for RD0.**
11:8	RD0_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received is compared to the data received at previous clock. This register holds the mismatch counter of RD0.**
6:0	RD0_TAP	**This is the delay tap of RD0. To modify the delay tap, it should be increased or decreased by 1.**

1B110314 TRGMII_RD0_RTT TRGMII RD0 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD0_DMPEDRV		RD0_DM_RDSEL						RD0_DMERODT	RD0_DMOECTL	RD0_ODTEN	RD0_DM_RTTBPJ	RD0_DM_RTTBNJ	RD0_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RD0_DM_SR	RD0_DM_ODTN				RD0_DM_ODTP			RD0_DM_DRVN				RD0_DM_DRVP			
Type	RW	RW				RW			RW				RW			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD0_DMPEDRV	
29:24	RD0_DM_RDSEL	**RX duty select**
23	RD0_DMERODT	**This is the ODT setting.**
22	RD0_DMOECTL	**OE edge select**
21	RD0_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD0_DM_RTTBPJ	**This is the RTT setting.**
19	RD0_DM_RTTBNJ	**This is the RTT setting.**
18:16	RD0_DM_RTT	**This is the RTT setting.**
15	RD0_DM_SR	
14:12	RD0_DM_ODTN	**programmable termination control for linear pull-down resistor**
10:8	RD0_DM_ODTP	**programmable termination control for linear pull-up resistor**
7:4	RD0_DM_DRVN	**Pull-Down Driving Strength Control.**
3:0	RD0_DM_DRVP	**Pull-Up Driving Strength Control.**

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1B110318 TRGMII_RD1 TRGMII RD1 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD1_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD1_ERRCNT					RD1_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To triger a bitslip operation, this bit should be written as 1. This bit is toggled when written as 1.** 1: bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks. The comparison error was stored in ERRCNT. This bit is toggled when written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: training pattern is toggling pattern. 1: training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.**
23:16	RD1_WD	**This register holds the received word for RD1.**
11:8	RD1_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received is compared to the data received at previous clock. This register holds the mismatch counter of RD1.**
6:0	RD1_TAP	**This is the delay tap of RD1. To modify the delay tap, it should be increased or decreased by 1.**

1B11031C TRGMII_RD1_RTT TRGMII RD1 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD1_DMPE		RD1_DM_RDSEL						RD1_DMER	RD1_DMOE	RD1_ODTEN	RD1_DM_R	RD1_DM_R	RD1_DM_RTT		

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	DRV								ODT	CTL		TTBPJ	TTBNJ			
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD1_DM_SR	RD1_DM_ODTN				RD1_DM_ODTP			RD1_DM_DRVN				RD1_DM_DRVP			
Type	RW	RW				RW			RW				RW			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD1_DMPEDRV	
29:24	RD1_DM_RDSEL	**RX duty select**
23	RD1_DMERODT	**This is the ODT setting.**
22	RD1_DMOECTL	**OE edge select**
21	RD1_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD1_DM_RTTBPJ	**This is the RTT setting.**
19	RD1_DM_RTTBNJ	**This is the RTT setting.**
18:16	RD1_DM_RTT	**This is the RTT setting.**
15	RD1_DM_SR	
14:12	RD1_DM_ODTN	**programmable termination control for linear pull-down resistor**
10:8	RD1_DM_ODTP	**programmable termination control for linear pull-up resistor**
7:4	RD1_DM_DRVN	**Pull-Down Driving Strength Control.**

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Bit(s)	Name	Description
3:0	RD1_DM_DRVP	**Pull-Up Driving Strength Control.**

1B110320 TRGMII_RD2 TRGMII RD2 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD2_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD2_ERRCNT					RD2_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To triger a bitslip operation, this bit should be written as 1. This bit is toggled when written as 1.** 1: bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks. The comparison error was stored in ERRCNT. This bit is toggled when written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: training pattern is toggling pattern. 1: training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.**
23:16	RD2_WD	**This register holds the received word for RD2.**
11:8	RD2_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received is compared to the data received at previous clock. This register holds the mismatch counter of RD2.**
6:0	RD2_TAP	**This is the delay tap of RD2. To modify the delay tap, it should be increased or decreased by 1.**

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1B110324 TRGMII_RD2_RTT TRGMII RD2 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD2_DMPEDRV		RD2_DM_RDSEL						RD2_DMERODT	RD2_DMOECTL	RD2_ODTEN	RD2_DM_RTTBPJ	RD2_DM_RTTBNJ	RD2_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD2_DM_SR	RD2_DM_ODTN				RD2_DM_ODTP			RD2_DM_DRVN				RD2_DM_DRVP			
Type	RW	RW				RW			RW				RW			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD2_DMPEDRV	
29:24	RD2_DM_RDSEL	**RX duty select**
23	RD2_DMERODT	**This is the ODT setting.**
22	RD2_DMOECTL	**OE edge select**
21	RD2_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD2_DM_RTTBPJ	**This is the RTT setting.**
19	RD2_DM_RTTBNJ	**This is the RTT setting.**
18:16	RD2_DM_RTT	**This is the RTT setting.**
15	RD2_DM_SR	
14:12	RD2_DM_ODTN	**programmable termination control for linear pull-down resistor**

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Bit(s)	Name	Description
10:8	RD2_DM_ODTP	**programmable termination control for linear pull-up resistor**
7:4	RD2_DM_DRVN	**Pull-Down Driving Strength Control.**
3:0	RD2_DM_DRVP	**Pull-Up Driving Strength Control.**

1B110328 TRGMII_RD3 TRGMII RD3 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD3_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD3_ERRCNT					RD3_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To triger a bitslip operation, this bit should be written as 1. This bit is toggled when written as 1.** 1: bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks. The comparison error was stored in ERRCNT. This bit is toggled when written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: training pattern is toggling pattern. 1: training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.**
23:16	RD3_WD	**This register holds the received word for RD3.**
11:8	RD3_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received is compared to the data received at previous clock. This register holds the mismatch counter of RD3.**

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Bit(s)	Name	Description
6:0	RD3_TAP	**This is the delay tap of RD3. To modify the delay tap, it should be increased or decreased by 1.**

1B11032C TRGMII_RD3_RTT TRGMII RD3 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD3_DMPEDRV		RD3_DM_RDSEL						RD3_DMERODT	RD3_DMOECTL	RD3_ODTEN	RD3_DM_RTTBPJ	RD3_DM_RTTBNJ	RD3_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD3_DM_SR	RD3_DM_ODTN				RD3_DM_ODTP			RD3_DM_DRVN				RD3_DM_DRVP			
Type	RW	RW				RW			RW				RW			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD3_DMPEDRV	
29:24	RD3_DM_RDSEL	**RX duty select**
23	RD3_DMERODT	**This is the ODT setting.**
22	RD3_DMOECTL	**OE edge select**
21	RD3_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD3_DM_RTTBPJ	**This is the RTT setting.**
19	RD3_DM_RTTBNJ	**This is the RTT setting.**

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Bit(s)	Name	Description
18:16	RD3_DM_RTT	**This is the RTT setting.**
15	RD3_DM_SR	
14:12	RD3_DM_ODTN	**programmable termination control for linear pull-down resistor**
10:8	RD3_DM_ODTP	**programmable termination control for linear pull-up resistor**
7:4	RD3_DM_DRVN	**Pull-Down Driving Strength Control.**
3:0	RD3_DM_DRVP	**Pull-Up Driving Strength Control.**

1B110330 TRGMII_RXCTL TRGMII RXCTL CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RXCTL_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RXCTL_ERRCNT					RXCTL_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To triger a bitslip operation, this bit should be written as 1. This bit is toggled when written as 1.** 1: bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks. The comparison error was stored in ERRCNT. This bit is toggled when written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: training pattern is toggling pattern. 1: training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is**

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Bit(s)	Name	Description
		enabled. The suggested value is 15, 0, or 1.
23:16	RXCTL_WD	**This register holds the received word for RXCTL.**
11:8	RXCTL_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received is compared to the data received at previous clock. This register holds the mismatch counter of RXCTL.**
6:0	RXCTL_TAP	**This is the delay tap of RXCTL. To modify the delay tap, it should be increased or decreased by 1.**

1B110334 TRGMII_RXCTL_RTT TRGMII RXCTL RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RXCTL_DMPEDRV		RXCTL_DM_RDSEL						RXCTL_DMERODT	RXCTL_DMOECTL	RXCTL_ODTEN	RXCTL_DM_RTTBPJ	RXCTL_DM_RTTBNJ	RXCTL_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXCTL_DM_SR	RXCTL_DM_ODTN				RXCTL_DM_ODTP			RXCTL_DM_DRVN				RXCTL_DM_DRVP			
Type	RW	RW				RW			RW				RW			
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RXCTL_DMPEDRV	
29:24	RXCTL_DM_RDSEL	**RX duty select**
23	RXCTL_DMERODT	**This is the ODT setting.**
22	RXCTL_DMOECTL	**OE edge select**

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Bit(s)	Name	Description
21	RXCTL_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RXCTL_DM_RTTBPJ	**This is the RTT setting.**
19	RXCTL_DM_RTTBNJ	**This is the RTT setting.**
18:16	RXCTL_DM_RTT	**This is the RTT setting.**
15	RXCTL_DM_SR	
14:12	RXCTL_DM_ODTN	**programmable termination control for linear pull-down resistor**
10:8	RXCTL_DM_ODTP	**programmable termination control for linear pull-up resistor**
7:4	RXCTL_DM_DRVN	**Pull-Down Driving Strength Control.**
3:0	RXCTL_DM_DRVP	**Pull-Up Driving Strength Control.**

1B110340 TRGMII_TXCTRL TRGMII TX CONTROL REGISTER 40020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRAIN_TXEN	TXC_INV	TX_DOEO	TX_RST										TX_DMWTLAT		
Type	RW	RW	RW	RW										RW		
Reset	0	1	0	0										0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

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Bit(s)	Name	Description
31	TRAIN_TXEN	**In training mode, training pattern are transmitted.** 0: training pattern is disabled. 1: training is enabled.
30	TXC_INV	**TXC can be generated in normal phase or inverted phase.** 0: TXC is not inverted. 1: TXC is inverted.
29	TX_DOEO	**TX can be disabled for test purpose.** 0: TX is transmitted. 1: TX is disabled.
28	TX_RST	**Reset of TX.** 0: reset is released. 1: reset is asserted.
18:16	TX_DMWTLAT	**TX Latency Adjustment**

1B110350 TRGMII_TD0_CTRL TRGMII TD0 CTRL REGISTER 00000055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD0_DM_SR	TD0_DMERODT	TD0_DMOECTL		TD0_TAP				TD0_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TD0_DMPEDRV	
15	TD0_DM_SR	

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Bit(s)	Name	Description
14	TD0_DMERODT	**This is the ODT setting.**
13	TD0_DMOECTL	**OE edge select**
11:8	TD0_TAP	**This is the delay tap of TD0. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD0_TRAIN_WD	**This is the training word in training mode.**

1B110354 TRGMII_TD0_ODT TRGMII TD0 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DM_DRVN_PRE		TD0_DM_DRVP_PRE		TD0_DM_TDSEL				TD0_ODTEN			TD0_DME_PRE	TD0_DM_DRVNT0	TD0_DM_DRVPT0	TD0_DM_DRVNTE	TD0_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD0_DM_ODTN				TD0_DM_ODTP			TD0_DM_DRVN				TD0_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD0_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD0_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD0_DM_TDSEL	
23	TD0_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TD0_DME_PRE	**This is the pre-emphasis setting.**

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Bit(s)	Name	Description
19	TD0_DM_DRVNT0	
18	TD0_DM_DRVPT0	
17	TD0_DM_DRVNTE	
16	TD0_DM_DRVPTE	
14:12	TD0_DM_ODTN	**This is the ODT setting.**
10:8	TD0_DM_ODTP	**This is the ODT setting.**
7:4	TD0_DM_DRVN	**This is the driving current.**
3:0	TD0_DM_DRVP	**This is the driving current.**

1B110358 TRGMII_TD1_CTRL TRGMII TD1 CTRL REGISTER 00000055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD1_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD1_DM_SR	TD1_DMERODT	TD1_DMOECTL		TD1_TAP				TD1_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TD1_DMPEDRV	

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Bit(s)	Name	Description
15	TD1_DM_SR	
14	TD1_DMERODT	**This is the ODT setting.**
13	TD1_DMOECTL	**OE edge select**
11:8	TD1_TAP	**This is the delay tap of TD1. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD1_TRAIN_WD	**This is the training word in training mode.**

1B11035C TRGMII_TD1_ODT TRGMII TD1 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD1_DM_DRVN_PRE		TD1_DM_DRVP_PRE		TD1_DM_TDSEL				TD1_ODTEN			TD1_DME_PRE	TD1_DM_DRVNTo	TD1_DM_DRVPTo	TD1_DM_DRVNTE	TD1_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD1_DM_ODTN				TD1_DM_ODTP			TD1_DM_DRVN				TD1_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD1_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD1_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD1_DM_TDSEL	
23	TD1_ODTEN	0: ODT is disabled. 1: ODT is enabled.

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Bit(s)	Name	Description
20	TD1_DME_PRE	**This is the pre-emphasis setting.**
19	TD1_DM_DRVNT0	
18	TD1_DM_DRVPT0	
17	TD1_DM_DRVNTE	
16	TD1_DM_DRVPTE	
14:12	TD1_DM_ODTN	**This is the ODT setting.**
10:8	TD1_DM_ODTP	**This is the ODT setting.**
7:4	TD1_DM_DRVN	**This is the driving current.**
3:0	TD1_DM_DRVP	**This is the driving current.**

1B110360 TRGMII_TD2_CTRL TRGMII TD2 CTRL REGISTER 00000055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD2_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD2_DM_SR	TD2_DMERODT	TD2_DMOECTL		TD2_TAP				TD2_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
31	TD2_DMPEDRV	
15	TD2_DM_SR	
14	TD2_DMERODT	**This is the ODT setting.**
13	TD2_DMOECTL	**OE edge select**
11:8	TD2_TAP	**This is the delay tap of TD2. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD2_TRAIN_WD	**This is the training word in training mode.**

1B110364 TRGMII_TD2_ODT TRGMII TD2 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD2_DM_DRVN_PRE		TD2_DM_DRVP_PRE		TD2_DM_TDSEL				TD2_ODTEN			TD2_DME_PRE	TD2_DM_DRVNTo	TD2_DM_DRVPTo	TD2_DM_DRVNTE	TD2_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD2_DM_ODTN				TD2_DM_ODTP			TD2_DM_DRVN				TD2_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD2_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD2_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD2_DM_TDSEL	
23	TD2_ODTEN	

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Bit(s)	Name	Description
		0: ODT is disabled. 1: ODT is enabled.
20	TD2_DME_PRE	**This is the pre-emphasis setting.**
19	TD2_DM_DRVNT0	
18	TD2_DM_DRVPT0	
17	TD2_DM_DRVNTE	
16	TD2_DM_DRVPTE	
14:12	TD2_DM_ODTN	**This is the ODT setting.**
10:8	TD2_DM_ODTP	**This is the ODT setting.**
7:4	TD2_DM_DRVN	**This is the driving current.**
3:0	TD2_DM_DRVP	**This is the driving current.**

1B110368 TRGMII_TD3_CTRL TRGMII TD3 CTRL REGISTER 00000055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD3_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD3_DM_SR	TD3_DMERODT	TD3_DMOECTL		TD3_TAP				TD3_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

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Bit(s)	Name	Description
31	TD3_DMPEDRV	
15	TD3_DM_SR	
14	TD3_DMERODT	**This is the ODT setting.**
13	TD3_DMOECTL	**OE edge select**
11:8	TD3_TAP	**This is the delay tap of TD3. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD3_TRAIN_WD	**This is the training word in training mode.**

1B11036C TRGMII_TD3_ODT TRGMII TD3 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD3_DM_DRVN_PRE		TD3_DM_DRVP_PRE		TD3_DM_TDSEL				TD3_ODTEN			TD3_DME_PRE	TD3_DM_DRVNTo	TD3_DM_DRVPTo	TD3_DM_DRVNTE	TD3_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD3_DM_ODTN				TD3_DM_ODTP			TD3_DM_DRVN				TD3_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD3_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD3_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD3_DM_TDSEL	
23	TD3_ODTEN	

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Bit(s)	Name	Description
		0: ODT is disabled. 1: ODT is enabled.
20	TD3_DME_PRE	**This is the pre-emphasis setting.**
19	TD3_DM_DRVNT0	
18	TD3_DM_DRVPT0	
17	TD3_DM_DRVNTE	
16	TD3_DM_DRVPTE	
14:12	TD3_DM_ODTN	**This is the ODT setting.**
10:8	TD3_DM_ODTP	**This is the ODT setting.**
7:4	TD3_DM_DRVN	**This is the driving current.**
3:0	TD3_DM_DRVP	**This is the driving current.**

1B110370 TRGMII_TXCTL_CTRL TRGMII TXCTL CTRL REGISTER 00000055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXCTL_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXCTL_DM_SR	TXCTL_DMERODT	TXCTL_DMOECTL		TXCTL_TAP				TXCTL_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

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Bit(s)	Name	Description
31	TXCTL_DMPEDRV	
15	TXCTL_DM_SR	
14	TXCTL_DMERODT	**This is the ODT setting.**
13	TXCTL_DMOECTL	**OE edge select**
11:8	TXCTL_TAP	**This is the delay tap of TXCTL. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TXCTL_TRAIN_WD	**This is the training word in training mode.**

1B110374 TRGMII_TXCTL_ODT TRGMII TXCTL ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXCTL_DM_DRVN_PRE		TXCTL_DM_DRVP_PRE		TXCTL_DM_TDSEL				TXCTL_ODTEN			TXCTL_DME_PRE	TXCTL_DM_DRVNTo	TXCTL_DM_DRVPTo	TXCTL_DM_DRVNTE	TXCTL_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TXCTL_DM_ODTN				TXCTL_DM_ODTP			TXCTL_DM_DRVN				TXCTL_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TXCTL_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TXCTL_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TXCTL_DM_TDSEL	

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Bit(s)	Name	Description
23	TXCTL_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TXCTL_DME_PRE	**This is the pre-emphasis setting.**
19	TXCTL_DM_DRVNT0	
18	TXCTL_DM_DRVPT0	
17	TXCTL_DM_DRVNTE	
16	TXCTL_DM_DRVPTE	
14:12	TXCTL_DM_ODTN	**This is the ODT setting.**
10:8	TXCTL_DM_ODTP	**This is the ODT setting.**
7:4	TXCTL_DM_DRVN	**This is the driving current.**
3:0	TXCTL_DM_DRVP	**This is the driving current.**

1B110378 TRGMII_TCK_CTRL TRGMII TCK CTRL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCK_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TCK_DM_SR	TCK_DMERODT	TCK_DMOECTL		TCK_TAP											
Type	RW	RW	RW		RW											

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Reset	0	0	0		0	0	0	0								

Bit(s)	Name	Description
31	TCK_DMPEDRV	
15	TCK_DM_SR	
14	TCK_DMERODT	**This is the ODT setting.**
13	TCK_DMOECTL	**OE edge select**
11:8	TCK_TAP	**This is the delay tap of TCK. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**

1B11037C TRGMII_TCK_ODT TRGMII TCK ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCK_DM_DRVN_PRE		TCK_DM_DRVP_PRE		TCK_DM_TDSEL				TCK_ODTEN			TCK_DME_PRE	TCK_DM_DRVNTo	TCK_DM_DRVPTo	TCK_DM_DRVNTE	TCK_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TCK_DM_ODTN				TCK_DM_ODTP			TCK_DM_DRVN				TCK_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TCK_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TCK_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TCK_DM_TDSEL	
23	TCK_ODTEN	

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Bit(s)	Name	Description
		0: ODT is disabled. 1: ODT is enabled.
20	TCK_DME_PRE	**This is the pre-emphasis setting.**
19	TCK_DM_DRVNT0	
18	TCK_DM_DRVPT0	
17	TCK_DM_DRVNTE	
16	TCK_DM_DRVPTE	
14:12	TCK_DM_ODTN	**This is the ODT setting.**
10:8	TCK_DM_ODTP	**This is the ODT setting.**
7:4	TCK_DM_DRVN	**This is the driving current.**
3:0	TCK_DM_DRVP	**This is the driving current.**

1B110380 MCM_IOTEST MCM IO TEST 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PAD	
Type															RW	
Reset															0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MCM_IOTEST_RX						TRGMII_MCM_IOTEST		MCM_IOTEST_TX					
Type			RO						RW		RW					
Reset			0	0	0	0	0	0	0		0	0	0	0	0	0

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Bit(s)	Name	Description
17:16	PAD	Bit 16 0 : 1.5 V for PAD 1: 1.8 V for PAD Bit 17 1: Enable Loopback test
13:8	MCM_IOTEST_RX	**MCM IO TEST RX**
7	TRGMII_MCM_IOTEST	**MCM TRGMII IO TEST enable**
5:0	MCM_IOTEST_TX	**MCM IO TEST TX**

1B110384 Loopback test LOOPBACK TEST 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											LOOPBACK_RESULT					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	LOOPBACK_RESULT	**LOOPBACK_RESULT**

1B110390 INTF_MODE Interface Mode Register 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														csr_trgmii_mode		csr_

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																trgmii_intf_dis
Type														RW		RW
Reset														0	1	0

Bit(s)	Name	Description
2:1	csr_trgmii_mode	**bit [0] 0 : RGMII mode** 1 : TRGMII mode bit [1] : 0 : edge align 1 : shift 90 degree (centeral align)
0	csr_trgmii_intf_dis	**TRGMII Interface Disable** 1'b1: Disable 1'b0 : Enable

1B110600 DEBUG_PROBE_SEL Probe select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												csr_trgmii_probe_sel				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	csr_trgmii_probe_sel	

1B110610 DEBUG DEBUG 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**csr_trgmii_probe_grp**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	csr_trgmii_probe_grp	

4.5 *Calibration Flow*

4.5.1 Scenario

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4.5.2 FE Rx (Giga Switch to FE)

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Step No.	Procedure	Related CR operation	Note
1	RX clock gating	fb110304[31:30] =2'b00	
2	Assert RX RST	fb110300[31] =1'b1	
3	Set TX OE edge	fb110378[13]=1'b1	
4	Disable Clock Gating	fb110304[31:30] =2'b11	
5	Release RX RST	fb110300[31] =1'b0	
6	Set bslip_en	fb110310 [31] =1 fb110318 [31] =1 fb110320 [31] =1 fb110328 [31] =1 fb110330 [31] =1	
7	Enable TX Training Mode	0x7a40[31] = 1'b1	Set Switch
8	Enable EDGE CHECK	fb110310 [30] =1 fb110318 [30] =1 fb110320 [30] =1 fb110328 [30] = 1 fb110330 [30] =1	
9	RX clock gating	fb110304[31:30] =2'b00	
10	RXC Delay Adjust	incremental delay and set fb110300[15:0]	
11	Disable Clock Gating	fb110304[31:30] =2'b11	
12	Set bslip_en	fb110310 [31] =1 fb110318 [31] =1 fb110320 [31] =1 fb110328 [31] =1 fb110330 [31] =1	
13	Disable EDGE CHECK	fb110310 [30] =0 fb110318 [30] =0 fb110320 [30] =0 fb110328 [30] = 0 fb110330 [30] =0	
14	Check ERRFLAG	read fb110310 [23:8] read fb110318 [23:8] read fb110320 [23:8] read fb110328 [23:8] read fb110330 [23:8]	
15	Enable EDGE CHECK	fb110310 [30] =1 fb110318 [30] =1 fb110320 [30] =1 fb110328 [30] = 1 fb110330 [30] =1	
16	RXD Delay Adjustment		incremental delay
17	Disable EDGE CHECK	fb110310 [30] =0 fb110318 [30] =0 fb110320 [30] =0 fb110328 [30] = 0 fb110330 [30] =0	
18	Check ERRFLAG	read fb110310 [23:8] read fb110318 [23:8] read fb110320 [23:8] read fb110328 [23:8] read fb110330 [23:8]	
19	Record min. Delay Tap (A)	write fb110310 [6:0] write fb110318 [6:0] wtite fb110320 [6:0] write fb110328 [6:0] write fb110330 [6:0]	Record min. Delay Tap
20	Enable EDGE CHECK	fb110310 [30] =1 fb110318 [30] =1 fb110320 [30] =1 fb110328 [30] = 1 fb110330 [30] =1	
21	RXD Delay Adjustment		incremental delay
22	Disable EDGE CHECK	fb110310 [30] =0	

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		fb110318 [30] =0 fb110320 [30] =0 fb110328 [30] = 0 fb110330 [30] =0	
23	Check ERRFLAG	read fb110310 [23:8] read fb110318 [23:8] read fb110320 [23:8] read fb110328 [23:8] read fb110330 [23:8]	
24	Record max. Delay Tap (B)		Record max. Delay Tap
25	Calculate RXD delay and store to register	write fb110310 [6:0] write fb110318 [6:0] wtite fb110320 [6:0] write fb110328 [6:0] write fb110330 [6:0]	Calculate final delay (A+B)/2
26	Enable TX Training Mode	0x7a40[31] = 1'b1	Set Switch

4.5.3 Giga Switch Rx (FE to Giga Switch)

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Step No.	Procedure	Setting	Note
1	RX clock gating	0x7a04[31:30] =2'b00	
2	Set TX OE edge	0x7a78[13]=1'b1	
3	Assert RX RST	0x7a00[31] =1'b1	
4	Release RX RST	0x7a00[31] =1'b0	
5	Disable Clock Gating	0x7a04[31:30] =2'b11	
7	Set FE TX delay	0xfb110378[11:8] = 4	Set FE
8	Enable TX Training Mode	0xfb110340[31] = 1'b1	Set FE
9	Enable EDGE CHECK	0x7a10 [30] =1 0x7a18[30] =1 0x7a20 [30] =1 0x7a28 [30] =1 0x7a30 [30] =1	
10	Disable EDGE CHECK	0x7a10 [30] =0 0x7a18[30] =0 0x7a20 [30] =0 0x7a28 [30] =0 0x7a30 [30] =0	
11	RX clock gating	0x7a04[31:30] =2'b00	
12	Assert RX RST	0x7a00[31] =1'b1	
13	RXC Delay Adjust	incremental delay and set 0x7a00[6:0]	
14	Release RX RST	0x7a00[31] =1'b0	
15	Disable Clock Gating	0x7a04[31:30] =2'b11	
16	Check ERRFLAG	read 0x7a10 [23:8] read 0x7a18[23:8] read 0x7a20 [23:8] read 0x7a28 [23:8] read 0x7a30 [23:8]	
17	Enable EDGE CHECK	0x7a10 [30] =1 0x7a18[30] =1 0x7a20 [30] =1 0x7a28 [30] =1 0x7a30 [30] =1	
18	RXD Delay Adjustment		Incremental delay
19	Disable EDGE CHECK	0x7a10 [30] =0	

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		0x7a18[30] =0 0x7a20 [30] =0 0x7a28 [30] =0 0x7a30 [30] =0	
20	Check ERRFLAG	read 0x7a10 [23:8] read 0x7a18[23:8] read 0x7a20 [23:8] read 0x7a28 [23:8] read 0x7a30 [23:8]	
21	Record min. Delay Tap (A)	write 0x7a10 [6:0] write 0x7a18[6:0] write 0x7a20 [6:0] write 0x7a28 [6:0] write 0x7a30 [6:0]	Record min. Delay Tap
22	Enable EDGE CHECK	0x7a10 [30] =1 0x7a18[30] =1 0x7a20 [30] =1 0x7a28 [30] =1 0x7a30 [30] =1	
23	RXD Delay Adjustment		Incremental delay
24	Disable EDGE CHECK	0x7a10 [30] =0 0x7a18[30] =0 0x7a20 [30] =0 0x7a28 [30] =0 0x7a30 [30] =0	
25	Check ERRFLAG	read 0x7a10 [23:8] read 0x7a18[23:8] read 0x7a20 [23:8] read 0x7a28 [23:8] read 0x7a30 [23:8]	
26	Record max. Delay Tap (B)		Record max. Delay Tap
27	Calculate RXD delay and store to register	write 0x7a10 [6:0] write 0x7a18[6:0] write 0x7a20 [6:0] write 0x7a28 [6:0] write 0x7a30 [6:0]	Calculate final delay (A+B)/2
28	Enable TX Training Mode	0xfb110340[31] = 1'b1	Set FE

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5 Giga Switch

5.1 *Introduction*

The GSW is a highly integrated Ethernet switch with high performance and non-blocking transmission. It includes a 7-port Gigabit Ethernet MAC and a 5-port Gigabit Ethernet PHY for several applications, such as xDSL, xPON, WiFi AP, and cable modem. GSW enables an advanced power-saving feature to meet the market requirement. It complies with IEEE803.3az for Energy Efficient Ethernet and cable-length/link-down power saving mode. GSW is also designed for cost-sensitive applications in retail and Telecom market. MediaTek's industry-leading techniques provide customers with the most cost-competitive and lowest power consumption Ethernet product in the industry. Please refer to the below figure to know the construct of GSW.

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5.2 Function Description

5.2.1 Mode setting

The register 0x7800 is hardware trap, it is made when power on (define by boot-strap resistance). You can change it by writing 0x7804. Finally, the system would active according ox7804 not 0x7800. Some registers of 0x7800 cannot be changed. For detail, please check the switch register map. You should check it bit by bit.

00007800 HWTRAP Hardware Trap Status Register 01007FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ht_loopdet_dis	ht_p5_intf_sel	ht_smi_addr		ht_xtal_fsel		ht_p6_intf_dis	ht_p5_intf_mode	ht_p5_intf_dis	ht_c_mdio_bps_n	ht_eeprom_en	ht_chip_mode			
Type		RO	RO	RO		RO		RO	RO	RO	RO	RO	RO			
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

If you want to change 0x7804, you need to set bit 16 as 1 of 0x7804 first.

00007804 MHWTRAP Modified Hardware Trap Status Register 0100000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												csr_p5_phy0_sel				csr_chg_trap
Type												RW				RW
Reset												0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_gsw_ck_sel	csr_loopdet_dis	csr_p5_intf_sel	csr_smi_addr		csr_xtal_fsel		csr_p6_intf_dis	csr_p5_intf_mode	csr_p5_intf_dis	csr_c_mdio_bps_n	csr_eeprom_en	csr_chip_mode			
Type	RW	RW	RW	RO		RO		RW	RW	RW	RW	RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
20	csr_p5_phy0_sel	**When p5_intf_sel == 1'b0, the external device will be connected to** 1'b0: GPHY4 1'b1: GPHY0
16	csr_chg_trap	**Change HW-TRAP setting** 1'b1: Change 1'b0: Use default HW-TRAP setting
15	csr_gsw_ck_sel	**Control GSW_CK (if csr_chg_trap == 1)** 1'b0: 500MHz 1'b1: 200MHz
14	csr_loopdet_dis	**Hardware Loop Detection Disable (if csr_chg_trap == 1)** 1'b0: Enable 1'b1: Disable
13	csr_p5_intf_sel	**Port 5 Interface Selection (if csr_chg_trap == 1)** 1'b1: P5 Interface connects to GMAC5 1'b0: P5 Interface connects to GePHY4 or GePHY0 (depends on csr_p5_phy0_sel)
12:11	csr_smi_addr	**csr_smi_addr is equal to ht_smi_addr[1:0] (offset: 0x7800, bit 12~11) since this hardware trap cannot be modified by software.**

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10:9	csr_xtal_fsel	**csr_xtal_fsel is equal to ht_xtal_fsel[1:0](offset: 0x7800, bit 10~9)since this hardware trap cannot be modified by software.**
8	csr_p6_intf_dis	**From hw_trap[8]** Port 6 Interface Disable (if csr_chg_trap == 1) 1'b0: Enable 1'b1: Disable
7	csr_p5_intf_mode	**Port 5 Interface Mode (if csr_chg_trap == 1)** 1'b0: GMII/MII 1'b1: RGMII
6	csr_p5_intf_dis	**Port 5 Interface Disable (if csr_chg_trap == 1)** 1'b1: Disable 1'b0: Enable
5	csr_c_mdio_bps_n	**Directly access phy mdc (if csr_chg_trap==1)** 0: Directly access PHY registers via C_MDC/C_MDIO 1: Indirectly access PHY registers
4	csr_eeprom_en	**csr_eeprom_en is equal to ht_eeprom_en (offset: 0x7800, bit 4) since this hardware trap cannot be modified by software.**
3:0	csr_chip_mode	**csr_chip_mode is equal to ht_chip_mode[3:0] (offset: 0x7800, bit 3~0) since this hardware trap cannot be modified by software.**

5.2.2 *Reset*

Check the Register 0x7000 if you want to do the software reset to switch or PHY.
Usually, we would set 0x7000 as 0x3 for re-start switch.

00007000 SYS_CTRL System Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ACL_TAB_INIT	MAC_TAB_INIT	VLAN_TAB_INIT				BMU_MEM_INIT
Type										RO	RO	RO				RO
Reset										0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRTCM_BIST_STS	MASK_BIST_STS	CTRL_BIST_STS	ADDR_BIST_STS	VLN_BIST_STS	MIB_BIST_STS	PB_BIST_STS	PL_BIST_STS	FL_BIST_STS	MBIST_CMP	MBIST_EN		SW_PHY_RST	SW_SYS_RST	SW_REG_RST
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW		R/W/SC	R/W/SC	R/W/SC
Reset		0	0	0	0	0	0	0	0	0	0	0		0	0	0

5.2.3 *Access control list (ACL)*

ACL Rule table is implemented along with packet parser. For the incoming packet, 2-bytes packet content will be filtered sequentially and compared with 64 patterns in the ACL rule table. When one pattern is hit, the corresponding rule flag will be set. After the whole packet is done, the final 64-bits rule flag will be sent to the ACL look-up engine to get the corresponding rule control. GSW can support up to 32 entries ACL rules.

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Take port 0 for example:

0x2004 ff0400 //enable ACL of port 0, this setting is by per-port.

After enable ACL, you need to setup ACL hit pattern. We would check the VLAN for example here.

First:

Set ACL pattern:

0x94 ffff8100 //"ffff" mean compare 2-bytes payload and need match 0x8100.

0x98 0008ff0c //ACL pattern enable, MAC header. P0 to P6. Offset 12byte.

0x90 80005001 //bit [15:12]: 4'b0101:

//Write the specific ACL Table entry. It is 1st rule.

Second:

Set ACL mask:

0x94 00000021 //0x21 = 0010.0001 . Active 1st and 6th rule.

0x98 00000000

0x90 80009002 //bit [15:12]: 4'b1001: Write the specific 3rd ACL Mask entry

//use mask can enable many rules at the same time

Or set ACL mask (another sample):

0x94 00000004 //0x4= 0100. Active 3th rule.

0x98 80000000 //0x80000000= 1000.0000.0000.0000 . Active 63th rule.

0x90 800090 3F //bit [15:12]: 4'b1001: Write the specific 64th ACL Mask entry

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//The first Mask start from “0”, so the 64th mask entry is 0x3f(63).

Setup the ACL action:

0x94 18000080 //Refer to 0x0094 (ACL rule control). This is used for drop packet.

0x98 00000000

0x90 8000b001 //bit [15:12]: 4’b1011: Write ACL rule control entry, Action for 1st rule.

//The first rule entry need to start from “1”.

Destination Address	Source Address	VLAN TAG	Type / Length	Payload	FCS
6 byte	6 byte	4byte	2byte	1500 byte	4 byte

00002004 PCR **Port Control of P0** **00FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000090 **VTCR** **VLAN Table Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_INVLD
Type	W1C	DC														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BUSY	**VLAN Table Is Busy** SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.
30:17	REV0	**Reserved**
16	IDX_INVLD	**Entry is not Valid** This index for the access control is out of the valid index.
15:12	FUNC	**Access Control Function**

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		Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits . 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry. 4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved
11:0	VID	**1. VLAN ID Number: 0x0 to 0x1F (16)** 2. ACL table index: 0x0 to 0x3F (64) 3. ACL mask control: 0x0 to 0x3F (32 or 64)

0x94

(ACL Rule Table)

Bits	Type	Name	Description	Initial value
31:16	RW	BIT_MASK	**Comparison Pattern Mask**	0x0
15:0	RW	CMP_PAT	**Comparison Pattern**	0x0

(ACL Rule Mask)

Bits	Type	Name	Description	Initial value
31:0	RW	ACL_MASK	**ACL Mask[31:0]**	0x0

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(ACL Rule Control)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	0x0
29	RW	ACL_MANG	Management Frame Attribute	0x0
28	RW	INT_EN	Interrupt Enable	0x0
27	RW	ACL_CNT_EN	Enable ACL Hit Count	0x0
26:24	RW	CNT_IDX	Counter Group Index	0x0
23	RW	VLAN_PORT_EN	Swap VLAN Member	0x0
22	RW	DA_SWAP	Multicast MAC Address Swap	0x0
21	RW	SA_SWAP	Source MAC Address Swap	0x0
20	RW	PPP_RM	PPPoE Header Removal	0x0
19	RW	LKY_VLAN	Leaky VLAN	0x0
18:16	RW	EG_TAG	Egress VLAN Tag Attribute	0x0
15:8	RW	PORT	Destination Port / VLAN Member	0x0
7	RW	PORT_EN	Force Destination port	0x0
6:4	RW	PRI_USER	User Priority from ACL	0x0
3	RW	MIR_EN	Frame Copy to Mirror Port	0x0
2:0	RW	PORT_FW	Frame TO_CPU Forwarding	0x0

0x98

(ACL Rule Table)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19	RW	EN	ACL Pattern Enable	0x0
18:16	RW	OFST_TP	Offset Range	0x0
15:8	RW	SP	Incoming Source Port Bit-map	0x0
7:1	RW	WORD_OFST	Word Offset	0x0
0	RW	CMP_SEL	Comparison mode selection	0x0

Offset range table:

3'b000: MAC Header (inc. VLAN tags and Length/Type) (L2 Offset)

3'b001: L2 Payload (L2 Offset)

3'b010: IP Header (L3 Offset)

3'b011: IP Datagram (L3 Offset)

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3'b100: TCP/UDP Header (L4 Offset)

3'b101: TCP/UDP Datagram (L4 Offset)

3'b110: IPv6 Header (L3 Offset)

3'b111: Reserved

(ACL Rule Mask)

Bits	Type	Name	Description	Initial value
31:0	RW	ACL_MASK	ACL Mask[63:32]	0x0

(ACL Rule Control)

Bits	Type	Name	Description	Initial value
31:24	RW	Reserved		0x0
23:19	RW	ACL_CLASS_IDX	**Class index for the 32-entries meter table**	0x0
18:17	RW	Reserved		0x0
16	RW	Reserved		0x0
15:14	RW	Reserved		0x0
13:11	RW	DROP_PCD_G	**User Defined Drop Precedence for Green color packet**	0x0
10:8	RW	DROP_PCD_Y	**User Defined Drop Precedence for Yellow color packet**	0x0
7:5	RW	DROP_PCD_R	**User Defined Drop Precedence for Red color packet**	0x0
4:2	RW	CLASS_SLR	**User Defined Class Selector**	0x0
1	RW	CLASS_SLR_SEL	**Select original class_selector value or ACL control table defined class selector value**	0x0
0	RW	DROP_PCD_SEL	**Select original drop precedence value or ACL control table defined drop Precedence value**	0x0

5.2.4 Broadcast Storm suppression

Broadcast Storm is commonly caused by faulty protocol implementations, undetected network loops, or faulty network equipment. Broadcast storms can cause significant disruption to the network. Broadcast control is possible by using filters or user-defined throttle settings that limit broadcast/multicast propagation to a certain rate.

GSW provide the per-port broadcast storm controller , loop detection and alarm signal to avoid it.

Here we show the example to do the rate-base control of Broadcast storm.

Register 0x30c0 is used for setting the loop detection.

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You may set it if Broadcast storm came from port 1:
Set 0x30c0 as 0x1f130000 //port 0 ~ port 4 enable LPDET,
Set 0x211c as 0xce030303 //set port 1 to detect broadcast storm according to rate-based , and drop the packet. The limit rate is around 3Mbps for 1000Mbps, 100Mbps and 10Mbps base.

Read 0x30c0 again to check the per-port LPDET_ALARMx information.

000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LPDET_EN6	LPDET_EN5	LPDET_EN4	LPDET_EN3	LPDET_EN2	LPDET_EN1	LPDET_EN0	LPDET_PERIOD_EN	LPDET_ALARM_EN	LPDET_PASS	LPDET_PERIOD	LPDET_LED_RATE	LPDET_THRESHOLD		
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_ST_LOOP	LPDET_ST_BCST	LPDET_TRAP_EN							LPDET_ALARM6	LPDET_ALARM5	LPDET_ALARM4	LPDET_ALARM3	LPDET_ALARM2	LPDET_ALARM1	LPDET_ALARM0
Type	RO	RO	RO							RO	RO	RO	RO	RO	RO	W1C
Reset	0	0	0							0	0	0	0	0	0	0

Bit(s)	Name	Description
30	LPDET_EN6	**Enable the loop detection ability of user port 6.** 0: Disable 1: Enable
29	LPDET_EN5	**Enable loop detection the ability of user port 5.** 0: Disable 1: Enable
28	LPDET_EN4	**Enable loop detection the ability of user port 4.** 0: Disable 1: Enable
27	LPDET_EN3	**Enable loop detection the ability of user port 3.** 0: Disable 1: Enable
26	LPDET_EN2	**Enable loop detection the ability of user port 2.** 0: Disable 1: Enable
25	LPDET_EN1	**Enable loop detection the ability of user port 1.** 0: Disable 1: Enable
24	LPDET_EN0	**Enable loop detection the ability of user port 0.** 0: Disable 1: Enable
23	LPDET_PERIOD_EN	**The loop detection frame is triggered by a periodical timer or by broadcast storm.** 0: Broadcast mode 1: Periodical mode
22	LPDET_ALARM_EN	**Enable 2 kHz alarm output and per-port LED when loop is detected.** 0: Disable 1: Enable
21	LPDET_PASS	**Loop detection frame is blocked or passed to packet memory.** 0: Blocked 1: Pass

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20	LPDET_PERIOD	**Interval of transmitting loop detection frame in Periodical mode.** 0: 125 us 1: 1000 ms
19	LPDET_LED_RATE	**LED blinking rate of per port when loop is detected.** 0: LED blinking at 2 Hz 1: LED blinking at 4 Hz
18:16	LPDET_THRESHOLD	**Number of missed loop detection frame before 2 kHz alarm is reset**
15	LPDET_ST_LOOP	**The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.** 0: Not in Loop state 1: Loop state
14	LPDET_ST_BCST	**The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.** 0: Not in BCST state 1: BCST state
13	LPDET_TRAP_EN	**Status of strap pin for loop detection** 0: Disabled 1: Enabled
6	LPDET_ALARM6	**The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
5	LPDET_ALARM5	**The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
4	LPDET_ALARM4	**The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
3	LPDET_ALARM3	**The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
2	LPDET_ALARM2	**The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
1	LPDET_ALARM1	**The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
0	LPDET_ALARM0	**The status of loop detected on port 0. This bit is cleared when it is written as 1.** 0: Not detected 1: Detected

0000201C BSR Broadcast Storm Rate Control of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

5.2.5 Drop Precedence control

The “Drop Precedence” is addon function for the Flow Control. The function can enable or disable. When an enqueue request is on, the control signals of the packet like as queue priority, drop precedence which are from ARL module will feed into Drop Precedence controller, the controller will check the queue depth and drop probability to decide the packet will be dropped or not. Fin ally, it will feedback the “dp_packet_drop” signal to tell the Flow Control to drop the packet or not. The drop precedence of value is by user setting inthe ACL entry or trTCM engine.

The meaning of dorop precedence which is from ARL is

(a) 2’b00, 2’b01 : No drop.

(b) 2’b10 : The drop probability of the incoming packet is based on “Graph A” setting.

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(c) 2'b11 : The drop probability of the incoming packet is based on "Graph B" setting.

PnQm_pr_dp10/11 : Drop probability of Port n Queue m when drop precedence = 2'b10/2'b11.
PnQm_lt_dp10/11 : Low threshold of of Port n Queue m when drop precedence = 2'b10/2'b11.
PnQm_ht_dp10/11 : High threshold of of Port n Queue m when drop precedence = 2'b10/2'b11.

Here we show the test environment as below:

We would design one ACL to hit the"0x0001" in the data from port 6 to mark a color for it. And use DROP precedence at port 0.

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```
;ACL port enable
ethphxcmd gsww 2604 00ff0403

;ACL entry
ethphxcmd gsww 0094 ffff0001        // 0xffff - compare 2-byte data
                                    // 0x0001- compare pattern should be as 0x0001

ethphxcmd gsww 0098 0008400c        // 0x000 MAC offset (bit 18:16)
  //0x8 – ACL pattern enable
                                    // 0x4 – incoming source port is port 6(bit 15:8)
                                    // 0xc –offset
ethphxcmdgsww 0090 80005000         //Write ACL table entry

ethphxcmd gsww 0094 00000001
ethphxcmd gsww 0098 00000000
ethphxcmd gsww 0090 80009000        //Write ACL mask

ethphxcmd gsww 0094 00000000
ethphxcmd gsww 0098 00060000        //mark as red
ethphxcmd gsww 0090 8000b000        //ACL rule control
```

- Set Drop precedence for Port 0 Q2

```
ethphxcmd gsww 180c 80000000  //enable drop precedence
ethphxcmd gsww 1814 80000000
ethphxcmd gsww 182c 011ff000    // Drop probability of P0 Q2
```

0x0098 (ACL Rule Control)

Bits	Type	Name	Description	Initial value
31:24	RW	Reserved		0x0
23:19	RW	ACL_CLASS_ID X	ACL Class index for the 32-entries meter table (TrTcm)	0x0
18:17	RW	ACL_ User defined color remark	00:default, 01:Green, 10:Yellow, 11:Red)	0x0
16	RW	Select Color	1: TrTcm 0: ACL	0x0
15:14	RW	Reserved		0x0
13:11	RW	DROP_PCD_G	User Defined Drop Precedence for Green	0x0
10:8	RW	DROP_PCD_Y	User Defined Drop Precedence for Yellow	0x0
7:5	RW	DROP_PCD_R	User Defined Drop Precedence for Red	0x0
4:2	RW	CLASS_SLR	User Defined Class Selector	0x0
1	RW	CLASS_SLR_S	Select ACL Defined Class Selector	0x0

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		EL		
0	RW	DROP_PCD_SEL	Select ACL Defined Drop Precedence	0x0

0000180C MMDPR_10_Q0 P0 Drop Precedence control 10 of Q0 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P0_DP_en					P0Q0_pr_dp10						P0Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp10[3:0]							P0Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P0_DP_en	**Enable Drop Precedence function of P0. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P0Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P0Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P0Q0_lt_dp10 <= queue depth < P0Q0_ht_dp10, the drop probability of incoming packet is based on the setting P0Q0_pr_dp10. 0: Disable 1: Enable
26:24	P0Q0_pr_dp10	**Drop probability of P0 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q0_ht_dp10	**High threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q0_lt_dp10	**Low threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001814 MMDPR_10_Q2 P0 Drop Precedence control 10 of Q2 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q2_pr_dp10						P0Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q2_ht_dp10[3:0]							P0Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q2_pr_dp10	**Drop probability of P0 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)

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20:12	P0Q2_ht_dp10	**High threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q2_lt_dp10	**Low threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size**

0000182C MMDPR_11_Q0_P0 Drop Precedence control 11 of Q0 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q0_pr_dp11						P0Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp11[3:0]							P0Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q0_pr_dp11	**Drop probability of P0 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q0_ht_dp11	**High threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q0_lt_dp11	**Low threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size**

5.2.6 Egress Rate limit control

There are many ways to do the rate control, like ACL rate control, ingress or egress rate control. If you want to use egress rate control, please disable flow control first to avoid the ingress congestion.

Set bit 31 of 0x1fe0 as 0 to disable global flow control.
Set 0x10e0 as 0x118 to include the IPG byte for egress rate control.
Here we show the sample for port 1 egress rate control.

egress rate	Reg 0x1140
10Mbps	0x0138898f
20Mbps	0x0271898f
30Mbps	0x03a9898f
40Mbps	0x04e2898f
100Mbps	0x0c35898f

000010E0 GERLCR Global Egress Rate Limit Control Register 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name							EGC_MFRM_EX	EGC_IPG_OP	EGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
9	EGC_MFRM_EX	**When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)** 0: Include management frames 1: Exclude management frames
8	EGC_IPG_OP	**Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	EGC_IPG_BYTE	**Egress Rate IPG Byte Count** Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC (default) 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble

00001040 ERLCR_P0 Egress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P0			EGC_RATE_CIR_16_P0	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0				EGC_TB_EN_P0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P0	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P0	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P0	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms

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		11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P0	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0	**Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

5.2.7 *Flow control*

You should set 0x1fe0 bit 31 as 1 for global flow control first.

We take Port 5 for example, if you want to disable TX and RX flow control, you should set the bit 5 and bit 4 of 0x3500 as 0. And read 4th and 5th bit of 0x3508 to check it works or not.

Please know we just discussed about the MAC layer flow control. You need to check the PHY ability if you use auto polling mode. Please check the blow table:

00001FE0 GFCCR0 Global Flow_Control Control Register 0 A0087858

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_EN		FC_OFF2ON_OPT	FC_ON2OFF_OPT					FC_PORT_BLK_THD							
Type	RW		RW	RW					RW							
Reset	1		1	0					0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FC_FREE_BLK_HITHD								FC_FREE_BLK_LOTHD							
Type	RW								RW							
Reset	0	1	1	1	1	0	0	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
31	FC_EN	0: Disable flow control 1: Enable flow control

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29	FC_OFF2ON_OPT	**Flow control assertion option** 0: Disable 1: Enable aggressive frame discard option in flow control transition from OFF to ON
28	FC_ON2OFF_OPT	**Flow control de-assertion option** 0: Disable 1: Enable aggressive frame discard option in flow control transition from ON to OFF
23:16	FC_PORT_BLK_THD	**Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)**
15:8	FC_FREE_BLK_HITHD	**High water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.**
7:0	FC_FREE_BLK_LOTHD	**Low water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.**

00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P5		EXT_PHY_P5	MAC_MODE_P5
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P5	MAC_TX_EN_P5	MAC_RX_EN_P5		MAC_PRE_P5		BKOFF_EN_P5	BACKPR_EN_P5	FORCE_EEE1G_P5	FORCE_EEE100_P5	FORCE_RX_FC_P5	FORCE_TX_FC_P5	FORCE_SPD_P5		FORCE_DPX_P5	FORCE_LNK_P5
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5		MAC_DPX_STS_P5	MAC_LNK_STS_P5
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P5	**PORT 5 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P5	**PORT 5 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P5	**PORT 5 RX XFC Status. Port 5 Rx flow control status** 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P5	**PORT 5 TX XFC Status** PORT 5 TX flow control status 0: Disabled. 1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P5	**PORT 5 Speed [1:0] Status**

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		Current speed of PORT 5 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P5	**PORT 5 duplex Status** Current duplex mode of port 5 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P5	**Port 5 Link Up Status. Link up status of PORT 5.** 0: Link Down 1: Link Up

5.2.8 *Ingress rate control*

Ingress rate control is one of basic rate control. We cannot limit the rate of physical transmission line, but we can limit the resources of packet process rate.
Refer to the below to know the behavior of ingress rate control:

-Each interval of time (programmable) H/W fill IGC_CIR bit token to bucket.
-H/W remove token (equal to packet size) when there is packet income.
-if remain token > packet, the packet can pass to network otherwise will drop packet.
-A bucket with CBS sizes allow some burst traffic pass switch.

For example, to set the ingress rate as 1000kbps
EGC_TBEN = 1
EGC_CIR = 1000K/32K = 31 = 0x1f
EGC_TB_T = ¼ ms

To avoid the inter-fame gap effect, please set 0x1ff0 as 0x00110118
We provide some reference data to do the rate control. For port 1, please set the register 0x1800.

Ingress CIR	Reg 0x1800

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Ingress CIR	Reg 0x1800
10Mbps	0x0138898f
20Mbps	0x0271898f
30Mbps	0x03a9898f
40Mbps	0x04e2898f
100Mbps	0x0c35898f

00001FF0 GIRLCR Global Ingress Rate Limit Control Register 00110104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IGC_FC_OFF_THD				IGC_FC_DROP_THD			
Type									RW				RW			
Reset									0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IGC_MFRM_EX	IGC_IPG_OP	IGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
23:20	IGC_FC_OFF_THD	**Ingress Rate Limit Pause-Off Threshold** Pause-off frame is sent when the ingress token bucket is higher than pause-off threshold. Threshold = max_bucket_size >> igc_fc_off_thd
19:16	IGC_FC_DROP_THD	**Ingress Rate Limit Drop Threshold** If Port Flow Control and rate limit control is enabled, frame is drop when the ingress token bucket is less than drop threshold. Threshold = -(max_bucket_size >> igc_fc_drop_thd)
9	IGC_MFRM_EX	**Ingress Rate Excludes Management Frames** Management frames will be ignored by rate limit. (management frame type is set by ARL registers) 0: Include management frames 1: Exclude management frames
8	IGC_IPG_OP	**Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	IGC_IPG_BYTE	**Ingress Rate IPG Byte Count** Byte count should be added while calculating the rate limit 8'h4: add 4 byte CRC (byte rate calculation) 8'h18: add 4 byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation)

00001800 IRLCR_P0 Ingress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P0			IGC_RATE_CIR_16_P0	IGC_RATE_EXP_P0_IGC_TB_T_P0				IGC_TB_EN_P0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						

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Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P0	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P0	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P0	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P0_IGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P0	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0	**Mantissa part of port 0 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

5.2.9 *Link Status*

You can find MAC control register put at 0x3500 for MAC 5, and 0x3600 for MAC 6. You can change MAC ability at this register. We would suggest don't use the register 0x3000 to 0x3400. It may not work.

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00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P5		EXT_PHY_P5	MAC_MODE_P5
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P5	MAC_TX_EN_P5	MAC_RX_EN_P5		MAC_PRE_P5		BKOFF_EN_P5	BACKPR_EN_P5	FORCE_EEE1G_P5	FORCE_EEE100_P5	FORCE_RX_FC_P5	FORCE_TX_FC_P5	FORCE_SPD_P5		FORCE_DPX_P5	FORCE_LNK_P5
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P5	**PORT 5 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P5	**PORT 5 External PHY** Port 5 connects with external PHY. 0: PORT 5 DOES NOT connect with external PHY. 1: PORT 5 connects with external PHY.
16	MAC_MODE_P5	**PORT 5 MAC Mode** PORT 5 operates in MAC mode. 0: PORT 5 operates in PHY mode. 1: PORT 5 operates in MAC mode.
15	FORCE_MODE_P5	**PORT 5 Force Mode** PORT 5 operates in force mode. It is used to control PORT 5 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g. 0: Force mode is off (mac status is determined by phy auto-polling module). 1: Force mode is on (mac status is determined by force_xxx_P5 register).
14	MAC_TX_EN_P5	**Port 5 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P5	**PORT 5 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P5	**TX short preamble mode**

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		0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P5	**PORT 5 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 5 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P5	**PORT 5 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P5	**PORT 5 Force LPI Mode For 1000Mbps** When (force_mode_P5 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps
6	FORCE_EEE100_P5	**PORT 5 Force LPI Mode For 100Mbps** When (force_mode_P5 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps
5	FORCE_RX_FC_P5	**PORT 5 Force RX FC** When (force_mode_P5 = 1), this bit is used to control the RX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P5	**PORT 5 Force TX FC** When (force_mode_P5 = 1), this bit is used to control the TX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P5	**PORT 5 Force Speed [1:0]** When (force_mode_P5 = 1), these bits are used to control MAC speed of PORT 5. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P5	**PORT 5 Force duplex** When (force_mode_P5 = 1), this bit is used to control MAC duplex of PORT 5. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P5	**PORT 5 Force MAC Link Up** When (force_mode_P5 = 1), this bit is used to control link status of PORT 5. 0: Link Down 1: Link Up

For MAC 5 and MAC6, they have its own status to check register. 0x3508 is for MAC 5 status and 0x3608 is for MAC 6. If you want to change MAC 5 status, you can use 0x3500 to change its ability.

00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5		MAC_DPX_STS_P5	MAC_LNK_STS_P5
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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7	EEE1G_STS_P5	**PORT 5 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P5	**PORT 5 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P5	**PORT 5 RX XFC Status. Port 5 Rx flow control status** 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P5	**PORT 5 TX XFC Status** PORT 5 TX flow control status 0: Disabled. 1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P5	**PORT 5 Speed [1:0] Status** Current speed of PORT 5 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P5	**PORT 5 duplex Status** Current duplex mode of port 5 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P5	**Port 5 Link Up Status. Link up status of PORT 5.** 0: Link Down 1: Link Up

5.2.10 *Link Status change*

You can find the 0x700c is a record if PHY status was changed. For example, if you plug into PHY 1, you can find the 0x700c become 00080002. Then drew the PHY 1, the 0x700c would still keep 00080002.You need to write “1” to the bit which you want clean at the register 0x700c. After that you can find it would become 00080000.

0000700C SYS_INT_STS System Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_INT	ARL_SEC_TAG_INT	ARL_SEC_VLAN_INT	ARL_SEC_IG1X_INT	ARL_PKT_BC_INT	ARL_EQ_ERR_INT	ARL_PKT_QERR_INT	ARL_TBL_ERR_INT					PTP_INT	MIB_INT	BMU_INT	MAC_PC_INT
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PHY6_INT	PHY5_INT	PHY4_INT	PHY3_INT	PHY2_INT	PHY1_INT	PHY0_INT		PHY6_LC_INT	PHY5_LC_INT	PHY4_LC_INT	PHY3_LC_INT	PHY2_LC_INT	PHY1_LC_INT	PHY0_LC_INT
Type		W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

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5.2.11 *LED controller*

All hardware traps of GSW are weakly pull-up internally. The only way to pull-down these traps is using an external pull-down circuit. However, hardware traps and LEDs share the same pins in GSW. To make LEDs work normally, the hardware configurations of LEDs will depend on its related values in the current design.
Every port has 1 LED to mean its behavior:

GSW Px_LED_0 is used for any ability linkup and traffic (10/100/1000).

For trapping-high pins, the external LEDs should be active low. Its configuration is shown as below. OEs (output enables) of LED pads are controlled by the internal circuits, and LED_DO will always be LOW under this configuration. So the external LEDs should be active low.

For LED configuration, you can follow the below descrition.

00007D00 LED_EN LED I/O function enable 00077777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_EN		
Type														RW		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_EN				P2_LED_EN				P1_LED_EN				P0_LED_EN		
Type		RW				RW				RW				RW		
Reset		1	1	1		1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
18:16	P4_LED_EN	**P4 LED I/O Enable** P4_LED_EN[2] for P4 LED #2 P4_LED_EN[1] for P4 LED #1 P4_LED_EN[0] for P4 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
14:12	P3_LED_EN	**P3 LED I/O Enable** P3_LED_EN[2] for P3 LED #2 P3_LED_EN[1] for P3 LED #1 P3_LED_EN[0] for P3 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
10:8	P2_LED_EN	**P2 LED I/O Enable**

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		P2_LED_EN[2] for P2 LED #2 P2_LED_EN[1] for P2 LED #1 P2_LED_EN[0] for P2 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
6:4	P1_LED_EN	**P1 LED I/O Enable** P1_LED_EN[2] for P1 LED #2 P1_LED_EN[1] for P1 LED #1 P1_LED_EN[0] for P1 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
2:0	P0_LED_EN	**P0 LED I/O Enable** P0_LED_EN[2] for P0 LED #2 P0_LED_EN[1] for P0 LED #1 P0_LED_EN[0] for P0 LED #0 For individual LED 1'b0: Disable 1'b1: Enable

00007D04 LED_IO_MODE LED I/O Mode 00077777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_MODE		
Type														RW		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_MODE				P2_LED_MODE				P1_LED_MODE				P0_LED_MODE		
Type		RW				RW				RW				RW		
Reset		1	1	1		1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
18:16	P4_LED_MODE	**P4 LED I/O Mode** P4_LED_MODE[2] for P4 LED #2 P4_LED_MODE[1] for P4 LED #1 P4_LED_MODE[0] for P4 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
14:12	P3_LED_MODE	**P3 LED I/O Mode** P3_LED_MODE[2] for P3 LED #2 P3_LED_MODE[1] for P3 LED #1 P3_LED_MODE[0] for P3 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
10:8	P2_LED_MODE	**P2 LED I/O Mode** P2_LED_MODE[2] for P2 LED #2 P2_LED_MODE[1] for P2 LED #1 P2_LED_MODE[0] for P2 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
6:4	P1_LED_MODE	**P1 LED I/O Mode** P1_LED_MODE[2] for P1 LED #2 P1_LED_MODE[1] for P1 LED #1 P1_LED_MODE[0] for P1 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED

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2:0	P0_LED_MODE	**P0 LED I/O Mode** P0_LED_MODE[2] for P0 LED #2 P0_LED_MODE[1] for P0 LED #1 P0_LED_MODE[0] for P0 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED

If you want to change the LED behavior, please write these registers of Ethernet physical.

51F00240 dev1Fh_reg024h LED0 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led0_en	rg_led0_pol								led0_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led0_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led0_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led0_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00250 dev1Fh_reg025h LED0 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led0_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led0_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity

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Bit[2]:100Mbps TX Activity
Bit[3]:100Mbps RX Activity
Bit[4]:10Mbps TX Activity
Bit[5]:10Mbps RX Activity
Bit[6]:Collision
Bit[7]:RX CRC Error
Bit[8]:RX Idle Error
Bit[9]:Force Blinks (Logic 1)

51F00260 dev1Fh_reg026h LED1 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led1_en	rg_led1_pol								led1_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led1_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led1_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led1_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00270 dev1Fh_reg027h LED1 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led1_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led1_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity

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Bit[5]:10Mbps RX Activity
Bit[6]:Collision
Bit[7]:RX CRC Error
Bit[8]:RX Idle Error
Bit[9]:Force Blinks (Logic 1)

51F00280 dev1Fh_reg028h LED2 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led2_en	rg_led2_pol								led2_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led2_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led2_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led2_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00290 dev1Fh_reg029h LED2 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led2_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led2_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error

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Bit[8]:RX Idle Error
Bit[9]:Force Blinks (Logic 1)

51F002A0 dev1Fh_reg02Ah LED3 On Control Register 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led3_en	rg_led3_pol								led3_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led3_en	**Enable Ethernet LED Function.** 0: Disable (Hi-Z) 1: Enable
14	rg_led3_pol	**Select LED polarity. This field only takes effect when LED_EN is 1b1.** Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led3_on_mask	**LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.** Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F002B0 dev1Fh_reg02Bh LED3 Blinking Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							led3_blk_mask									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led3_blk_mask	**LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error Bit[8]:RX Idle Error Bit[9]:Force Blinks (Logic 1)

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5.2.12 *Loop Detection*

When loop detection function is enabled by setting hardware strapping(0x7804), the GSW provide two different signal out. One is sent the loop frame with the SID as 0180c2000001, another is sent the period LED.

Follow the step to check it:

1. Set 0x30c0 (for example : enable p0,p1,p3, set as 0x07130000)
2. Set 0x201c,0x211c ..0x261c to enable per port broadcast storm detection(for example, set 0x201c as cc030303 for port 0)

After that, you can check the Loop frame and alarm signal from 96th pin.

3. Read 0x30c0 to check the Alarm message.
(You can write bit 1 of 0x30c0 as 1 to clean the status)

000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LPDET_EN6	LPDET_EN5	LPDET_EN4	LPDET_EN3	LPDET_EN2	LPDET_EN1	LPDET_EN0	LPDET_PERIOD_EN	LPDET_ALARM_EN	LPDET_PASS	LPDET_PERIOD	LPDET_LED_RATE	LPDET_THRESHOLD		
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_ST_LOOP	LPDET_ST_BCST	LPDET_TRAP_EN							LPDET_ALARM6	LPDET_ALARM5	LPDET_ALARM4	LPDET_ALARM3	LPDET_ALARM2	LPDET_ALARM1	LPDET_ALARM0
Type	RO	RO	RO							RO	RO	RO	RO	RO	RO	W1C
Reset	0	0	0							0	0	0	0	0	0	0

Bit(s)	Name	Description
30	LPDET_EN6	**Enable the loop detection ability of user port 6.** 0: Disable 1: Enable
29	LPDET_EN5	**Enable loop detection the ability of user port 5.** 0: Disable 1: Enable
28	LPDET_EN4	**Enable loop detection the ability of user port 4.** 0: Disable 1: Enable
27	LPDET_EN3	**Enable loop detection the ability of user port 3.** 0: Disable 1: Enable
26	LPDET_EN2	**Enable loop detection the ability of user port 2.** 0: Disable 1: Enable
25	LPDET_EN1	**Enable loop detection the ability of user port 1.** 0: Disable 1: Enable
24	LPDET_EN0	**Enable loop detection the ability of user port 0.** 0: Disable

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		1: Enable
23	LPDET_PERIOD_EN	**The loop detection frame is triggered by a periodical timer or by broadcast storm.** 0: Broadcast mode 1: Periodical mode
22	LPDET_ALARM_EN	**Enable 2 kHz alarm output and per-port LED when loop is detected.** 0: Disable 1: Enable
21	LPDET_PASS	**Loop detection frame is blocked or passed to packet memory.** 0: Blocked 1: Pass
20	LPDET_PERIOD	**Interval of transmitting loop detection frame in Periodical mode.** 0: 125 us 1: 1000 ms
19	LPDET_LED_RATE	**LED blinking rate of per port when loop is detected.** 0: LED blinking at 2 Hz 1: LED blinking at 4 Hz
18:16	LPDET_THRESHOLD	**Number of missed loop detection frame before 2 kHz alarm is reset**
15	LPDET_ST_LOOP	**The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.** 0: Not in Loop state 1: Loop state
14	LPDET_ST_BCST	**The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.** 0: Not in BCST state 1: BCST state
13	LPDET_TRAP_EN	**Status of strap pin for loop detection** 0: Disabled 1: Enabled
6	LPDET_ALARM6	**The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
5	LPDET_ALARM5	**The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
4	LPDET_ALARM4	**The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
3	LPDET_ALARM3	**The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
2	LPDET_ALARM2	**The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
1	LPDET_ALARM1	**The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
0	LPDET_ALARM0	**The status of loop detected on port 0. This bit is cleared when it is written as 1.** 0: Not detected 1: Detected

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0000201C BSR Broadcast Storm Rate Control of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

5.2.13 *MAC forward control*

0x0010 is used for MAC forwarding control rule. For different traffic, like broadcast, Unknown multicast...etc, you can set the forwarding port at this register.

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00000010 MFC MAC Forward Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BC_FFP								UNM_FFP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNU_FFP								CPU_EN	CPU_PORT			MIRROR_EN	MIRROR_PORT		
Type	RW								RW	RW			RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BC_FFP	**Broadcast Frame Flooding Ports** If MAC receives broadcast frames, this field indicates the flooding ports. [NOTE] 1. The flooding port excludes the received port on the switch. 2. Frame dropped though BC_FFP=6'b0
23:16	UNM_FFP	**Unknown Multicast Frame Flooding Ports** If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports. [NOTE] 1. The flooding port will exclude the received port by HW. 2. Frame dropped though UNM_FFP=6'b0.
15:8	UNU_FFP	**Unknown Unicast Frame Flooding Ports** If MAC receives the unicast or multicast frames which can not be found on the ARL. The field indicates the flooding port. [NOTE] 1. The flooding port will excludes the received port by HW 2. Frame dropped though UNM_FFP=6'b0
7	CPU_EN	**CPU Port Enable** Enable the CPU port specified in CPU_PORT. 0: No CPU port exists. 1: Enable
6:4	CPU_PORT	**CPU Port Number** Set the CPU port number. 3'h0: Port 0 ... 3'h7: Port 7
3	MIRROR_EN	**Mirror Port Enable** Enable the mirror port specified in MIRROR_PORT. 0: No mirror available 1: Enable mirror
2:0	MIRROR_PORT	**Mirror Port Number** Set the mirror port number. 3'h0: Port 0 ... 3'h7: Port 7

Here also show the forwarding rule which you can set at register 0x0010.

FTAG	ACL Enable	ARL/DIP Table	Action
BC	ACL Hit and Port Map is enabled	-	Follow ACL Forwarding Port Map
	Disable or ACL not Hit	-	Follow MFC .BC_FFP register
MC	ACL Hit and Port Map	-	Follow ACL Forwarding Port Map

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IP_MULT IPV6_MULTI	is enabled		
	Disable or ACL not Hit	ARL Hit	Follow ARL Forwarding Port Map
		ARL not Hit	Follow MFC.UNM_FFP register
UC	ACL Hit and Port Map is enabled	-	Follow ACL Forwarding Port Map
	Disable or ACL not Hit	ARL Hit	Follow ARL Forwarding Port Map
		ARL not Hit	Follow MFC.UNU_FFP register

5.2.14 *MAC table aging time*

Aging time is used for recording the MAC is exist or not and would be clean after 300 seconds if there is no traffic pass through again. For changing this, you can modify the 0x00A0.
The aging time would be depending on the switch core clock speed.

000000A0 AAC Address Age Control 00095001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0											AGE_DIS	AGE_CNT[7:4]			
Type	DC											RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_CNT[3:0]				AGE_UNIT											
Type	RW				RW											
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:21	REV0	**Reserved**
20	AGE_DIS	**Address Table Aging Disable** Disable or pause MAC address aging.
19:12	AGE_CNT	**Address Table Age Count** This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds.
11:0	AGE_UNIT	**Address Table Age Unit** The applied aging unit is equal to (AGE_UNIT+1) seconds.

5.2.15 *MAC table*

We have 2048 MAC entries exist in switch.
GSW build in the API command:
Ethphxcmd arl mactbl-disp
MAC AABBCCDDEEFF : TIMER:149, SA_PORT_FW:0, SA_MIR_EN:0, USER_PRI:0, EG_TAG:0, LEAKY_EN:0, PORT:4, STATUS:1, TYPE:0
You can find that have an aging time, source port information over there.

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For RT63368 or others platform, you can use the command flow to check the MAC table list:

Ethphxcmd gsww 80 8002 //clean
Ethphxcmd gsww 80 8004 //first MAC entry
Ethphxcmd gswr 84 // show the first entry
Ethphxcmd gswr 88 // show the firstentry
Ethphxcmd gsww 80 8005 //next MAC entry
Ethphxcmd gswr 84 // show the second entry
Ethphxcmd gswr 88 // show the second entry

For detail, you can check the register 0x0080,0x0084 and 0x0088.

00000080 ATC Address Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				ADDR											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSY	SRCH_END	SRCH_HIT	ADDR_INVLD	AC_MAT				REV1		AC_SAT		REV2	AC_CMD		
Type	W1C	RO	RO	RO	RW				DC		RW		DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000084 TSRA1 Table Search Read Address I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[47:40] / Destination IP(DIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[39:32] / Destination IP(DIP) Address [23:16]**
15:8	BYTE_2	**MAC Address[31:24] / Destination IP(DIP) Address [15:8]**
7:0	BYTE_3	**MAC Address[23:16] / Destination IP(DIP) Address [7:0]**

00000088 TSRA2 Table Search Read Address II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[15:8] / Source IP(SIP) Address [31:24]**

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23:16	BYTE_1	**MAC Address[7:0] / Source IP(SIP) Address [23:16]**
15:8	BYTE_2	**SIP Address [15: 8] or** bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table.
7:0	BYTE_3	**SIP Address[7:0] or CVID[7:0]**

5.2.16 *Output queue*

Each port has 8 queues for different QoS services. Please know that QoS only active when traffic jam happen. It means that you should have flow control first for QoS. If not, you would only find the packet loss.
Free page: Read the 0x1fc0

For GSW, if you want to check the queue, please use:
ethphxcmd gsww 7038 220
ethphxcmd gswr 7034

Here show the Q map:

	Q1 & Q0	Q3 & Q2	Q5 & Q4	Q7 & Q6
P0	220	221	222	223
P1	224	225	226	227
P2	228	229	22a	22b
P3	22c	22d	22e	22f
P4	230	231	232	233
P5	234	235	236	237
P6	238	239	23a	23b

00001FC0 FPLC Free Page Link Count Register 01EE01EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MIN_FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0

Bit(s)	Name	Description
25:16	MIN_FREE_PL_CNT	**Minimal Free Page Link Count in LMU from last read access**
9:0	FREE_PL_CNT	**Free Page Link Count in LMU**

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5.2.17 *VLAN setting*

You need use three registers to make one VLAN rule. Please follow the below information to do that:
Set the port you want into security mode and as user port, take port 1 as example:

0x 2104 00ff0003 //set as security mode
0x 2110 81000000 //set as user port
You should set up the each VLAN port you want to be security mode and user port.
Next, you need to setup the VLAN ID and group member. Here, we set port 0 to 3 and port 6 as one group and their VLAN ID is 10. And just only port 3 get the egress tag.

0x94 104F0001 Port member 0~3+6 (4f =0100 1111)
0x98 000000c0 Egress tag enable for port 3 , refer to register 0x98
0x90 80001003 VID member VID set as 03
Note: Please don't use 0 and 4095 for VID.

If you do not want to add egress tag at any port, just set 0x98 as 0. For detail, check the register 0x0098 at the below.

00002104 PCR Port Control of P1 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000090 VTCR VLAN Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_INVLD
Type	W1C	DC														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BUSY	**VLAN Table Is Busy** SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on

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		FUNC bits.
30:17	REV0	**Reserved**
16	IDX_INVLD	**Entry is not Valid** This index for the access control is out of the valid index.
15:12	FUNC	**Access Control Function** Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits . 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry. 4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved
11:0	VID	**1. VLAN ID Number: 0x0 to 0x1F (16)** 2. ACL table index: 0x0 to 0x3F (64) 3. ACL mask control: 0x0 to 0x3F (32 or 64)

00000094 VAWD1 VLAN and ACL Write Data I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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(VLAN Entry)

Bits	Type	Name	Description	Initial value
31	RW	PORT_STAG	Port based STAG	0x0
30	RW	IVL_MAC	Independent VLAN Learning	0x0
29	RW	EG_CON	Egress Tag Consistent	0x0
28	RW	VTAG_EN	Per VLAN Egress Tag Control	0x0
27	RW	COPY_PRI	Copy User Priority Value from Customer Priority Tag for Stack VLAN	0x0
26:24	RW	USER_PRI	Service Tag User Priority Value from VLAN Table	0x0
23:16	RW	PORT_MEM	VLAN Member Control	0x0
15:4	RW	S_TAG1	Service Tag I	0x0
3:1	RW	FID	Filtering Database	0x0
0	RW	VALID	VLAN Entry Valid	0x0

00000098 VAWD2 VLAN and ACL Write Data II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(VLAN Entry)

Bits	Type	Name	Description	Initial value
31:16	RW	S_TAG2	Service Tag II	0x0
15:14	-	-	Reserved	0x0
13:12	RW	P6_TAG	P6 Egress Tag Control	0x0
11:10	RW	P5_TAG	P5 Egress Tag Control	0x0
9:8	RW	P4_TAG	P4 Egress Tag Control	0x0
7:6	RW	P3_TAG	P3 Egress Tag Control	0x0
5:4	RW	P2_TAG	P2 Egress Tag Control	0x0
3:2	RW	P1_TAG	P1 Egress Tag Control	0x0
1:0	RW	P0_TAG	P0 Egress Tag Control	0x0

00002010 PVC Port VLAN Control of P0 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the

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		indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

Note: if you want to drop (or not)packet with VLAN tag(or not), you can set bit 1:0 of REG 0x2010,0x2110,0x2210…0x2610 to do that.

5.2.18 *QoS (Quality of Services)*

QoS is the ability to provide different priority to different applications or the data flows. GSW can support strict priority (SP) and weighted round-robin (WRR) mode for QoS. Please refer to packet format at the below figure and know the VID and user priority are the key for QoS. We will suggest that you should disable flow control if you want to use QoS.

SP:

WRR:

You may need to make the port you want as security mode and user port first. For detail, please check the page about VALN setting in this document.

0x 2104 00ff0003 //set as security mode
0x 2110 81000000 //set as user port

0x94 104F0001 Port member 0~3+6 (4f =0100 1111)
0x98 000000c0 Egress tag enable for port 3 , refer to register 0x98
0x90 80001003 VID member VID set as 03
Please also refer the chapter of VLAN to know the detail setting.

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Follow the step to setup the QoS:

Default Priority-to-queue mapping
(802.3D QoS)
Priority 7 – Queue 7
Priority 6 – Queue 6
Priority 5 – Queue 5
Priority 4 – Queue 4
Priority 3 – Queue 3
Priority 1 – Queue 2
Priority 0 – Queue 1
Priority 2 – Queue 0

You can swap the Q map as you want.
For example:
Change priority 1 from Q2 to Q1:
0x0048 09080240
Change priority 1 from Q1 to Q2:
0x0048 0a080240

Please notice the GSW use output queue structure.
That means you should set these setting at output port.
Set as Tag-base
0x0044 as 0x222722 //Tag-base for first priority

If want to use SP:
0x1000 as 0x80000000 //SP for Q0 of Port 0
0x1004 as 0x00000000 //SP for Q0 of Port 0
0x1008 as 0x80000000 //SP for Q1 of Port 0
0x100c as 0x00000000 //SP for Q1 of Port 0

If want to use WRR:
0x1000 as 0x80008000 //WRR for Q0 of P0
0x1004 as 0x01000000 //weight of Q0 of P0
0x1008 as 0x80008000 //WRR for Q1 of P0
0x100c as 0x03000000 //weight of Q1 of P0

Set the port weight:
0x1004 as 0x01000000 //Weighting of P0 Q0 is 2 (**q0_max_weight+1'b1)**
0x100c as 0x03000000 //Weighting of P0 Q1 is 4 (**q1_max_weight+1'b1)**
…
Note: Queue n service with probability Pn (Pn = weight n / Sum (weight))

Follow the table and set the mode as SP or WRR.

	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Port 0	0x1000	0x1008	0x1010	0x1018	0x1020	0x1028	0x1030	0x1038
Port 1	0x1100	0x1108	0x1110	0x1118	0x1120	0x1128	0x1130	0x1138
Port 2	0x1200	0x1208	0x1210	0x1218	0x1220	0x1228	0x1230	0x1238
Port 3	0x1300	0x1308	0x1310	0x1318	0x1320	0x1328	0x1330	0x1338
Port 4	0x1400	0x1408	0x1410	0x1418	0x1420	0x1428	0x1430	0x1438
Port 5	0x1500	0x1508	0x1510	0x1518	0x1520	0x1528	0x1530	0x1538

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	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Port 6	0x1600	0x1608	0x1610	0x1618	0x1620	0x1628	0x1630	0x1638

P0 weighting setting map:

00001004	**MMSCR1_Q0P0**	32	**Max-Min Scheduler Control Register 1 of Queue 0/Port 0**
0000100C	**MMSCR1_Q1P0**	32	**Max-Min Scheduler Control Register 1 of Queue 1/Port 0**
00001014	**MMSCR1_Q2P0**	32	**Max-Min Scheduler Control Register 1 of Queue 2/Port 0**
0000101C	**MMSCR1_Q3P0**	32	**Max-Min Scheduler Control Register 1 of Queue 3/Port 0**
00001024	**MMSCR1_Q4P0**	32	**Max-Min Scheduler Control Register 1 of Queue 4/Port 0**
0000102C	**MMSCR1_Q5P0**	32	**Max-Min Scheduler Control Register 1 of Queue 5/Port 0**
00001034	**MMSCR1_Q6P0**	32	**Max-Min Scheduler Control Register 1 of Queue 6/Port 0**
0000103C	**MMSCR1_Q7P0**	32	**Max-Min Scheduler Control Register 1 of Queue 7/Port 0**

00000044 UPW User Priority Weight 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0									ARL_UPW			REV1	PORT_UPW		
Type	DC									RW			DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	DC	RW			DC	RW			DC	RW			DC	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
31:23	REV0	**Reserved**
22:20	ARL_UPW	**ARL User Priority Weight (MAC/DIP Hit)**
19	REV1	**Reserved**
18:16	PORT_UPW	**Port-Based User Priority Weight Value** Weights range from 0x0 to 0x7.
15	REV2	**Reserved**
14:12	DSCP_UPW	**DSCP Priority Weight (IPv4)**
11	REV3	**Reserved**
10:8	TAG_UPW	**Priority Tag User Priority Weight**
7	REV4	**Reserved**
6:4	STAG_UPW	**Special Tag User Priority Weight**
3	REV5	**Reserved**
2:0	ACL_UPW	**ACL User Priority Weight (ACL Hit)**

00000048 PEM1 User Priority Egress Mapping I 08480240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_1			QUE_CPU_1			QUE_LAN_1		DSCP_PRI_1					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_0			QUE_CPU_0			QUE_LAN_0		DSCP_PRI_0					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**

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29:27	TAG_PRI_1	**User Priority 1 Priority Tag Value**
26:24	QUE_CPU_1	**User Priority 1 CPU Queue Selectio**
23:22	QUE_LAN_1	**User Priority 1 LAN Queue Selection**
21:16	DSCP_PRI_1	**User Priority 1 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_0	**User Priority 0 Priority Tag Value**
10:8	QUE_CPU_0	**User Priority 0 CPU Queue Selectio**
7:6	QUE_LAN_0	**User Priority 0 LAN Queue Selection**
5:0	DSCP_PRI_0	**User Priority 0 DSCP Value**

0000004C PEM2 User Priority Egress Mapping II 1B581110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_3			QUE_CPU_3			QUE_LAN_3		DSCP_PRI_3					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_2			QUE_CPU_2			QUE_LAN_2		DSCP_PRI_2					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_3	**User Priority 3 Priority Tag Value**
26:24	QUE_CPU_3	**User Priority 3 CPU Queue Selectio**
23:22	QUE_LAN_3	**User Priority 3 LAN Queue Selection**
21:16	DSCP_PRI_3	**User Priority 3 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_2	**User Priority 2 Priority Tag Value**
10:8	QUE_CPU_2	**User Priority 2 CPU Queue Selectio**
7:6	QUE_LAN_2	**User Priority 2 LAN Queue Selection**
5:0	DSCP_PRI_2	**User Priority 2 DSCP Value**

00001000 MMSCR0_Q0P0 Max-Min Scheduler Control Register 0 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P0				MIN_RATE_CTRL_EXP_Q0_P0					MIN_RATE_CTRL_MAN_Q0_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P0	**Port 0 Queue 0 min. traffic arbitration scheme**

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		0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P0	**Port 0 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass (infinite rate). 1: Queue 0 min. rate limit control is enabled.
11:8	MIN_RATE_CTRL_EXP_Q0_P0	**Exponent part of Port 0 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P0	**Mantissa part of Port 0 Queue 0 min. shaper rate limit control** Value range: 1..100

00001004 MMSCR1_Q0P0 Max-Min Scheduler Control Register 1 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P0				MAX_WEIGHT_Q0_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P0				MAX_RATE_CTRL_EXP_Q0_P0					MAX_RATE_CTRL_MAN_Q0_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P0	**Port 0 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P0	**Port 0 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P0	**Port 0 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate). 1: Queue 0 maximum shaper rate limit is enabled.
11:8	MAX_RATE_CTRL_EXP_Q0_P0	**Exponent part of Port 0 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P0	**Mantissa part of Port 0 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001008 MMSCR0_Q1P0 Max-Min Scheduler Control Register 0 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_R				MIN_RATE_CTRL_EXP_Q1					MIN_RATE_CTRL_MAN_Q1_P0						

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	ATE_EN_Q1_P0				_P0											
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P0	**Port 0 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P0	**Port 0 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P0	**Exponent part of Port 0 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P0	**Mantissa part of Port 0 Queue 1 min. shaper rate limit control** Value range: 1..127

0000100C MMSCR1_Q1P0 Max-Min Scheduler Control Register 1 of Queue 1/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P0				MAX_WEIGHT_Q1_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P0				MAX_RATE_CTRL_EXP_Q1_P0					MAX_RATE_CTRL_MAN_Q1_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P0	**Port 0 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P0	**Port 0 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P0	**Port 0 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P0	**Exponent part of Port 0 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P0	**Mantissa part of Port 0 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001010 MMSCR0_Q2P0 Max-Min Scheduler Control Register 0 of Queue 2/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WR															

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	R_Q2_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P0				MIN_RATE_CTRL_EXP_Q2_P0					MIN_RATE_CTRL_MAN_Q2_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P0	**Port 0 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P0	**Port 0 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P0	**Exponent part of Port 0 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P0	**Mantissa part of Port 0 Queue 2 min. shaper rate limit control** Value range: 1..127

00001014 MMSCR1_Q2P0 Max-Min Scheduler Control Register 1 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P0				MAX_WEIGHT_Q2_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P0				MAX_RATE_CTRL_EXP_Q2_P0					MAX_RATE_CTRL_MAN_Q2_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P0	**Port 0 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P0	**Port 0 Queue 2 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P0	**Port 0 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P0	**Exponent part of Port 0 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN	**Mantissa part of Port 0 Queue 2 maximum shaper rate limit control**

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	_Q2_P0	Value range: 0..127 (7-bit)

00001018 MMSCR0_Q3P0 Max-Min Scheduler Control Register 0 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P0				MIN_RATE_CTRL_EXP_Q3_P0					MIN_RATE_CTRL_MAN_Q3_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P0	**Port 0 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P0	**Port 0 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P0	**Exponent part of Port 0 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P0	**Mantissa part of Port 0 Queue 3 min. shaper rate limit control** Value range: 1..127

0000101C MMSCR1_Q3P0 Max-Min Scheduler Control Register 1 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P0				MAX_WEIGHT_Q3_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P0				MAX_RATE_CTRL_EXP_Q3_P0					MAX_RATE_CTRL_MAN_Q3_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P0	**Port 0 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P0	**Port 0 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P0	**Port 0 Queue 3 maximum shaper rate limit control is enabled.**

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		0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P0	**Exponent part of Port 0 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P0	**Mantissa part of Port 0 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001020 MMSCR0_Q4P0 Max-Min Scheduler Control Register 0 of Queue 4/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P0				MIN_RATE_CTRL_EXP_Q4_P0					MIN_RATE_CTRL_MAN_Q4_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P0	**Port 0 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P0	**Port 0 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P0	**Exponent part of Port 0 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P0	**Mantissa part of Port 0 Queue 4 min. shaper rate limit control** Value range: 1..127

00001024 MMSCR1_Q4P0 Max-Min Scheduler Control Register 1 of Queue 4/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P0				MAX_WEIGHT_Q4_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P0				MAX_RATE_CTRL_EXP_Q4_P0					MAX_RATE_CTRL_MAN_Q4_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description

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31	MAX_SP_WFQ_Q4_P0	**Port 0 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P0	**Port 0 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P0	**Port 0 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P0	**Exponent part of Port 0 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P0	**Mantissa part of Port 0 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001028 MMSCR0_Q5P0 Max-Min Scheduler Control Register 0 of Queue 5/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P0				MIN_RATE_CTRL_EXP_Q5_P0					MIN_RATE_CTRL_MAN_Q5_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P0	**Port 0 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P0	**Port 0 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P0	**Exponent part of Port 0 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P0	**Mantissa part of Port 0 Queue 5 min. shaper rate limit control** Value range: 1..127

0000102C MMSCR1_Q5P0 Max-Min Scheduler Control Register 1 of Queue 5/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P0				MAX_WEIGHT_Q5_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE				MAX_RATE_CTRL_EXP_Q5_P0					MAX_RATE_CTRL_MAN_Q5_P0						

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	_EN_ Q5_P0															
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P0	**Port 0 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P0	**Port 0 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P0	**Port 0 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP _Q5_P0	**Exponent part of Port 0 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN _Q5_P0	**Mantissa part of Port 0 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001030 MMSCR0_Q6P0 Max-Min Scheduler Control Register 0 of Queue 6/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P0				MIN_RATE_CTRL_EXP_Q6_P0					MIN_RATE_CTRL_MAN_Q6_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P0	**Port 0 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P0	**Port 0 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_ Q6_P0	**Exponent part of Port 0 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_ Q6_P0	**Mantissa part of Port 0 Queue 6 min. shaper rate limit control** Value range: 1..127

00001034 MMSCR1_Q6P0 Max-Min Scheduler Control Register 1 of Queue 6/Port 00000000 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_				MAX_WEIGHT_Q6_P0											

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	SP_WFQ_Q6_P0															
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P0				MAX_RATE_CTRL_EXP_Q6_P0					MAX_RATE_CTRL_MAN_Q6_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P0	**Port 0 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P0	**Port 0 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P0	**Port 0 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P0	**Exponent part of Port 0 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P0	**Mantissa part of Port 0 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001038 MMSCR0_Q7P0 Max-Min Scheduler Control Register 0 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P0				MIN_RATE_CTRL_EXP_Q7_P0					MIN_RATE_CTRL_MAN_Q7_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P0	**Port 0 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P0	**Port 0 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P0	**Exponent part of Port 0 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_	**Mantissa part of Port 0 Queue 7 min. shaper rate limit control**

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	Q7_P0	Value range: 1..127

0000103C MMSCR1_Q7P0 Max-Min Scheduler Control Register 1 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P0				MAX_WEIGHT_Q7_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P0				MAX_RATE_CTRL_EXP_Q7_P0					MAX_RATE_CTRL_MAN_Q7_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P0	**Port 0 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P0	**Port 0 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P0	**Port 0 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P0	**Exponent part of Port 0 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P0	**Mantissa part of Port 0 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001040 ERLCR_P0 Egress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P0			EGC_RATE_CIR_16_P0	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0				EGC_TB_EN_P0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P0	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P0	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps

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		0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P0	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P0	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0	**Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

000010E0 GERLCR Global Egress Rate Limit Control Register 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EGC_MFRM_EX	EGC_IPG_OP	EGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
9	EGC_MFRM_EX	**When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)** 0: Include management frames 1: Exclude management frames
8	EGC_IPG_OP	**Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	EGC_IPG_BYTE	**Egress Rate IPG Byte Count** Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC (default) 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble

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5.2.19 *Special tag format*

Special is used for taking the per-port information to CPU port. It replaces the VLAN tag and inserts the special tag format as below:

Rx:

FUP	UPRI[2:0]			DVP	DRM	VPM[1:0]
PT	SA	DP[5:0]				

Tx:

0	0	0	0	0	0	VPM[1:0]
PT	0	0	0	0	SPN[2:0]	

RX

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	FUP	UPR[2:0]			DVP	DRM	VPM[1:0]	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PT	SA	DP[5:0]					

Bit(s)	Name	Description
15	FUP	**Force PPE user priority**
14:12	UPR	PPE user priority
11	DVP	Disable VALN priority remarking
10	DRM	Disable DSCP priority remarking
9:8	VPM	Tag attribute before special tag insertion; 2'b00 untagged; 2'b01 TPID=8100; 2'b10 TPID=predefined (e.g. 0x9100 or 0x88a8)
7	PT	Pass through
6	SA	Disable SA learning
5:0	DP	Force forwarding port map; all 0 means disable.

TX

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	0	0	0	0	0	0	VPM[1:0]	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PT	0	0	0	0	SPN[2:0]		

Bit(s)	Name	Description
9:8	VPM	Tag attribute before special tag insertion; 2'b00 untagged; 2'b01 TPID=8100; 2'b10 TPID=predefined (e.g. 0x9100 or 0x88a8)
7	PT	Pass through
2:0	SPN	Disable VALN priority remarking Source port number

We show some case here to explain the behavior of special tag:

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RX: PORT_STAG=0, TX: PORT_STAG=1

RX: PORT_STAG=1, TX: PORT_STAG=1

You can enable them at Reg 0x2010,0x2110…etc.., for per-port ability.

00002010 PVC Port VLAN Control of P0 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

5.2.20 *Local port enable*

This is used for debugging not for normal use. It means it would add the self port to the MAC table. So, the same packet would come out from the input port. Set 7th of 0x000c to enable it.

0000000C AGC ARL Global Control 00071819

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	MLDv2_int_en	REV0												ACL_INT	VLAN_INT	ADDR_INT
Type	RW	DC												RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATE_COMP	COMP_BNUM							LOCAL_EN	ARL_PADDING	ACL_MULTI	L2LEN_CHK	CTRL_DROP	VLAN4CPU	ARL_PRI	ALR_RST_N
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1

5.2.21 *System MAC Controller*

GSW build-in the internal MAC. The default MAC is 00000017a501. We put them at 0x30E8 and 0x30E4. You can change the default value as you want.

000030E4 SMACCR0 System MAC Control Register 0 0017A501

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMACCR0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR0[15:0]															
Type	RW															
Reset	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	SMACCR0	**System MAC Address, sys_mac [31:0]. The first 32-bit of system MAC address. It is unique and is specified for pause frame.**

000030E8 SMACCR1 System MAC Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SMACCR1	**System MAC Address, sys_mac [47:32]. The second 16-bit of system MAC address. It is unique and is specified for pause frame.**

5.2.22 *MIB (management information base) counter*

MIB counters are used to record the packet number of ingress and egress port. You can use software reset to clean it. Or write 0x4fe0 as 0 then write 80000000 to restart it.

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MIB counter of port 0:

00004000	TDPC_P0	32	TX Drop Packet Counter of Port 0
00004004	TCRC_P0	32	TX CRC Packet Counter of Port 0
00004008	TUPC_P0	32	TX Unicast Packet Counter of Port 0
0000400C	TMPC_P0	32	TX Multicast Packet Counter of Port 0
00004010	TBPC_P0	32	TX Broadcast Packet Counter of Port 0
00004014	TCEC_P0	32	TX Collision Event Counter of Port 0
00004018	TSCEC_P0	32	TX Single Collision Event Counter of Port 0
0000401C	TMCEC_P0	32	TX Multiple Collision Event Counter of Port 0
00004020	TDEC_P0	32	TX Deferred Event Counter of Port 0
00004024	TLCEC_P0	32	TX Late Collision Event Counter of Port 0
00004028	TXCEC_P0	32	TX excessive Collision Event Counter of Port 0
0000402C	TPPC_P0	32	TX Pause Packet Counter of Port 0
00004030	TL64PC_P0	32	TX packet Length in 64-byte slot Packet Counter of Port 0
00004034	TL65PC_P0	32	TX packet Length in 65-byte slot Packet Counter of Port 0
00004038	TL128PC_P0	32	TX packet Length in 128-byte slot Packet Counter of Port 0
0000403C	TL256PC_P0	32	TX packet Length in 256-byte slot Packet Counter of Port 0
00004040	TL512PC_P0	32	TX packet Length in 512-byte slot Packet Counter of Port 0
00004044	TL1024PC_P0	32	TX packet Length in 1024-byte slot Packet Counter of Port 0
00004048	TOCL_P0	32	TX Octet Counter Low double word of Port 0
0000404C	TOCH_P0	32	TX Octet Counter High double word of Port 0
00004060	RDPC_P0	32	RX Drop Packet Counter of Port 0
00004064	RFPC_P0	32	RX Filtering Packet Counter of Port 0
00004068	RUPC_P0	32	RX Unicast Packet Counter of Port 0
0000406C	RMPC_P0	32	RX Multicast Packet Counter of Port 0
00004070	RBPC_P0	32	RX Broadcast Packet Counter of Port 0
00004074	RAEPC_P0	32	RX Alignment Error Packet Counter of Port 0
00004078	RCEPC_P0	32	RX CRC(FCS) Error Packet Counter of Port 0
0000407C	RUSPC_P0	32	RX Undersize Packet Counter of Port 0
00004080	RFEPC_P0	32	RX Fragment Error Packet Counter of Port 0
00004084	ROSPC_P0	32	RX Oversize Packet Counter of Port 0
00004088	RJEPC_P0	32	RX Jabber Error Packet Counter of Port 0
0000408C	RPPC_P0	32	RX Pause Packet Counter of Port 0
00004090	RL64PC_P0	32	RX packet Length in 64-byte slot Packet Counter of Port 0
00004094	RL65PC_P0	32	RX packet Length in 65-byte slot Packet Counter of Port 0
00004098	RL128PC_P0	32	RX packet Length in 128-byte slot Packet Counter of Port 0
0000409C	RL256PC_P0	32	RX packet Length in 256-byte slot Packet Counter of Port 0
000040A0	RL512PC_P0	32	RX packet Length in 512-byte slot Packet Counter of Port 0
000040A4	RL1024PC_P0	32	RX packet Length in 1024-byte slot Packet Counter of Port 0
000040A8	ROCL_P0	32	RX Octet Counter Low double word of Port 0
000040AC	ROCH_P0	32	Rx Octet Counter High double word of Port 0
000040B0	RDPC_CTRL_P0	32	RX CTRL Drop Packet Counter of Port 0
000040B4	RDPC_ING_P0	32	RX Ingress Drop Packet Counter of Port 0
000040B8	RDPC_ARL_P0	32	RX ARL Drop Packet Counter of Port 0
000040D0	TMIB_HF_STS_P0	32	TX Port MIB Counter Half Full Status of Port 0
000040D4	RMIB_HF_STS_P0	32	RX Port MIB Counter Half Full Status of Port 0

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MIB counter of port 1:

00004100	TDPC_P1	32	TX Drop Packet Counter of Port 1
00004104	TCRC_P1	32	TX CRC Packet Counter of Port 1
00004108	TUPC_P1	32	TX Unicast Packet Counter of Port 1
0000410C	TMPC_P1	32	TX Multicast Packet Counter of Port 1
00004110	TBPC_P1	32	TX Broadcast Packet Counter of Port 1
00004114	TCEC_P1	32	TX Collision Event Counter of Port 1
00004118	TSCEC_P1	32	TX Single Collision Event Counter of Port 1
0000411C	TMCEC_P1	32	TX Multiple Collision Event Counter of Port 1
00004120	TDEC_P1	32	TX Deferred Event Counter of Port 1
00004124	TLCEC_P1	32	TX Late Collision Event Counter of Port 1
00004128	TXCEC_P1	32	TX excessive Collision Event Counter of Port 1
0000412C	TPPC_P1	32	TX Pause Packet Counter of Port 1
00004130	TL64PC_P1	32	TX packet Length in 64-byte slot Packet Counter of Port 1
00004134	TL65PC_P1	32	TX packet Length in 65-byte slot Packet Counter of Port 1
00004138	TL128PC_P1	32	TX packet Length in 128-byte slot Packet Counter of Port 1
0000413C	TL256PC_P1	32	TX packet Length in 256-byte slot Packet Counter of Port 1
00004140	TL512PC_P1	32	TX packet Length in 512-byte slot Packet Counter of Port 1
00004144	TL1024PC_P1	32	TX packet Length in 1024-byte slot Packet Counter of Port 1
00004148	TOCL_P1	32	TX Octet Counter Low double word of Port 1
0000414C	TOCH_P1	32	TX Octet Counter High double word of Port 1
00004160	RDPC_P1	32	RX Drop Packet Counter of Port 1
00004164	RFPC_P1	32	RX Filtering Packet Counter of Port 1
00004168	RUPC_P1	32	RX Unicast Packet Counter of Port 1
0000416C	RMPC_P1	32	RX Multicast Packet Counter of Port 1
00004170	RBPC_P1	32	RX Broadcast Packet Counter of Port 1
00004174	RAEPC_P1	32	RX Alignment Error Packet Counter of Port 1
00004178	RCEPC_P1	32	RX CRC(FCS) Error Packet Counter of Port 1
0000417C	RUSPC_P1	32	RX Undersize Packet Counter of Port 1
00004180	RFEPC_P1	32	RX Fragment Error Packet Counter of Port 1
00004184	ROSPC_P1	32	RX Oversize Packet Counter of Port 1
00004188	RJEPC_P1	32	RX Jabber Error Packet Counter of Port 1
0000418C	RPPC_P1	32	RX Pause Packet Counter of Port 1
00004190	RL64PC_P1	32	RX packet Length in 64-byte slot Packet Counter of Port 1
00004194	RL65PC_P1	32	RX packet Length in 65-byte slot Packet Counter of Port 1
00004198	RL128PC_P1	32	RX packet Length in 128-byte slot Packet Counter of Port 1
0000419C	RL256PC_P1	32	RX packet Length in 256-byte slot Packet Counter of Port 1
000041A0	RL512PC_P1	32	RX packet Length in 512-byte slot Packet Counter of Port 1
000041A4	RL1024PC_P1	32	RX packet Length in 1024-byte slot Packet Counter of Port 1
000041A8	ROCL_P1	32	RX Octet Counter Low double word of Port 1
000041AC	ROCH_P1	32	Rx Octet Counter High double word of Port 1
000041B0	RDPC_CTRL_P1	32	RX CTRL Drop Packet Counter of Port 1
000041B4	RDPC_ING_P1	32	RX Ingress Drop Packet Counter of Port 1
000041B8	RDPC_ARL_P1	32	RX ARL Drop Packet Counter of Port 1
000041D0	TMIB_HF_STS_P1	32	TX Port MIB Counter Half Full Status of Port 1

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000041D4	RMIB_HF_STS_P1	32	RX Port MIB Counter Half Full Status of Port 1

MIB counter of port 2:

00004200	TDPC_P2	32	TX Drop Packet Counter of Port 2
00004204	TCRC_P2	32	TX CRC Packet Counter of Port 2
00004208	TUPC_P2	32	TX Unicast Packet Counter of Port 2
0000420C	TMPC_P2	32	TX Multicast Packet Counter of Port 2
00004210	TBPC_P2	32	TX Broadcast Packet Counter of Port 2
00004214	TCEC_P2	32	TX Collision Event Counter of Port 2
00004218	TSCEC_P2	32	TX Single Collision Event Counter of Port 2
0000421C	TMCEC_P2	32	TX Multiple Collision Event Counter of Port 2
00004220	TDEC_P2	32	TX Deferred Event Counter of Port 2
00004224	TLCEC_P2	32	TX Late Collision Event Counter of Port 2
00004228	TXCEC_P2	32	TX excessive Collision Event Counter of Port 2
0000422C	TPPC_P2	32	TX Pause Packet Counter of Port 2
00004230	TL64PC_P2	32	TX packet Length in 64-byte slot Packet Counter of Port 2
00004234	TL65PC_P2	32	TX packet Length in 65-byte slot Packet Counter of Port 2
00004238	TL128PC_P2	32	TX packet Length in 128-byte slot Packet Counter of Port 2
0000423C	TL256PC_P2	32	TX packet Length in 256-byte slot Packet Counter of Port 2
00004240	TL512PC_P2	32	TX packet Length in 512-byte slot Packet Counter of Port 2
00004244	TL1024PC_P2	32	TX packet Length in 1024-byte slot Packet Counter of Port 2
00004248	TOCL_P2	32	TX Octet Counter Low double word of Port 2
0000424C	TOCH_P2	32	TX Octet Counter High double word of Port 2
00004260	RDPC_P2	32	RX Drop Packet Counter of Port 2
00004264	RFPC_P2	32	RX Filtering Packet Counter of Port 2
00004268	RUPC_P2	32	RX Unicast Packet Counter of Port 2
0000426C	RMPC_P2	32	RX Multicast Packet Counter of Port 2
00004270	RBPC_P2	32	RX Broadcast Packet Counter of Port 2
00004274	RAEPC_P2	32	RX Alignment Error Packet Counter of Port 2
00004278	RCEPC_P2	32	RX CRC(FCS) Error Packet Counter of Port 2
0000427C	RUSPC_P2	32	RX Undersize Packet Counter of Port 2
00004280	RFEPC_P2	32	RX Fragment Error Packet Counter of Port 2
00004284	ROSPC_P2	32	RX Oversize Packet Counter of Port 2
00004288	RJEPC_P2	32	RX Jabber Error Packet Counter of Port 2
0000428C	RPPC_P2	32	RX Pause Packet Counter of Port 2
00004290	RL64PC_P2	32	RX packet Length in 64-byte slot Packet Counter of Port 2
00004294	RL65PC_P2	32	RX packet Length in 65-byte slot Packet Counter of Port 2
00004298	RL128PC_P2	32	RX packet Length in 128-byte slot Packet Counter of Port 2
0000429C	RL256PC_P2	32	RX packet Length in 256-byte slot Packet Counter of Port 2
000042A0	RL512PC_P2	32	RX packet Length in 512-byte slot Packet Counter of Port 2
000042A4	RL1024PC_P2	32	RX packet Length in 1024-byte slot Packet Counter of Port 2
000042A8	ROCL_P2	32	RX Octet Counter Low double word of Port 2
000042AC	ROCH_P2	32	Rx Octet Counter High double word of Port 2
000042B0	RDPC_CTRL_P2	32	RX CTRL Drop Packet Counter of Port 2
000042B4	RDPC_ING_P2	32	RX Ingress Drop Packet Counter of Port 2
000042B8	RDPC_ARL_P2	32	RX ARL Drop Packet Counter of Port 2

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000042D0	TMIB_HF_STS_P2	32	TX Port MIB Counter Half Full Status of Port 2
000042D4	RMIB_HF_STS_P2	32	RX Port MIB Counter Half Full Status of Port 2

MIB counter of port 3:

00004300	TDPC_P3	32	TX Drop Packet Counter of Port 3
00004304	TCRC_P3	32	TX CRC Packet Counter of Port 3
00004308	TUPC_P3	32	TX Unicast Packet Counter of Port 3
0000430C	TMPC_P3	32	TX Multicast Packet Counter of Port 3
00004310	TBPC_P3	32	TX Broadcast Packet Counter of Port 3
00004314	TCEC_P3	32	TX Collision Event Counter of Port 3
00004318	TSCEC_P3	32	TX Single Collision Event Counter of Port 3
0000431C	TMCEC_P3	32	TX Multiple Collision Event Counter of Port 3
00004320	TDEC_P3	32	TX Deferred Event Counter of Port 3
00004324	TLCEC_P3	32	TX Late Collision Event Counter of Port 3
00004328	TXCEC_P3	32	TX excessive Collision Event Counter of Port 3
0000432C	TPPC_P3	32	TX Pause Packet Counter of Port 3
00004330	TL64PC_P3	32	TX packet Length in 64-byte slot Packet Counter of Port 3
00004334	TL65PC_P3	32	TX packet Length in 65-byte slot Packet Counter of Port 3
00004338	TL128PC_P3	32	TX packet Length in 128-byte slot Packet Counter of Port 3
0000433C	TL256PC_P3	32	TX packet Length in 256-byte slot Packet Counter of Port 3
00004340	TL512PC_P3	32	TX packet Length in 512-byte slot Packet Counter of Port 3
00004344	TL1024PC_P3	32	TX packet Length in 1024-byte slot Packet Counter of Port 3
00004348	TOCL_P3	32	TX Octet Counter Low double word of Port 3
0000434C	TOCH_P3	32	TX Octet Counter High double word of Port 3
00004360	RDPC_P3	32	RX Drop Packet Counter of Port 3
00004364	RFPC_P3	32	RX Filtering Packet Counter of Port 3
00004368	RUPC_P3	32	RX Unicast Packet Counter of Port 3
0000436C	RMPC_P3	32	RX Multicast Packet Counter of Port 3
00004370	RBPC_P3	32	RX Broadcast Packet Counter of Port 3
00004374	RAEPC_P3	32	RX Alignment Error Packet Counter of Port 3
00004378	RCEPC_P3	32	RX CRC(FCS) Error Packet Counter of Port 3
0000437C	RUSPC_P3	32	RX Undersize Packet Counter of Port 3
00004380	RFEPC_P3	32	RX Fragment Error Packet Counter of Port 3
00004384	ROSPC_P3	32	RX Oversize Packet Counter of Port 3
00004388	RJEPC_P3	32	RX Jabber Error Packet Counter of Port 3
0000438C	RPPC_P3	32	RX Pause Packet Counter of Port 3
00004390	RL64PC_P3	32	RX packet Length in 64-byte slot Packet Counter of Port 3
00004394	RL65PC_P3	32	RX packet Length in 65-byte slot Packet Counter of Port 3
00004398	RL128PC_P3	32	RX packet Length in 128-byte slot Packet Counter of Port 3
0000439C	RL256PC_P3	32	RX packet Length in 256-byte slot Packet Counter of Port 3
000043A0	RL512PC_P3	32	RX packet Length in 512-byte slot Packet Counter of Port 3
000043A4	RL1024PC_P3	32	RX packet Length in 1024-byte slot Packet Counter of Port 3
000043A8	ROCL_P3	32	RX Octet Counter Low double word of Port 3
000043AC	ROCH_P3	32	Rx Octet Counter High double word of Port 3
000043B0	RDPC_CTRL_P3	32	RX CTRL Drop Packet Counter of Port 3
000043B4	RDPC_ING_P3	32	RX Ingress Drop Packet Counter of Port 3

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000043B8	RDPC_ARL_P3	32	RX ARL Drop Packet Counter of Port 3
000043D0	TMIB_HF_STS_P3	32	TX Port MIB Counter Half Full Status of Port 3
000043D4	RMIB_HF_STS_P3	32	RX Port MIB Counter Half Full Status of Port 3

MIB counter of port 4:

00004400	TDPC_P4	32	TX Drop Packet Counter of Port 4
00004404	TCRC_P4	32	TX CRC Packet Counter of Port 4
00004408	TUPC_P4	32	TX Unicast Packet Counter of Port 4
0000440C	TMPC_P4	32	TX Multicast Packet Counter of Port 4
00004410	TBPC_P4	32	TX Broadcast Packet Counter of Port 4
00004414	TCEC_P4	32	TX Collision Event Counter of Port 4
00004418	TSCEC_P4	32	TX Single Collision Event Counter of Port 4
0000441C	TMCEC_P4	32	TX Multiple Collision Event Counter of Port 4
00004420	TDEC_P4	32	TX Deferred Event Counter of Port 4
00004424	TLCEC_P4	32	TX Late Collision Event Counter of Port 4
00004428	TXCEC_P4	32	TX excessive Collision Event Counter of Port 4
0000442C	TPPC_P4	32	TX Pause Packet Counter of Port 4
00004430	TL64PC_P4	32	TX packet Length in 64-byte slot Packet Counter of Port 4
00004434	TL65PC_P4	32	TX packet Length in 65-byte slot Packet Counter of Port 4
00004438	TL128PC_P4	32	TX packet Length in 128-byte slot Packet Counter of Port 4
0000443C	TL256PC_P4	32	TX packet Length in 256-byte slot Packet Counter of Port 4
00004440	TL512PC_P4	32	TX packet Length in 512-byte slot Packet Counter of Port 4
00004444	TL1024PC_P4	32	TX packet Length in 1024-byte slot Packet Counter of Port 4
00004448	TOCL_P4	32	TX Octet Counter Low double word of Port 4
0000444C	TOCH_P4	32	TX Octet Counter High double word of Port 4
00004460	RDPC_P4	32	RX Drop Packet Counter of Port 4
00004464	RFPC_P4	32	RX Filtering Packet Counter of Port 4
00004468	RUPC_P4	32	RX Unicast Packet Counter of Port 4
0000446C	RMPC_P4	32	RX Multicast Packet Counter of Port 4
00004470	RBPC_P4	32	RX Broadcast Packet Counter of Port 4
00004474	RAEPC_P4	32	RX Alignment Error Packet Counter of Port 4
00004478	RCEPC_P4	32	RX CRC(FCS) Error Packet Counter of Port 4
0000447C	RUSPC_P4	32	RX Undersize Packet Counter of Port 4
00004480	RFEPC_P4	32	RX Fragment Error Packet Counter of Port 4
00004484	ROSPC_P4	32	RX Oversize Packet Counter of Port 4
00004488	RJEPC_P4	32	RX Jabber Error Packet Counter of Port 4
0000448C	RPPC_P4	32	RX Pause Packet Counter of Port 4
00004490	RL64PC_P4	32	RX packet Length in 64-byte slot Packet Counter of Port 4
00004494	RL65PC_P4	32	RX packet Length in 65-byte slot Packet Counter of Port 4
00004498	RL128PC_P4	32	RX packet Length in 128-byte slot Packet Counter of Port 4
0000449C	RL256PC_P4	32	RX packet Length in 256-byte slot Packet Counter of Port 4
000044A0	RL512PC_P4	32	RX packet Length in 512-byte slot Packet Counter of Port 4
000044A4	RL1024PC_P4	32	RX packet Length in 1024-byte slot Packet Counter of Port 4
000044A8	ROCL_P4	32	RX Octet Counter Low double word of Port 4
000044AC	ROCH_P4	32	Rx Octet Counter High double word of Port 4
000044B0	RDPC_CTRL_P4	32	RX CTRL Drop Packet Counter of Port 4

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000044B4	RDPC_ING_P4	32	RX Ingress Drop Packet Counter of Port 4
000044B8	RDPC_ARL_P4	32	RX ARL Drop Packet Counter of Port 4
000044D0	TMIB_HF_STS_P4	32	TX Port MIB Counter Half Full Status of Port 4
000044D4	RMIB_HF_STS_P4	32	RX Port MIB Counter Half Full Status of Port 4

MIB counter of port 5:

00004500	TDPC_P5	32	TX Drop Packet Counter of Port 5
00004504	TCRC_P5	32	TX CRC Packet Counter of Port 5
00004508	TUPC_P5	32	TX Unicast Packet Counter of Port 5
0000450C	TMPC_P5	32	TX Multicast Packet Counter of Port 5
00004510	TBPC_P5	32	TX Broadcast Packet Counter of Port 5
00004514	TCEC_P5	32	TX Collision Event Counter of Port 5
00004518	TSCEC_P5	32	TX Single Collision Event Counter of Port 5
0000451C	TMCEC_P5	32	TX Multiple Collision Event Counter of Port 5
00004520	TDEC_P5	32	TX Deferred Event Counter of Port 5
00004524	TLCEC_P5	32	TX Late Collision Event Counter of Port 5
00004528	TXCEC_P5	32	TX excessive Collision Event Counter of Port 5
0000452C	TPPC_P5	32	TX Pause Packet Counter of Port 5
00004530	TL64PC_P5	32	TX packet Length in 64-byte slot Packet Counter of Port 5
00004534	TL65PC_P5	32	TX packet Length in 65-byte slot Packet Counter of Port 5
00004538	TL128PC_P5	32	TX packet Length in 128-byte slot Packet Counter of Port 5
0000453C	TL256PC_P5	32	TX packet Length in 256-byte slot Packet Counter of Port 5
00004540	TL512PC_P5	32	TX packet Length in 512-byte slot Packet Counter of Port 5
00004544	TL1024PC_P5	32	TX packet Length in 1024-byte slot Packet Counter of Port 5
00004548	TOCL_P5	32	TX Octet Counter Low double word of Port 5
0000454C	TOCH_P5	32	TX Octet Counter High double word of Port 5
00004560	RDPC_P5	32	RX Drop Packet Counter of Port 5
00004564	RFPC_P5	32	RX Filtering Packet Counter of Port 5
00004568	RUPC_P5	32	RX Unicast Packet Counter of Port 5
0000456C	RMPC_P5	32	RX Multicast Packet Counter of Port 5
00004570	RBPC_P5	32	RX Broadcast Packet Counter of Port 5
00004574	RAEPC_P5	32	RX Alignment Error Packet Counter of Port 5
00004578	RCEPC_P5	32	RX CRC(FCS) Error Packet Counter of Port 5
0000457C	RUSPC_P5	32	RX Undersize Packet Counter of Port 5
00004580	RFEPC_P5	32	RX Fragment Error Packet Counter of Port 5
00004584	ROSPC_P5	32	RX Oversize Packet Counter of Port 5
00004588	RJEPC_P5	32	RX Jabber Error Packet Counter of Port 5
0000458C	RPPC_P5	32	RX Pause Packet Counter of Port 5
00004590	RL64PC_P5	32	RX packet Length in 64-byte slot Packet Counter of Port 5
00004594	RL65PC_P5	32	RX packet Length in 65-byte slot Packet Counter of Port 5
00004598	RL128PC_P5	32	RX packet Length in 128-byte slot Packet Counter of Port 5
0000459C	RL256PC_P5	32	RX packet Length in 256-byte slot Packet Counter of Port 5
000045A0	RL512PC_P5	32	RX packet Length in 512-byte slot Packet Counter of Port 5
000045A4	RL1024PC_P5	32	RX packet Length in 1024-byte slot Packet Counter of Port 5
000045A8	ROCL_P5	32	RX Octet Counter Low double word of Port 5
000045AC	ROCH_P5	32	Rx Octet Counter High double word of Port 5

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000045B0	RDPC_CTRL_P5	32	RX CTRL Drop Packet Counter of Port 5
000045B4	RDPC_ING_P5	32	RX Ingress Drop Packet Counter of Port 5
000045B8	RDPC_ARL_P5	32	RX ARL Drop Packet Counter of Port 5
000045D0	TMIB_HF_STS_P5	32	TX Port MIB Counter Half Full Status of Port 5
000045D4	RMIB_HF_STS_P5	32	RX Port MIB Counter Half Full Status of Port 5

MIB counter of port 6:

00004600	TDPC_P6	32	TX Drop Packet Counter of Port 6
00004604	TCRC_P6	32	TX CRC Packet Counter of Port 6
00004608	TUPC_P6	32	TX Unicast Packet Counter of Port 6
0000460C	TMPC_P6	32	TX Multicast Packet Counter of Port 6
00004610	TBPC_P6	32	TX Broadcast Packet Counter of Port 6
00004614	TCEC_P6	32	TX Collision Event Counter of Port 6
00004618	TSCEC_P6	32	TX Single Collision Event Counter of Port 6
0000461C	TMCEC_P6	32	TX Multiple Collision Event Counter of Port 6
00004620	TDEC_P6	32	TX Deferred Event Counter of Port 6
00004624	TLCEC_P6	32	TX Late Collision Event Counter of Port 6
00004628	TXCEC_P6	32	TX excessive Collision Event Counter of Port 6
0000462C	TPPC_P6	32	TX Pause Packet Counter of Port 6
00004630	TL64PC_P6	32	TX packet Length in 64-byte slot Packet Counter of Port 6
00004634	TL65PC_P6	32	TX packet Length in 65-byte slot Packet Counter of Port 6
00004638	TL128PC_P6	32	TX packet Length in 128-byte slot Packet Counter of Port 6
0000463C	TL256PC_P6	32	TX packet Length in 256-byte slot Packet Counter of Port 6
00004640	TL512PC_P6	32	TX packet Length in 512-byte slot Packet Counter of Port 6
00004644	TL1024PC_P6	32	TX packet Length in 1024-byte slot Packet Counter of Port 6
00004648	TOCL_P6	32	TX Octet Counter Low double word of Port 6
0000464C	TOCH_P6	32	TX Octet Counter High double word of Port 6
00004660	RDPC_P6	32	RX Drop Packet Counter of Port 6
00004664	RFPC_P6	32	RX Filtering Packet Counter of Port 6
00004668	RUPC_P6	32	RX Unicast Packet Counter of Port 6
0000466C	RMPC_P6	32	RX Multicast Packet Counter of Port 6
00004670	RBPC_P6	32	RX Broadcast Packet Counter of Port 6
00004674	RAEPC_P6	32	RX Alignment Error Packet Counter of Port 6
00004678	RCEPC_P6	32	RX CRC(FCS) Error Packet Counter of Port 6
0000467C	RUSPC_P6	32	RX Undersize Packet Counter of Port 6
00004680	RFEPC_P6	32	RX Fragment Error Packet Counter of Port 6
00004684	ROSPC_P6	32	RX Oversize Packet Counter of Port 6
00004688	RJEPC_P6	32	RX Jabber Error Packet Counter of Port 6
0000468C	RPPC_P6	32	RX Pause Packet Counter of Port 6
00004690	RL64PC_P6	32	RX packet Length in 64-byte slot Packet Counter of Port 6
00004694	RL65PC_P6	32	RX packet Length in 65-byte slot Packet Counter of Port 6
00004698	RL128PC_P6	32	RX packet Length in 128-byte slot Packet Counter of Port 6
0000469C	RL256PC_P6	32	RX packet Length in 256-byte slot Packet Counter of Port 6
000046A0	RL512PC_P6	32	RX packet Length in 512-byte slot Packet Counter of Port 6
000046A4	RL1024PC_P6	32	RX packet Length in 1024-byte slot Packet Counter of Port 6

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000046A8	ROCL_P6	32	RX Octet Counter Low double word of Port 6
000046AC	ROCH_P6	32	Rx Octet Counter High double word of Port 6
000046B0	RDPC_CTRL_P6	32	RX CTRL Drop Packet Counter of Port 6
000046B4	RDPC_ING_P6	32	RX Ingress Drop Packet Counter of Port 6
000046B8	RDPC_ARL_P6	32	RX ARL Drop Packet Counter of Port 6
000046D0	TMIB_HF_STS_P6	32	TX Port MIB Counter Half Full Status of Port 6
000046D4	RMIB_HF_STS_P6	32	RX Port MIB Counter Half Full Status of Port 6

5.2.23 *GPHY Register*

Module name: gphy_all Base address: (+0h)

Address	Name	Width	Register Function
0000	Reg00h	16	Mode Control Register
0001	Reg01h	16	Mode Status Register
0002	Reg02h	16	PHY Identifier 1 Register
0003	Reg03h	16	PHY Identifier 2 Register
0004	Reg04h	16	Auto-Negotiation Advertisement Register
0005	Reg05h	16	Auto-Negotiation Link Partner Ability Register
0006	Reg06h	16	Auto-Negotiation Expansion Register
0007	Reg07h	16	Auto-Negotiation Next Page Transmit Register
0008	Reg08h	16	Auto-Negotiation LP Next Page Receive Register
0009	Reg09h	16	1000BASE-T Control Register
000A	Reg0Ah	16	1000BASE-T Status Register
000D	Reg0dh	16	MMD access control Register
000E	Reg0eh	16	MMD access address data Register
000F	Reg0Fh	16	1000BASE-T Status Extension 1 Register

0000 Reg00h Mode Control Register 1040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MainReset	Loopback	MrForceSpeedSelInt_0	MrAutonegEnableSMIInt	Pwdn	Isolate Int	MrRestartAutoneg	MrDuplexModeInt	MrCollisionTestEn	MrForceSpeedSelInt_1						
Type	RW_SC	RW	RW	RW	RW	RW	RW_SC	RW	RW	RW						
Reset	0	0	0	1	0	0	0	0	0	1						

Bit(s)	Name	Description
15	MainReset	**Software Reset** 0: Reset de-asserted 1: Reset asserted
14	Loopback	**Loopback** 0: Loopback disabled 1: Loopback enabled
13	MrForceSpeedSelInt_0	**Forced Speed Selection [LSB]MSB = bit6, LSB = bit1300: 10Mbps01: 100Mbps10: 1000Mbps11: Reserved**
12	MrAutonegEnableSMIInt	**Auto-negotiation Enable**

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		0: Auto-negotiation disabled. 1: Auto-negotiation enabled
11	Pwdn	**Power-down** 0: No effect 1: RGMII in-band signaling does not function
10	IsolateInt	**Isolate** 0: No effect 1: Disable MAC interface outputs and ignore MAC interface inputs
9	MrRestartAutoneg	**Restart Auto-nogotiation** 0: No effect 1: Restart auto-negotiation
8	MrDuplexModeInt	**Duplex** 0: Half-duplex 1: Full-duplex
7	MrCollisionTestEn	**Collision Test Enable** 0: No effect 1: Collision Test enabled
6	MrForceSpeedSelInt_1	**Forced Speed Selection [MSB]See bit 13 above**

0001 **Reg01h** **Mode Status Register** **7949**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAP_100T4	CAP_100X_FDX	CAP_100X_HDX	CAP_10T_FDX	CAP_10T_HDX	CAP_100T2_FDX	CAP_100T2_HDX	EXT_STA_EN		PRAM_SUP_CAP	MrAutonegComplete_RefClk	RemoteFault_RefClk	AN_CAP	LinkStatus	JabberActiveStateBit_sp_refclk	EXT_CAP
Type	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO
Reset	0	1	1	1	1	0	0	1		1	0	0	1	0	0	1

Bit(s)	Name	Description
15	CAP_100T4	**100BASE-T4 Capability** 0: Not 100BASE-T4 capable 1: 100BASE-T4 capable
14	CAP_100X_FDX	**100BASE-X FDX Capability** 0: Not 100BASE-X FDX capable 1: 100BASE-X FDX capable
13	CAP_100X_HDX	**100BASE-X HDX Capability** 0: Not 100BASE-X HDX capable 1: 100BASE-X HDX capable
12	CAP_10T_FDX	**10BASE-T FDX Capability** 0: Not 10BASE-T FDX capable 1: 10BASE-T FDX capable
11	CAP_10T_HDX	**10BASE-T HDX Capability** 0: Not 10BASE-T HDX capable 1: 10BASE-T HDX capable

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10	CAP_100T2_FDX	**100BASE-T2 FDX Capability** 0: Not 100BASE-T2 FDX capable 1: 100BASE-T2 FDX capable
9	CAP_100T2_HDX	**100BASE-T2 HDX Capability** 0: Not 100BASE-T2 HDX capable 1: 100BASE-T2 HDX capable
8	EXT_STA_EN	**Extended Status Enable** 0: No effect 1: Extended status information present in register 15
6	PRAM_SUP_CAP	**Preamble Suppression Capability** 0: MF always required 1: MF preamble may be suppressed
5	MrAutonegComplete_RefClk	**Auto-negotiation Complete** 0: Auto-negotiation not complete 1: Auto-negotiation complete
4	RemoteFault_RefClk	**Remote Fault** 0: Far-end fault not detected 1: Far-end fault detected
3	AN_CAP	**Auto-negotiation Capability** 0: Auto-negotiation not capable 1: Auto-negotiation capable
2	LinkStatus	**Link Status** 0: Link is not up 1: Link is up
1	JabberActiveStateBit_sp_refclk	**Jabber Detect** 0: Jabber condition not detected 1: Jabber condition detected
0	EXT_CAP	**Extended Capability** 0: Extended register not capable 1: Extended register capable

0002 Reg02h PHY Identifier 1 Register 03A2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUI_I															
Type	RO															
Reset	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0

Bit(s)	Name	Description
15:0	OUI_I	**Organizationally Unique Identifier [3:18]OUI bit 3 to bit 18**

0003 Reg03h PHY Identifier 2 Register A411

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUI_u						PartNumber						RevCode			
Type	RO						RO						RO			

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Reset	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
15:10	OUI_u	**Organizationally Unique Identifier [19:24]OUI bit 19 to bit 24**
9:4	PartNumber	**Part Number**
3:0	RevCode	**Revision Code**

0004 Reg04h Auto-Negotiation Advertisement Register 05E1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NextPageReq		SmiRf_CL28		Pause		AdvCap100T4	AdvCap100FDX	AdvCap100HDX	AdvCap10FDX	AdvCap10HDX	AdvSelector				
Type	RW		A0		RW		RW	RW	RW	RW	RW	RW				
Reset	0		0		0	1	0	1	1	1	1	0	0	0	0	1

Bit(s)	Name	Description
15	NextPageReq	**Next Page Transmission Request** 0: Request disabled 1: Request enabled
13	SmiRf_CL28	**Transmit Remote Fault** 0: Disabled 1: Enabled
11:10	Pause	**Advertise Asynchronous Pause**
9	AdvCap100T4	**Advertise 100BASE-T4** 0: No effect 1: Advertises 100BASE-T4
8	AdvCap100FDX	**Advertise 100BASE-TX FDX** 0: No effect 1: Advertise 100BASE-TX FDX
7	AdvCap100HDX	**Advertise 100BASE-TX HDX** 0: No effect 1: Advertise 100BASE-TX HDX
6	AdvCap10FDX	**Advertise 10BASE-T FDX** 0: No effect 1: Advertise 10BASE-T FDX
5	AdvCap10HDX	**Advertise 10BASE-T HDX** 0: No effect 1: Advertise 10BASE-T HDX
4:0	AdvSelector	**Advertise Selector** 5'h00: Reserved for future Auto-negotiation development 5'h01: IEEE Std 802.3 5'h02: IEEE Std 802.9 ISLAN-16T 5'h1F: Reserved for future Auto-negotiation development

0005 Reg05h Auto-Negotiation Link Partner Ability Register 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LpNextPageTxReq_RefClk	Lp_Ack_RefClk	LpCapRF_final_RefClk	LpReservedTech_RefClk	LpCapPause_RefClk		LpCap100T4_RefClk	LpCap100FDX_RefClk	LpCap100HDX_RefClk	LpCap10FDX_RefClk	LpCap10HDX_RefClk	LpSelector_RefClk				
Type	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	LpNextPageTxReq_RefClk	**LP Next Page Transmission Request** 0: Not Requested 1: Requested
14	Lp_Ack_RefClk	**LP Acknowledge** 0: No effect 1: Acknowledge
13	LpCapRF_final_RefClk	**LP Remote Fault** 0: No effect 1: Remote fault
12	LpReservedTech_RefClk	**LP Reserved TechnologiesReserved for future technology**
11:10	LpCapPause_RefClk	**LP Advertise Asynchronous Pause**
9	LpCap100T4_RefClk	**LP Advertise 100BASE-T4** 0: No effect 1: Capable of 100BASE-T4
8	LpCap100FDX_RefClk	**LP Advertise 100BASE-TX FDX** 0: No effect 1: Capable of 100BASE-TX FDX
7	LpCap100HDX_RefClk	**LP Advertise 100BASE-TX HDX** 0: No effect 1: Capable of 100BASE-TX HDX
6	LpCap10FDX_RefClk	**LP Advertise 10BASE-T FDX** 0: No effect 1: Capable of 10BASE-T FDX
5	LpCap10HDX_RefClk	**LP Advertise 10BASE-T HDX** 0: No effect 1: Capable of 10BASE-T HDX
4:0	LpSelector_RefClk	**LP Advertise Selector** 5'h00: Reserved for future Auto-negotiation development 5'h01: IEEE Std 802.3 5'h02: IEEE Std 802.9 ISLAN-16T 5'h1F: Reserved for future Auto-negotiation development

0006 Reg06h Auto-Negotiation Expansion Register 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MrParallelDetectFault_RefClk	MrLpNpAble_RefClk	MrNpAble	MrNewPageRxSMI	MrLpAutonegAble_RefClk
Type												RO	RO	RO	RC	RO

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Reset												0	0	1	0	0

Bit(s)	Name	Description
4	MrParallelDetectFault_RefClk	**Parallel Detection Fault** 0: No effect 1: Parallel detection fault
3	MrLpNpAble_RefClk	**LP Next Page Capable** 0: No effect 1: LP is next page capable
2	MrNpAble	**Local PHY Next Page Capable** 0: No effect 1: Local PHY is next page capable
1	MrNewPageRxSMI	**Page Received** 0: No effect 1: New page has been received
0	MrLpAutonegAble_RefClk	**LP Auto-negotiation Capable** 0: No effect 1: LP is capable of auto-negotiation

0007 Reg07h Auto-Negotiation Next Page Transmit Register 2001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**NP**		**MSG_PG**	**ACK2**	**MrToggleTx_RefClk**	**MSG_UF_CODE**										
Type	RW		RW	RW	RO	RW										
Reset	0		1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	NP	**Next Page** 0: No effect 1: More pages follow
13	MSG_PG	**Message Page** 0: Unformatted page 1: Message page
12	ACK2	**Acknowledge 2** 0: Cannot comply with request. 1: Complies with request
11	MrToggleTx_RefClk	**Toggle** 0: Previous transmitted LCW = 1 (LCW: Link Code Word) 1: Previous transmitted LCW = 0
10:0	MSG_UF_CODE	**Message/unformatted CodeContent of message/unformatted page**

0008 Reg08h Auto-Negotiation LP Next Page Receive Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	LP_NP	LP_ACK	LP_MSG	LP_ACK2	LP_MrToggle	LP_MSG_UF_CODE										
Type	RO	RO	RO	RO	RO	RO										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	LP_NP	**LP Next Page** 0: No effect 1: More pages follow
14	LP_ACK	**Acknowledge** 0: No effect 1: LP acknowledge
13	LP_MSG	**LP Message Page** 0: Unformatted page 1: Message page
12	LP_ACK2	**LP Acknowledge 2** 0: LP cannot comply with request 1: LP complies with request
11	LP_MrToggle	**LP Toggle** 0: Previous transmitted LCW = 1 (LCW: Link Code Word) 1: Previous transmitted LCW = 0
10:0	LP_MSG_UF_CODE	**LP Message /unformatted CodeContent of message/unformatted page**

0009 Reg09h 1000BASE-T Control Register 0600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_test_mode			MSConfEnInt	MSConfValInt	port_type	AdvCap1000FDX	AdvCap1000HDX								
Type	RW			RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	1	1	0								

Bit(s)	Name	Description
15:13	tx_test_mode	**Transmitter test mode** 000: Normal 001: Mode 1: Transmit waveform test 010: Mode 2: Transmit jitter test as master 011: Mode 3: Transmit jitter test as slave 100: Mode 4: Transmitter distortion test 101-111: Reserved: Operation not defined
12	MSConfEnInt	**Master/Slave manual configuration** 0: No effect 1: Master/Slave manual configuration enabled
11	MSConfValInt	**Master/Slave value (This register is only valid when bit 9.12 is set to 1)** 0: Configure PHY as slave during negotiation

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		1: Configure PHY as master during negotiation
10	port_type	**Port type** 0: Single port device 1: Multi port device
9	AdvCap1000FDX	**1000BASE-T FDX capability** 0: No effect 1: PHY is 1000BASE-T FDX capable
8	AdvCap1000HDX	**1000BASE-T HDX capability** 0: No effect 1: PHY is 1000BASE-T HDX capable

000A Reg0Ah 1000BASE-T Status Register 4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MrMSConfigFault_RefClk	MSConfig1000_RefClk	LocRcvrStatus1000_RefClk	RemRcvrStatus1000_RefClk	LpCap1000FDX_RefClk	LpCap1000HDX_RefClk			IdleErrCount1000_RefClk							
Type	RO	RO	RO	RO	RO	RO			RO							
Reset	0	1	0	0	0	0			0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	MrMSConfigFault_RefClk	**Master/Slave configuration fault (This bit latches high)** 0: No master/slave configuration fault detected 1: Master/Slave configuration fault detected
14	MSConfig1000_RefClk	**Master/Slave configuration resolution** 0: Local PHY configuration resolved to slave 1: Local PHY configuration resolved to master
13	LocRcvrStatus1000_RefClk	**Local receiver status** 0: Local receiver not OK 1: Local receiver OK
12	RemRcvrStatus1000_RefClk	**Remote receiver status** 0: Remote receiver not OK 1: Remote receiver OK
11	LpCap1000FDX_RefClk	**LP 1000BASE-T FDX capability** 0: LP 1000BASE-T No FDX capable 1: LP 1000BASE-T FDX capable
10	LpCap1000HDX_RefClk	**LP 1000BASE-T HDX capability** 0: LP 1000BASE-T No HDX capable 1: LP 1000BASE-T HDX capable
7:0	IdleErrCount1000_RefClk	**Idle error count**

000D Reg0dh MMD access control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mmd_op_mo											devAddr_c22				

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	de															
Type	RW											RW				
Reset	0	0										0	0	0	0	0

Bit(s)	Name	Description
15:14	mmd_op_mode	**13.1513.14** 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only
4:0	devAddr_c22	**Device address**

000E Reg0eh MMD access address data Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mmd_addr_data															
Type	Other															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	mmd_addr_data	**If 13.15:14 = 00, MMD DEVAD address register.** Otherwise, MMD DEVAD data register as indicated by the contents of its address register 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only

000F Reg0Fh 1000BASE-T Status Extension 1 Register 3000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GIGA_X_FDX_CAP	GIGA_X_HDX_CAP	GIGA_T_FDX_CAP	GIGA_T_HDX_CAP												
Type	RO	RO	RO	RO												
Reset	0	0	1	1												

Bit(s)	Name	Description
15	GIGA_X_FDX_CAP	**1000BASE-X FDX capability** 0: No 1000BASE-X FDX capability 1: PHY is 1000BASE-X FDX capability
14	GIGA_X_HDX_CAP	**1000BASE-X HDX capability** 0: No 1000BASE-X HDX capability 1: PHY is 1000BASE-X HDX capability
13	GIGA_T_FDX_CAP	**1000BASE-T FDX capability** 0: No 1000BASE-X FDX capability 1: PHY is 1000BASE-T FDX capability
12	GIGA_T_HDX_CAP	**1000BASE-T HDX capability** 0: No 1000BASE-X HDX capability 1: PHY is 1000BASE-T HDX capability

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5.3 Annex

5.3.1 User Port

The user port is the default VLAN port. The incoming VLAN-tagged frame is stripped by the outer tag despite the following inner tags. Per untagged or priority-tagged frame, PVID is treated as VID1 tag. At the same time, VID1 is used to look for VLAN table to get the FID and Service tag for VID0. When a new Source MAC address is learned, the VID1 will also be learned on the MAC table.
On the TX_CTRL side, each frame carries 2*N-port egress control bits on per-port based. Bit0 indicates whether this frame carries VID 0 or not; similarly, Bit.1 is for VID1. Once "Consistent tag" is set, the egress tag format will follow the ingress tag format.

VLAN Tag Process on User Port

5.3.2 Translation Port

The translation port is designated for 1:1 or N:1 VLAN aggregation according to CHINA TELECOM EPON requirement. When an incoming frame is received on the translation port, the corresponding custom VID will be found from MAC table, and then the CVID will be the VID for VLAN table.
In the uploading direction, several custom VIDs can be translated into one service VID from the VLAN table which is carried on VID0. When this frame is transmitted from the translation port, etag_ctrl[1:0] will be 2'b01 (Swap), and the service VID will appear on the egress frame.

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VLAN Tag Process on Translation Port

5.3.3 *Transparent Port*

When the port is chosen as transparent port, the VLAN tags on the incoming will be ignored and treated as un-tagged frames. VID0 and VID1 will store PVID as the default VID which is used to look up the VLAN table. On the egress side, TX_CTRL can accept "UNTAG" control to send the original frame.

VLAN Tag Process on Transparent Port

5.3.4 *Security mode*

Enable 802.1Q VLAN for all the received frames.
Discard received frame due to ingress membership violation (interrupt CPU)

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Discard received frames once if VID is missed on the VLAN table (interrupt CPU)

5.3.5 *Check mode*

Enable 802.1Q function for all the received frames.

Don't discard received frame due to ingress membership violation

Discard received frames once if VID is missed on the VLAN table (interrupt CPU)

5.3.6 *Fallback mode*

Enable 802.1Q function for all the received frames.
Don't discard received frame due to ingress membership violation
Frames whose VID is missed on the VLAN table will be filtered by the Port Matrix Member

5.3.7 *Port Matrix mode*

802.1Q function disables (VLAN Security and VLAN Filter Table)
Frames filtered by the Port Matrix Member

5.4 Register Definition

Module Name: SWITCH Base address: (+0h)

Address	Name	Width	Register Function
00000000	MISC0	32	MISC 0
00000004	MISC1	32	MISC 1
00000008	AISR	32	ACL Interrupt Status
0000000C	AGC	32	ARL Global Control
00000010	MFC	32	MAC Forward Control
00000014	VTC	32	VLAN TAG Control
00000018	ISC	32	IGMP Snooping Control
0000001C	IMC	32	IGMP/MLD Message Control
00000020	APC	32	ARP and PPPoE Control
00000024	BPC	32	BPDU and PAE Control
00000028	RGAC1	32	REV_01 and REV_02 Control
0000002C	RGAC2	32	REV_03 and REV_0E Control
00000030	RGAC3	32	REV_10 and REV_20 Control
00000034	RGAC4	32	REV_21 and REV_UN Control
00000038	PMC	32	Protocol Match Control
0000003C	PBG1	32	Protocol Based Group ID-1
00000040	PBG2	32	Protocol Based Group ID-2
00000044	UPW	32	User Priority Weight
00000048	PEM1	32	User Priority Egress Mapping I
0000004C	PEM2	32	User Priority Egress Mapping II
00000050	PEM3	32	DSCP Priority Ingress Mapping VII

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00000054	PEM4	32	User Priority Egress Mapping IV
00000058	PIM1	32	DSCP Priority Ingress Mapping I
0000005C	PIM2	32	DSCP Priority Ingress Mapping II
00000060	PIM3	32	DSCP Priority Ingress Mapping III
00000064	PIM4	32	DSCP Priority Ingress Mapping IV
00000068	PIM5	32	DSCP Priority Ingress Mapping V
0000006C	PIM6	32	DSCP Priority Ingress Mapping VI
00000070	PIM7	32	DSCP Priority Ingress Mapping VII
00000074	ATA1	32	Address Table Access I
00000078	ATA2	32	Address Table Access II
0000007C	ATWD	32	Address Table Write Data
00000080	ATC	32	Address Table Control
00000084	TSRA1	32	Table Search Read Address I
00000088	TSRA2	32	Table Search Read Address II
0000008C	ATRD	32	Address Table Read Data
00000090	VTCR	32	VLAN Table Control
00000094	VAWD1	32	VLAN and ACL Write Data I
00000098	VAWD2	32	VLAN and ACL Write Data II
0000009C	TRTCM	32	Two Rate Three Color Mark
000000A0	AAC	32	Address Age Control
000000A8	AISR_EXT	32	ACL Extension Interrupt Status
000000AC	MISR	32	MLDv2 Interrupt Status
00001000	MMSCR0_Q0P0	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 0
00001004	MMSCR1_Q0P0	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 0
00001008	MMSCR0_Q1P0	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 0
0000100C	MMSCR1_Q1P0	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 0
00001010	MMSCR0_Q2P0	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 0
00001014	MMSCR1_Q2P0	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 0
00001018	MMSCR0_Q3P0	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 0
0000101C	MMSCR1_Q3P0	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 0
00001020	MMSCR0_Q4P0	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 0
00001024	MMSCR1_Q4P0	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 0
00001028	MMSCR0_Q5P0	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 0
0000102C	MMSCR1_Q5P0	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 0
00001030	MMSCR0_Q6P0	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 0
00001034	MMSCR1_Q6P0	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 0
00001038	MMSCR0_Q7P0	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 0
0000103C	MMSCR1_Q7P0	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 0
00001040	ERLCR_P0	32	Egress Rate Limit Control Register of Port 0
000010E0	GERLCR	32	Global Egress Rate Limit Control Register
00001100	MMSCR0_Q0P1	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 1
00001104	MMSCR1_Q0P1	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 1
00001108	MMSCR0_Q1P1	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 1
0000110C	MMSCR1_Q1P1	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 1
00001110	MMSCR0_Q2P1	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 1
00001114	MMSCR1_Q2P1	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 1
00001118	MMSCR0_Q3P1	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 1

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0000111C	MMSCR1_Q3P1	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 1
00001120	MMSCR0_Q4P1	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 1
00001124	MMSCR1_Q4P1	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 1
00001128	MMSCR0_Q5P1	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 1
0000112C	MMSCR1_Q5P1	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 1
00001130	MMSCR0_Q6P1	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 1
00001134	MMSCR1_Q6P1	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 1
00001138	MMSCR0_Q7P1	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 1
0000113C	MMSCR1_Q7P1	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 1
00001140	ERLCR_P1	32	Egress Rate Limit Control Register of Port 1
00001200	MMSCR0_Q0P2	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 2
00001204	MMSCR1_Q0P2	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 2
00001208	MMSCR0_Q1P2	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 2
0000120C	MMSCR1_Q1P2	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 2
00001210	MMSCR0_Q2P2	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 2
00001214	MMSCR1_Q2P2	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 2
00001218	MMSCR0_Q3P2	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 2
0000121C	MMSCR1_Q3P2	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 2
00001220	MMSCR0_Q4P2	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 2
00001224	MMSCR1_Q4P2	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 2
00001228	MMSCR0_Q5P2	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 2
0000122C	MMSCR1_Q5P2	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 2
00001230	MMSCR0_Q6P2	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 2
00001234	MMSCR1_Q6P2	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 2
00001238	MMSCR0_Q7P2	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 2
0000123C	MMSCR1_Q7P2	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 2
00001240	ERLCR_P2	32	Egress Rate Limit Control Register of Port 2
00001300	MMSCR0_Q0P3	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 3
00001304	MMSCR1_Q0P3	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 3
00001308	MMSCR0_Q1P3	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 3
0000130C	MMSCR1_Q1P3	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 3
00001310	MMSCR0_Q2P3	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 3
00001314	MMSCR1_Q2P3	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 3
00001318	MMSCR0_Q3P3	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 3
0000131C	MMSCR1_Q3P3	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 3
00001320	MMSCR0_Q4P3	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 3
00001324	MMSCR1_Q4P3	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 3
00001328	MMSCR0_Q5P3	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 3
0000132C	MMSCR1_Q5P3	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 3
00001330	MMSCR0_Q6P3	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 3
00001334	MMSCR1_Q6P3	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 3
00001338	MMSCR0_Q7P3	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 3
0000133C	MMSCR1_Q7P3	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 3
00001340	ERLCR_P3	32	Egress Rate Limit Control Register of Port 3
00001400	MMSCR0_Q0P4	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 4
00001404	MMSCR1_Q0P4	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 4
00001408	MMSCR0_Q1P4	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 4

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0000140C	MMSCR1_Q1P4	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 4
00001410	MMSCR0_Q2P4	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 4
00001414	MMSCR1_Q2P4	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 4
00001418	MMSCR0_Q3P4	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 4
0000141C	MMSCR1_Q3P4	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 4
00001420	MMSCR0_Q4P4	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 4
00001424	MMSCR1_Q4P4	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 4
00001428	MMSCR0_Q5P4	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 4
0000142C	MMSCR1_Q5P4	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 4
00001430	MMSCR0_Q6P4	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 4
00001434	MMSCR1_Q6P4	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 4
00001438	MMSCR0_Q7P4	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 4
0000143C	MMSCR1_Q7P4	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 4
00001440	ERLCR_P4	32	Egress Rate Limit Control Register of Port 4
00001500	MMSCR0_Q0P5	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 5
00001504	MMSCR1_Q0P5	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 5
00001508	MMSCR0_Q1P5	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 5
0000150C	MMSCR1_Q1P5	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 5
00001510	MMSCR0_Q2P5	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 5
00001514	MMSCR1_Q2P5	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 5
00001518	MMSCR0_Q3P5	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 5
0000151C	MMSCR1_Q3P5	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 5
00001520	MMSCR0_Q4P5	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 5
00001524	MMSCR1_Q4P5	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 5
00001528	MMSCR0_Q5P5	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 5
0000152C	MMSCR1_Q5P5	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 5
00001530	MMSCR0_Q6P5	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 5
00001534	MMSCR1_Q6P5	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 5
00001538	MMSCR0_Q7P5	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 5
0000153C	MMSCR1_Q7P5	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 5
00001540	ERLCR_P5	32	Egress Rate Limit Control Register of Port 5
00001600	MMSCR0_Q0P6	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 6
00001604	MMSCR1_Q0P6	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 6
00001608	MMSCR0_Q1P6	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 6
0000160C	MMSCR1_Q1P6	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 6
00001610	MMSCR0_Q2P6	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 6
00001614	MMSCR1_Q2P6	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 6
00001618	MMSCR0_Q3P6	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 6
0000161C	MMSCR1_Q3P6	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 6
00001620	MMSCR0_Q4P6	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 6
00001624	MMSCR1_Q4P6	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 6
00001628	MMSCR0_Q5P6	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 6
0000162C	MMSCR1_Q5P6	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 6
00001630	MMSCR0_Q6P6	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 6
00001634	MMSCR1_Q6P6	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 6
00001638	MMSCR0_Q7P6	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 6
0000163C	MMSCR1_Q7P6	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 6

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00001640	ERLCR_P6	32	Egress Rate Limit Control Register of Port 6
00001800	IRLCR_P0	32	Ingress Rate Limit Control Register of Port 0
00001804	FPC_RXCTRL_P0	32	Free Page Count at RX_CTRL of Port 0
0000180C	MMDPR_10_Q0P0	32	Drop Precedence control 10 of Q0 Port 0
00001810	MMDPR_10_Q1P0	32	Drop Precedence control 10 of Q1 Port 0
00001814	MMDPR_10_Q2P0	32	Drop Precedence control 10 of Q2 Port 0
00001818	MMDPR_10_Q3P0	32	Drop Precedence control 10 of Q3 Port 0
0000181C	MMDPR_10_Q4P0	32	Drop Precedence control 10 of Q4 Port 0
00001820	MMDPR_10_Q5P0	32	Drop Precedence control 10 of Q5 Port 0
00001824	MMDPR_10_Q6P0	32	Drop Precedence control 10 of Q6 Port 0
00001828	MMDPR_10_Q7P0	32	Drop Precedence control 10 of Q7 Port 0
0000182C	MMDPR_11_Q0P0	32	Drop Precedence control 11 of Q0 Port 0
00001830	MMDPR_11_Q1P0	32	Drop Precedence control 11 of Q1 Port 0
00001834	MMDPR_11_Q2P0	32	Drop Precedence control 11 of Q2 Port 0
00001838	MMDPR_11_Q3P0	32	Drop Precedence control 11 of Q3 Port 0
0000183C	MMDPR_11_Q4P0	32	Drop Precedence control 11 of Q4 Port 0
00001840	MMDPR_11_Q5P0	32	Drop Precedence control 11 of Q5 Port 0
00001844	MMDPR_11_Q6P0	32	Drop Precedence control 11 of Q6 Port 0
00001848	MMDPR_11_Q7P0	32	Drop Precedence control 11 of Q7 Port 0
00001900	IRLCR_P1	32	Ingress Rate Limit Control Register of Port 1
00001904	FPC_RXCTRL_P1	32	Free Page Count at RX_CTRL of Port 1
0000190C	MMDPR_10_Q0P1	32	Drop Precedence control 10 of Q0 Port 1
00001910	MMDPR_10_Q1P1	32	Drop Precedence control 10 of Q1 Port 1
00001914	MMDPR_10_Q2P1	32	Drop Precedence control 10 of Q2 Port 1
00001918	MMDPR_10_Q3P1	32	Drop Precedence control 10 of Q3 Port 1
0000191C	MMDPR_10_Q4P1	32	Drop Precedence control 10 of Q4 Port 1
00001920	MMDPR_10_Q5P1	32	Drop Precedence control 10 of Q5 Port 1
00001924	MMDPR_10_Q6P1	32	Drop Precedence control 10 of Q6 Port 1
00001928	MMDPR_10_Q7P1	32	Drop Precedence control 10 of Q7 Port 1
0000192C	MMDPR_11_Q0P1	32	Drop Precedence control 11 of Q0 Port 1
00001930	MMDPR_11_Q1P1	32	Drop Precedence control 11 of Q1 Port 1
00001934	MMDPR_11_Q2P1	32	Drop Precedence control 11 of Q2 Port 1
00001938	MMDPR_11_Q3P1	32	Drop Precedence control 11 of Q3 Port 1
0000193C	MMDPR_11_Q4P1	32	Drop Precedence control 11 of Q4 Port 1
00001940	MMDPR_11_Q5P1	32	Drop Precedence control 11 of Q5 Port 1
00001944	MMDPR_11_Q6P1	32	Drop Precedence control 11 of Q6 Port 1
00001948	MMDPR_11_Q7P1	32	Drop Precedence control 11 of Q7 Port 1
00001A00	IRLCR_P2	32	Ingress Rate Limit Control Register of Port 2
00001A04	FPC_RXCTRL_P2	32	Free Page Count at RX_CTRL of Port 2
00001A0C	MMDPR_10_Q0P2	32	Drop Precedence control 10 of Q0 Port 2
00001A10	MMDPR_10_Q1P2	32	Drop Precedence control 10 of Q1 Port 2
00001A14	MMDPR_10_Q2P2	32	Drop Precedence control 10 of Q2 Port 2
00001A18	MMDPR_10_Q3P2	32	Drop Precedence control 10 of Q3 Port 2
00001A1C	MMDPR_10_Q4P2	32	Drop Precedence control 10 of Q4 Port 2
00001A20	MMDPR_10_Q5P2	32	Drop Precedence control 10 of Q5 Port 2
00001A24	MMDPR_10_Q6P2	32	Drop Precedence control 10 of Q6 Port 2
00001A28	MMDPR_10_Q7P2	32	Drop Precedence control 10 of Q7 Port 2

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00001A2C	MMDPR_11_Q0P2	32	Drop Precedence control 11 of Q0 Port 2
00001A30	MMDPR_11_Q1P2	32	Drop Precedence control 11 of Q1 Port 2
00001A34	MMDPR_11_Q2P2	32	Drop Precedence control 11 of Q2 Port 2
00001A38	MMDPR_11_Q3P2	32	Drop Precedence control 11 of Q3 Port 2
00001A3C	MMDPR_11_Q4P2	32	Drop Precedence control 11 of Q4 Port 2
00001A40	MMDPR_11_Q5P2	32	Drop Precedence control 11 of Q5 Port 2
00001A44	MMDPR_11_Q6P2	32	Drop Precedence control 11 of Q6 Port 2
00001A48	MMDPR_11_Q7P2	32	Drop Precedence control 11 of Q7 Port 2
00001B00	IRLCR_P3	32	Ingress Rate Limit Control Register of Port 3
00001B04	FPC_RXCTRL_P3	32	Free Page Count at RX_CTRL of Port 3
00001B0C	MMDPR_10_Q0P3	32	Drop Precedence control 10 of Q0 Port 3
00001B10	MMDPR_10_Q1P3	32	Drop Precedence control 10 of Q1 Port 3
00001B14	MMDPR_10_Q2P3	32	Drop Precedence control 10 of Q2 Port 3
00001B18	MMDPR_10_Q3P3	32	Drop Precedence control 10 of Q3 Port 3
00001B1C	MMDPR_10_Q4P3	32	Drop Precedence control 10 of Q4 Port 3
00001B20	MMDPR_10_Q5P3	32	Drop Precedence control 10 of Q5 Port 3
00001B24	MMDPR_10_Q6P3	32	Drop Precedence control 10 of Q6 Port 3
00001B28	MMDPR_10_Q7P3	32	Drop Precedence control 10 of Q7 Port 3
00001B2C	MMDPR_11_Q0P3	32	Drop Precedence control 11 of Q0 Port 3
00001B30	MMDPR_11_Q1P3	32	Drop Precedence control 11 of Q1 Port 3
00001B34	MMDPR_11_Q2P3	32	Drop Precedence control 11 of Q2 Port 3
00001B38	MMDPR_11_Q3P3	32	Drop Precedence control 11 of Q3 Port 3
00001B3C	MMDPR_11_Q4P3	32	Drop Precedence control 11 of Q4 Port 3
00001B40	MMDPR_11_Q5P3	32	Drop Precedence control 11 of Q5 Port 3
00001B44	MMDPR_11_Q6P3	32	Drop Precedence control 11 of Q6 Port 3
00001B48	MMDPR_11_Q7P3	32	Drop Precedence control 11 of Q7 Port 3
00001C00	IRLCR_P4	32	Ingress Rate Limit Control Register of Port 4
00001C04	FPC_RXCTRL_P4	32	Free Page Count at RX_CTRL of Port 4
00001C0C	MMDPR_10_Q0P4	32	Drop Precedence control 10 of Q0 Port 4
00001C10	MMDPR_10_Q1P4	32	Drop Precedence control 10 of Q1 Port 4
00001C14	MMDPR_10_Q2P4	32	Drop Precedence control 10 of Q2 Port 4
00001C18	MMDPR_10_Q3P4	32	Drop Precedence control 10 of Q3 Port 4
00001C1C	MMDPR_10_Q4P4	32	Drop Precedence control 10 of Q4 Port 4
00001C20	MMDPR_10_Q5P4	32	Drop Precedence control 10 of Q5 Port 4
00001C24	MMDPR_10_Q6P4	32	Drop Precedence control 10 of Q6 Port 4
00001C28	MMDPR_10_Q7P4	32	Drop Precedence control 10 of Q7 Port 4
00001C2C	MMDPR_11_Q0P4	32	Drop Precedence control 11 of Q0 Port 4
00001C30	MMDPR_11_Q1P4	32	Drop Precedence control 11 of Q1 Port 4
00001C34	MMDPR_11_Q2P4	32	Drop Precedence control 11 of Q2 Port 4
00001C38	MMDPR_11_Q3P4	32	Drop Precedence control 11 of Q3 Port 4
00001C3C	MMDPR_11_Q4P4	32	Drop Precedence control 11 of Q4 Port 4
00001C40	MMDPR_11_Q5P4	32	Drop Precedence control 11 of Q5 Port 4
00001C44	MMDPR_11_Q6P4	32	Drop Precedence control 11 of Q6 Port 4
00001C48	MMDPR_11_Q7P4	32	Drop Precedence control 11 of Q7 Port 4
00001D00	IRLCR_P5	32	Ingress Rate Limit Control Register of Port 5
00001D04	FPC_RXCTRL_P5	32	Free Page Count at RX_CTRL of Port 5
00001D0C	MMDPR_10_Q0P5	32	Drop Precedence control 10 of Q0 Port 5

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00001D10	MMDPR_10_Q1P5	32	Drop Precedence control 10 of Q1 Port 5
00001D14	MMDPR_10_Q2P5	32	Drop Precedence control 10 of Q2 Port 5
00001D18	MMDPR_10_Q3P5	32	Drop Precedence control 10 of Q3 Port 5
00001D1C	MMDPR_10_Q4P5	32	Drop Precedence control 10 of Q4 Port 5
00001D20	MMDPR_10_Q5P5	32	Drop Precedence control 10 of Q5 Port 5
00001D24	MMDPR_10_Q6P5	32	Drop Precedence control 10 of Q6 Port 5
00001D28	MMDPR_10_Q7P5	32	Drop Precedence control 10 of Q7 Port 5
00001D2C	MMDPR_11_Q0P5	32	Drop Precedence control 11 of Q0 Port 5
00001D30	MMDPR_11_Q1P5	32	Drop Precedence control 11 of Q1 Port 5
00001D34	MMDPR_11_Q2P5	32	Drop Precedence control 11 of Q2 Port 5
00001D38	MMDPR_11_Q3P5	32	Drop Precedence control 11 of Q3 Port 5
00001D3C	MMDPR_11_Q4P5	32	Drop Precedence control 11 of Q4 Port 5
00001D40	MMDPR_11_Q5P5	32	Drop Precedence control 11 of Q5 Port 5
00001D44	MMDPR_11_Q6P5	32	Drop Precedence control 11 of Q6 Port 5
00001D48	MMDPR_11_Q7P5	32	Drop Precedence control 11 of Q7 Port 5
00001E00	IRLCR_P6	32	Ingress Rate Limit Control Register of Port 6
00001E04	FPC_RXCTRL_P6	32	Free Page Count at RX_CTRL of Port 6
00001E0C	MMDPR_10_Q0P6	32	Drop Precedence control 10 of Q0 Port 6
00001E10	MMDPR_10_Q1P6	32	Drop Precedence control 10 of Q1 Port 6
00001E14	MMDPR_10_Q2P6	32	Drop Precedence control 10 of Q2 Port 6
00001E18	MMDPR_10_Q3P6	32	Drop Precedence control 10 of Q3 Port 6
00001E1C	MMDPR_10_Q4P6	32	Drop Precedence control 10 of Q4 Port 6
00001E20	MMDPR_10_Q5P6	32	Drop Precedence control 10 of Q5 Port 6
00001E24	MMDPR_10_Q6P6	32	Drop Precedence control 10 of Q6 Port 6
00001E28	MMDPR_10_Q7P6	32	Drop Precedence control 10 of Q7 Port 6
00001E2C	MMDPR_11_Q0P6	32	Drop Precedence control 11 of Q0 Port 6
00001E30	MMDPR_11_Q1P6	32	Drop Precedence control 11 of Q1 Port 6
00001E34	MMDPR_11_Q2P6	32	Drop Precedence control 11 of Q2 Port 6
00001E38	MMDPR_11_Q3P6	32	Drop Precedence control 11 of Q3 Port 6
00001E3C	MMDPR_11_Q4P6	32	Drop Precedence control 11 of Q4 Port 6
00001E40	MMDPR_11_Q5P6	32	Drop Precedence control 11 of Q5 Port 6
00001E44	MMDPR_11_Q6P6	32	Drop Precedence control 11 of Q6 Port 6
00001E48	MMDPR_11_Q7P6	32	Drop Precedence control 11 of Q7 Port 6
00001F60	PTP_CTRL	32	PTP CONTROL REGISTER
00001F68	TIMESTAMP_LSB	32	TIMESTAMP SECOND COUNTER LSB REGISTER
00001F70	TIMESTAMP_OFFSET_MODE	32	TIMESTAMP OFFSET MODE REGISTER
00001F78	TIMESTAMP_OFFSET_LSB	32	TIMESTAMP SECOND OFFSET LSB REGISTER
00001F90	TIMESTAMP_TFIFO_CTRL	32	TIMESTAMP TX FIFO CONTROL REGISTER
00001F98	TMSTMP_TFIFO_MSB	32	TIMESTAMP TX FIFO MSB REGISTER
00001F9C	TMSTMP_TFIFO_NS	32	TIMESTAMP TX FIFO NS REGISTER
00001FA0	TIMESTAMP_RFIFO_CTRL	32	TIMESTAMP RX FIFO CONTROL REGISTER
00001FA8	TMSTMP_RFIFO_MSB	32	TIMESTAMP RX FIFO MSB REGISTER
00001FAC	TMSTMP_RFIFO_NS	32	TIMESTAMP RX FIFO NS REGISTER
00001FC0	FPLC	32	Free Page Link Count Register

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00001FE0	GFCCR0	32	Global Flow_Control Control Register 0
00001FE4	GFCCR1	32	Global Flow_Control Control Register 1
00001FE8	FCBRCR0	32	Flow Control Block Reservation Control Register for group 0
00001FEC	FCBRCR1	32	Flow Control Block Reservation Control Register for group 1
00001FF0	GIRLCR	32	Global Ingress Rate Limit Control Register
00001FF4	GFCCR2	32	Global Flow_Control Control Register 2
00002000	SSC	32	STP State Control of P0
00002004	PCR	32	Port Control of P0
00002008	PIC	32	Port IGMP Control of P0
0000200C	PSC	32	Port Security Control of P0
00002010	PVC	32	Port VLAN Control of P0
00002014	PPBV1	32	Port-and-Protocol Based VLAN I of P0
00002018	PPBV2	32	Port-and-Protocol Based VLAN II of P0
0000201C	BSR	32	Broadcast Storm Rate Control of P0
00002020	STAG01	32	STAG Index 0/1 of P0
00002024	STAG23	32	STAG Index 2/3 of P0
00002028	STAG45	32	STAG Index 4/5 of P0
0000202C	STAG67	32	STAG Index 6/7 of P0
00002100	SSC	32	STP State Control of P1
00002104	PCR	32	Port Control of P1
00002108	PIC	32	Port IGMP Control of P1
0000210C	PSC	32	Port Security Control of P1
00002110	PVC	32	Port VLAN Control of P1
00002114	PPBV1	32	Port-and-Protocol Based VLAN I of P1
00002118	PPBV2	32	Port-and-Protocol Based VLAN II of P1
0000211C	BSR	32	Broadcast Storm Rate Control of P1
00002120	STAG01	32	STAG Index 0/1 of P1
00002124	STAG23	32	STAG Index 2/3 of P1
00002128	STAG45	32	STAG Index 4/5 of P1
0000212C	STAG67	32	STAG Index 6/7 of P1
00002200	SSC	32	STP State Control of P2
00002204	PCR	32	Port Control of P2
00002208	PIC	32	Port IGMP Control of P2
0000220C	PSC	32	Port Security Control of P2
00002210	PVC	32	Port VLAN Control of P2
00002214	PPBV1	32	Port-and-Protocol Based VLAN I of P2
00002218	PPBV2	32	Port-and-Protocol Based VLAN II of P2
0000221C	BSR	32	Broadcast Storm Rate Control of P2
00002220	STAG01	32	STAG Index 0/1 of P2
00002224	STAG23	32	STAG Index 2/3 of P2
00002228	STAG45	32	STAG Index 4/5 of P2
0000222C	STAG67	32	STAG Index 6/7 of P2
00002300	SSC	32	STP State Control of P3
00002304	PCR	32	Port Control of P3
00002308	PIC	32	Port IGMP Control of P3
0000230C	PSC	32	Port Security Control of P3
00002310	PVC	32	Port VLAN Control of P3

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00002314	PPBV1	32	Port-and-Protocol Based VLAN I of P3
00002318	PPBV2	32	Port-and-Protocol Based VLAN II of P3
0000231C	BSR	32	Broadcast Storm Rate Control of P3
00002320	STAG01	32	STAG Index 0/1 of P3
00002324	STAG23	32	STAG Index 2/3 of P3
00002328	STAG45	32	STAG Index 4/5 of P3
0000232C	STAG67	32	STAG Index 6/7 of P3
00002400	SSC	32	STP State Control of P4
00002404	PCR	32	Port Control of P4
00002408	PIC	32	Port IGMP Control of P4
0000240C	PSC	32	Port Security Control of P4
00002410	PVC	32	Port VLAN Control of P4
00002414	PPBV1	32	Port-and-Protocol Based VLAN I of P4
00002418	PPBV2	32	Port-and-Protocol Based VLAN II of P4
0000241C	BSR	32	Broadcast Storm Rate Control of P4
00002420	STAG01	32	STAG Index 0/1 of P4
00002424	STAG23	32	STAG Index 2/3 of P4
00002428	STAG45	32	STAG Index 4/5 of P4
0000242C	STAG67	32	STAG Index 6/7 of P4
00002500	SSC	32	STP State Control of P5
00002504	PCR	32	Port Control of P5
00002508	PIC	32	Port IGMP Control of P5
0000250C	PSC	32	Port Security Control of P5
00002510	PVC	32	Port VLAN Control of P5
00002514	PPBV1	32	Port-and-Protocol Based VLAN I of P5
00002518	PPBV2	32	Port-and-Protocol Based VLAN II of P5
0000251C	BSR	32	Broadcast Storm Rate Control of P5
00002520	STAG01	32	STAG Index 0/1 of P5
00002524	STAG23	32	STAG Index 2/3 of P5
00002528	STAG45	32	STAG Index 4/5 of P5
0000252C	STAG67	32	STAG Index 6/7 of P5
00002600	SSC	32	STP State Control of P6
00002604	PCR	32	Port Control of P6
00002608	PIC	32	Port IGMP Control of P6
0000260C	PSC	32	Port Security Control of P6
00002610	PVC	32	Port VLAN Control of P6
00002614	PPBV1	32	Port-and-Protocol Based VLAN I of P6
00002618	PPBV2	32	Port-and-Protocol Based VLAN II of P6
0000261C	BSR	32	Broadcast Storm Rate Control of P6
00002620	STAG01	32	STAG Index 0/1 of P6
00002624	STAG23	32	STAG Index 2/3 of P6
00002628	STAG45	32	STAG Index 4/5 of P6
0000262C	STAG67	32	STAG Index 6/7 of P6
00003000	PMCR_P0	32	PORT 0 MAC Control Register
00003004	PMEEECR_P0	32	PORT 0 MAC EEE Control Register
00003008	PMSR_P0	32	PORT 0 MAC Status Register
00003010	PINT_EN_P0	32	PORT 0 Interrupt Enable Register

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00003014	PINT_STS_P0	32	PORT 0 Interrupt Status Register
00003018	DBG_CNT	32	PORT 0 DEBUG COUNT
000030C0	LPDET_CTRL	32	LOOP DETECTION CONTROL REGISTER
000030C8	LPDET_SA_MSB	32	LOOP DETECTION SA MSB
000030CC	LPDET_SA_LSB	32	LOOP DETECTION SA LSB
000030D0	LPDET_RXSA_MSB	32	LOOP DETECTION RX SA MSB
000030E0	GMACCR	32	Global MAC Control Register
000030E4	SMACCR0	32	System MAC Control Register 0
000030E8	SMACCR1	32	System MAC Control Register 1
000030F0	CKGCR	32	Clock Gating Control Register
000030F4	GPINT_EN	32	Global Port Interrupt Enable Register
000030F8	GPINT_STS	32	Global Port Interrupt Status Register
00003100	PMCR_P1	32	PORT 1 MAC Control Register
00003104	PMEEECR_P1	32	PORT 1 MAC EEE Control Register
00003108	PMSR_P1	32	PORT 1 MAC Status Register
00003110	PINT_EN_P1	32	PORT 1 Interrupt Enable Register
00003114	PINT_STS_P1	32	PORT 1 Interrupt Status Register
00003118	DBG_CNT	32	PORT 1 DEBUG COUNT
00003200	PMCR_P2	32	PORT 2 MAC Control Register
00003204	PMEEECR_P2	32	PORT 2 MAC EEE Control Register
00003208	PMSR_P2	32	PORT 2 MAC Status Register
00003210	PINT_EN_P2	32	PORT 2 Interrupt Enable Register
00003214	PINT_STS_P2	32	PORT 2 Interrupt Status Register
00003218	DBG_CNT	32	PORT 2 DEBUG COUNT
00003300	PMCR_P3	32	PORT 3 MAC Control Register
00003304	PMEEECR_P3	32	PORT 3 MAC EEE Control Register
00003308	PMSR_P3	32	PORT 3 MAC Status Register
00003310	PINT_EN_P3	32	PORT 3 Interrupt Enable Register
00003314	PINT_STS_P3	32	PORT 3 Interrupt Status Register
00003318	DBG_CNT	32	PORT 3 DEBUG COUNT
00003400	PMCR_P4	32	PORT 4 MAC Control Register
00003404	PMEEECR_P4	32	PORT 4 MAC EEE Control Register
00003408	PMSR_P4	32	PORT 4 MAC Status Register
00003410	PINT_EN_P4	32	PORT 4 Interrupt Enable Register
00003414	PINT_STS_P4	32	PORT 4 Interrupt Status Register
00003418	DBG_CNT	32	PORT 4 DEBUG COUNT
00003500	PMCR_P5	32	PORT 5 MAC Control Register
00003504	PMEEECR_P5	32	PORT 5 MAC EEE Control Register
00003508	PMSR_P5	32	PORT 5 MAC Status Register
00003510	PINT_EN_P5	32	PORT 5 Interrupt Enable Register
00003514	PINT_STS_P5	32	PORT 5 Interrupt Status Register
00003518	DBG_CNT	32	PORT 5 DEBUG COUNT
00003600	PMCR_P6	32	PORT 6 MAC Control Register
00003604	PMEEECR_P6	32	PORT 6 MAC EEE Control Register
00003608	PMSR_P6	32	PORT 6 MAC Status Register
00003610	PINT_EN_P6	32	PORT 6 Interrupt Enable Register
00003614	PINT_STS_P6	32	PORT 6 Interrupt Status Register

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00003618	DBG_CNT	32	PORT 6 DEBUG COUNT
00004000	TDPC_P0	32	TX Drop Packet Counter of Port 0
00004004	TCRC_P0	32	TX CRC Packet Counter of Port 0
00004008	TUPC_P0	32	TX Unicast Packet Counter of Port 0
0000400C	TMPC_P0	32	TX Multicast Packet Counter of Port 0
00004010	TBPC_P0	32	TX Broadcast Packet Counter of Port 0
00004014	TCEC_P0	32	TX Collision Event Counter of Port 0
00004018	TSCEC_P0	32	TX Single Collision Event Counter of Port 0
0000401C	TMCEC_P0	32	TX Multiple Collision Event Counter of Port 0
00004020	TDEC_P0	32	TX Deferred Event Counter of Port 0
00004024	TLCEC_P0	32	TX Late Collision Event Counter of Port 0
00004028	TXCEC_P0	32	TX excessive Collision Event Counter of Port 0
0000402C	TPPC_P0	32	TX Pause Packet Counter of Port 0
00004030	TL64PC_P0	32	TX packet Length in 64-byte slot Packet Counter of Port 0
00004034	TL65PC_P0	32	TX packet Length in 65-byte slot Packet Counter of Port 0
00004038	TL128PC_P0	32	TX packet Length in 128-byte slot Packet Counter of Port 0
0000403C	TL256PC_P0	32	TX packet Length in 256-byte slot Packet Counter of Port 0
00004040	TL512PC_P0	32	TX packet Length in 512-byte slot Packet Counter of Port 0
00004044	TL1024PC_P0	32	TX packet Length in 1024-byte slot Packet Counter of Port 0
00004048	TOCL_P0	32	TX Octet Counter Low double word of Port 0
0000404C	TOCH_P0	32	TX Octet Counter High double word of Port 0
00004060	RDPC_P0	32	RX Drop Packet Counter of Port 0
00004064	RFPC_P0	32	RX Filtering Packet Counter of Port 0
00004068	RUPC_P0	32	RX Unicast Packet Counter of Port 0
0000406C	RMPC_P0	32	RX Multicast Packet Counter of Port 0
00004070	RBPC_P0	32	RX Broadcast Packet Counter of Port 0
00004074	RAEPC_P0	32	RX Alignment Error Packet Counter of Port 0
00004078	RCEPC_P0	32	RX CRC(FCS) Error Packet Counter of Port 0
0000407C	RUSPC_P0	32	RX Undersize Packet Counter of Port 0
00004080	RFEPC_P0	32	RX Fragment Error Packet Counter of Port 0
00004084	ROSPC_P0	32	RX Oversize Packet Counter of Port 0
00004088	RJEPC_P0	32	RX Jabber Error Packet Counter of Port 0
0000408C	RPPC_P0	32	RX Pause Packet Counter of Port 0
00004090	RL64PC_P0	32	RX packet Length in 64-byte slot Packet Counter of Port 0
00004094	RL65PC_P0	32	RX packet Length in 65-byte slot Packet Counter of Port 0
00004098	RL128PC_P0	32	RX packet Length in 128-byte slot Packet Counter of Port 0
0000409C	RL256PC_P0	32	RX packet Length in 256-byte slot Packet Counter of Port 0
000040A0	RL512PC_P0	32	RX packet Length in 512-byte slot Packet Counter of Port 0
000040A4	RL1024PC_P0	32	RX packet Length in 1024-byte slot Packet Counter of Port 0
000040A8	ROCL_P0	32	RX Octet Counter Low double word of Port 0
000040AC	ROCH_P0	32	Rx Octet Counter High double word of Port 0
000040B0	RDPC_CTRL_P0	32	RX CTRL Drop Packet Counter of Port 0
000040B4	RDPC_ING_P0	32	RX Ingress Drop Packet Counter of Port 0
000040B8	RDPC_ARL_P0	32	RX ARL Drop Packet Counter of Port 0
000040D0	TMIB_HF_STS_P0	32	TX Port MIB Counter Half Full Status of Port 0
000040D4	RMIB_HF_STS_P0	32	RX Port MIB Counter Half Full Status of Port 0
00004100	TDPC_P1	32	TX Drop Packet Counter of Port 1

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00004104	TCRC_P1	32	TX CRC Packet Counter of Port 1
00004108	TUPC_P1	32	TX Unicast Packet Counter of Port 1
0000410C	TMPC_P1	32	TX Multicast Packet Counter of Port 1
00004110	TBPC_P1	32	TX Broadcast Packet Counter of Port 1
00004114	TCEC_P1	32	TX Collision Event Counter of Port 1
00004118	TSCEC_P1	32	TX Single Collision Event Counter of Port 1
0000411C	TMCEC_P1	32	TX Multiple Collision Event Counter of Port 1
00004120	TDEC_P1	32	TX Deferred Event Counter of Port 1
00004124	TLCEC_P1	32	TX Late Collision Event Counter of Port 1
00004128	TXCEC_P1	32	TX excessive Collision Event Counter of Port 1
0000412C	TPPC_P1	32	TX Pause Packet Counter of Port 1
00004130	TL64PC_P1	32	TX packet Length in 64-byte slot Packet Counter of Port 1
00004134	TL65PC_P1	32	TX packet Length in 65-byte slot Packet Counter of Port 1
00004138	TL128PC_P1	32	TX packet Length in 128-byte slot Packet Counter of Port 1
0000413C	TL256PC_P1	32	TX packet Length in 256-byte slot Packet Counter of Port 1
00004140	TL512PC_P1	32	TX packet Length in 512-byte slot Packet Counter of Port 1
00004144	TL1024PC_P1	32	TX packet Length in 1024-byte slot Packet Counter of Port 1
00004148	TOCL_P1	32	TX Octet Counter Low double word of Port 1
0000414C	TOCH_P1	32	TX Octet Counter High double word of Port 1
00004160	RDPC_P1	32	RX Drop Packet Counter of Port 1
00004164	RFPC_P1	32	RX Filtering Packet Counter of Port 1
00004168	RUPC_P1	32	RX Unicast Packet Counter of Port 1
0000416C	RMPC_P1	32	RX Multicast Packet Counter of Port 1
00004170	RBPC_P1	32	RX Broadcast Packet Counter of Port 1
00004174	RAEPC_P1	32	RX Alignment Error Packet Counter of Port 1
00004178	RCEPC_P1	32	RX CRC(FCS) Error Packet Counter of Port 1
0000417C	RUSPC_P1	32	RX Undersize Packet Counter of Port 1
00004180	RFEPC_P1	32	RX Fragment Error Packet Counter of Port 1
00004184	ROSPC_P1	32	RX Oversize Packet Counter of Port 1
00004188	RJEPC_P1	32	RX Jabber Error Packet Counter of Port 1
0000418C	RPPC_P1	32	RX Pause Packet Counter of Port 1
00004190	RL64PC_P1	32	RX packet Length in 64-byte slot Packet Counter of Port 1
00004194	RL65PC_P1	32	RX packet Length in 65-byte slot Packet Counter of Port 1
00004198	RL128PC_P1	32	RX packet Length in 128-byte slot Packet Counter of Port 1
0000419C	RL256PC_P1	32	RX packet Length in 256-byte slot Packet Counter of Port 1
000041A0	RL512PC_P1	32	RX packet Length in 512-byte slot Packet Counter of Port 1
000041A4	RL1024PC_P1	32	RX packet Length in 1024-byte slot Packet Counter of Port 1
000041A8	ROCL_P1	32	RX Octet Counter Low double word of Port 1
000041AC	ROCH_P1	32	Rx Octet Counter High double word of Port 1
000041B0	RDPC_CTRL_P1	32	RX CTRL Drop Packet Counter of Port 1
000041B4	RDPC_ING_P1	32	RX Ingress Drop Packet Counter of Port 1
000041B8	RDPC_ARL_P1	32	RX ARL Drop Packet Counter of Port 1
000041D0	TMIB_HF_STS_P1	32	TX Port MIB Counter Half Full Status of Port 1
000041D4	RMIB_HF_STS_P1	32	RX Port MIB Counter Half Full Status of Port 1
00004200	TDPC_P2	32	TX Drop Packet Counter of Port 2
00004204	TCRC_P2	32	TX CRC Packet Counter of Port 2
00004208	TUPC_P2	32	TX Unicast Packet Counter of Port 2

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0000420C	TMPC_P2	32	TX Multicast Packet Counter of Port 2
00004210	TBPC_P2	32	TX Broadcast Packet Counter of Port 2
00004214	TCEC_P2	32	TX Collision Event Counter of Port 2
00004218	TSCEC_P2	32	TX Single Collision Event Counter of Port 2
0000421C	TMCEC_P2	32	TX Multiple Collision Event Counter of Port 2
00004220	TDEC_P2	32	TX Deferred Event Counter of Port 2
00004224	TLCEC_P2	32	TX Late Collision Event Counter of Port 2
00004228	TXCEC_P2	32	TX excessive Collision Event Counter of Port 2
0000422C	TPPC_P2	32	TX Pause Packet Counter of Port 2
00004230	TL64PC_P2	32	TX packet Length in 64-byte slot Packet Counter of Port 2
00004234	TL65PC_P2	32	TX packet Length in 65-byte slot Packet Counter of Port 2
00004238	TL128PC_P2	32	TX packet Length in 128-byte slot Packet Counter of Port 2
0000423C	TL256PC_P2	32	TX packet Length in 256-byte slot Packet Counter of Port 2
00004240	TL512PC_P2	32	TX packet Length in 512-byte slot Packet Counter of Port 2
00004244	TL1024PC_P2	32	TX packet Length in 1024-byte slot Packet Counter of Port 2
00004248	TOCL_P2	32	TX Octet Counter Low double word of Port 2
0000424C	TOCH_P2	32	TX Octet Counter High double word of Port 2
00004260	RDPC_P2	32	RX Drop Packet Counter of Port 2
00004264	RFPC_P2	32	RX Filtering Packet Counter of Port 2
00004268	RUPC_P2	32	RX Unicast Packet Counter of Port 2
0000426C	RMPC_P2	32	RX Multicast Packet Counter of Port 2
00004270	RBPC_P2	32	RX Broadcast Packet Counter of Port 2
00004274	RAEPC_P2	32	RX Alignment Error Packet Counter of Port 2
00004278	RCEPC_P2	32	RX CRC(FCS) Error Packet Counter of Port 2
0000427C	RUSPC_P2	32	RX Undersize Packet Counter of Port 2
00004280	RFEPC_P2	32	RX Fragment Error Packet Counter of Port 2
00004284	ROSPC_P2	32	RX Oversize Packet Counter of Port 2
00004288	RJEPC_P2	32	RX Jabber Error Packet Counter of Port 2
0000428C	RPPC_P2	32	RX Pause Packet Counter of Port 2
00004290	RL64PC_P2	32	RX packet Length in 64-byte slot Packet Counter of Port 2
00004294	RL65PC_P2	32	RX packet Length in 65-byte slot Packet Counter of Port 2
00004298	RL128PC_P2	32	RX packet Length in 128-byte slot Packet Counter of Port 2
0000429C	RL256PC_P2	32	RX packet Length in 256-byte slot Packet Counter of Port 2
000042A0	RL512PC_P2	32	RX packet Length in 512-byte slot Packet Counter of Port 2
000042A4	RL1024PC_P2	32	RX packet Length in 1024-byte slot Packet Counter of Port 2
000042A8	ROCL_P2	32	RX Octet Counter Low double word of Port 2
000042AC	ROCH_P2	32	Rx Octet Counter High double word of Port 2
000042B0	RDPC_CTRL_P2	32	RX CTRL Drop Packet Counter of Port 2
000042B4	RDPC_ING_P2	32	RX Ingress Drop Packet Counter of Port 2
000042B8	RDPC_ARL_P2	32	RX ARL Drop Packet Counter of Port 2
000042D0	TMIB_HF_STS_P2	32	TX Port MIB Counter Half Full Status of Port 2
000042D4	RMIB_HF_STS_P2	32	RX Port MIB Counter Half Full Status of Port 2
00004300	TDPC_P3	32	TX Drop Packet Counter of Port 3
00004304	TCRC_P3	32	TX CRC Packet Counter of Port 3
00004308	TUPC_P3	32	TX Unicast Packet Counter of Port 3
0000430C	TMPC_P3	32	TX Multicast Packet Counter of Port 3
00004310	TBPC_P3	32	TX Broadcast Packet Counter of Port 3

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00004314	TCEC_P3	32	TX Collision Event Counter of Port 3
00004318	TSCEC_P3	32	TX Single Collision Event Counter of Port 3
0000431C	TMCEC_P3	32	TX Multiple Collision Event Counter of Port 3
00004320	TDEC_P3	32	TX Deferred Event Counter of Port 3
00004324	TLCEC_P3	32	TX Late Collision Event Counter of Port 3
00004328	TXCEC_P3	32	TX excessive Collision Event Counter of Port 3
0000432C	TPPC_P3	32	TX Pause Packet Counter of Port 3
00004330	TL64PC_P3	32	TX packet Length in 64-byte slot Packet Counter of Port 3
00004334	TL65PC_P3	32	TX packet Length in 65-byte slot Packet Counter of Port 3
00004338	TL128PC_P3	32	TX packet Length in 128-byte slot Packet Counter of Port 3
0000433C	TL256PC_P3	32	TX packet Length in 256-byte slot Packet Counter of Port 3
00004340	TL512PC_P3	32	TX packet Length in 512-byte slot Packet Counter of Port 3
00004344	TL1024PC_P3	32	TX packet Length in 1024-byte slot Packet Counter of Port 3
00004348	TOCL_P3	32	TX Octet Counter Low double word of Port 3
0000434C	TOCH_P3	32	TX Octet Counter High double word of Port 3
00004360	RDPC_P3	32	RX Drop Packet Counter of Port 3
00004364	RFPC_P3	32	RX Filtering Packet Counter of Port 3
00004368	RUPC_P3	32	RX Unicast Packet Counter of Port 3
0000436C	RMPC_P3	32	RX Multicast Packet Counter of Port 3
00004370	RBPC_P3	32	RX Broadcast Packet Counter of Port 3
00004374	RAEPC_P3	32	RX Alignment Error Packet Counter of Port 3
00004378	RCEPC_P3	32	RX CRC(FCS) Error Packet Counter of Port 3
0000437C	RUSPC_P3	32	RX Undersize Packet Counter of Port 3
00004380	RFEPC_P3	32	RX Fragment Error Packet Counter of Port 3
00004384	ROSPC_P3	32	RX Oversize Packet Counter of Port 3
00004388	RJEPC_P3	32	RX Jabber Error Packet Counter of Port 3
0000438C	RPPC_P3	32	RX Pause Packet Counter of Port 3
00004390	RL64PC_P3	32	RX packet Length in 64-byte slot Packet Counter of Port 3
00004394	RL65PC_P3	32	RX packet Length in 65-byte slot Packet Counter of Port 3
00004398	RL128PC_P3	32	RX packet Length in 128-byte slot Packet Counter of Port 3
0000439C	RL256PC_P3	32	RX packet Length in 256-byte slot Packet Counter of Port 3
000043A0	RL512PC_P3	32	RX packet Length in 512-byte slot Packet Counter of Port 3
000043A4	RL1024PC_P3	32	RX packet Length in 1024-byte slot Packet Counter of Port 3
000043A8	ROCL_P3	32	RX Octet Counter Low double word of Port 3
000043AC	ROCH_P3	32	Rx Octet Counter High double word of Port 3
000043B0	RDPC_CTRL_P3	32	RX CTRL Drop Packet Counter of Port 3
000043B4	RDPC_ING_P3	32	RX Ingress Drop Packet Counter of Port 3
000043B8	RDPC_ARL_P3	32	RX ARL Drop Packet Counter of Port 3
000043D0	TMIB_HF_STS_P3	32	TX Port MIB Counter Half Full Status of Port 3
000043D4	RMIB_HF_STS_P3	32	RX Port MIB Counter Half Full Status of Port 3
00004400	TDPC_P4	32	TX Drop Packet Counter of Port 4
00004404	TCRC_P4	32	TX CRC Packet Counter of Port 4
00004408	TUPC_P4	32	TX Unicast Packet Counter of Port 4
0000440C	TMPC_P4	32	TX Multicast Packet Counter of Port 4
00004410	TBPC_P4	32	TX Broadcast Packet Counter of Port 4
00004414	TCEC_P4	32	TX Collision Event Counter of Port 4
00004418	TSCEC_P4	32	TX Single Collision Event Counter of Port 4

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0000441C	TMCEC_P4	32	TX Multiple Collision Event Counter of Port 4
00004420	TDEC_P4	32	TX Deferred Event Counter of Port 4
00004424	TLCEC_P4	32	TX Late Collision Event Counter of Port 4
00004428	TXCEC_P4	32	TX excessive Collision Event Counter of Port 4
0000442C	TPPC_P4	32	TX Pause Packet Counter of Port 4
00004430	TL64PC_P4	32	TX packet Length in 64-byte slot Packet Counter of Port 4
00004434	TL65PC_P4	32	TX packet Length in 65-byte slot Packet Counter of Port 4
00004438	TL128PC_P4	32	TX packet Length in 128-byte slot Packet Counter of Port 4
0000443C	TL256PC_P4	32	TX packet Length in 256-byte slot Packet Counter of Port 4
00004440	TL512PC_P4	32	TX packet Length in 512-byte slot Packet Counter of Port 4
00004444	TL1024PC_P4	32	TX packet Length in 1024-byte slot Packet Counter of Port 4
00004448	TOCL_P4	32	TX Octet Counter Low double word of Port 4
0000444C	TOCH_P4	32	TX Octet Counter High double word of Port 4
00004460	RDPC_P4	32	RX Drop Packet Counter of Port 4
00004464	RFPC_P4	32	RX Filtering Packet Counter of Port 4
00004468	RUPC_P4	32	RX Unicast Packet Counter of Port 4
0000446C	RMPC_P4	32	RX Multicast Packet Counter of Port 4
00004470	RBPC_P4	32	RX Broadcast Packet Counter of Port 4
00004474	RAEPC_P4	32	RX Alignment Error Packet Counter of Port 4
00004478	RCEPC_P4	32	RX CRC(FCS) Error Packet Counter of Port 4
0000447C	RUSPC_P4	32	RX Undersize Packet Counter of Port 4
00004480	RFEPC_P4	32	RX Fragment Error Packet Counter of Port 4
00004484	ROSPC_P4	32	RX Oversize Packet Counter of Port 4
00004488	RJEPC_P4	32	RX Jabber Error Packet Counter of Port 4
0000448C	RPPC_P4	32	RX Pause Packet Counter of Port 4
00004490	RL64PC_P4	32	RX packet Length in 64-byte slot Packet Counter of Port 4
00004494	RL65PC_P4	32	RX packet Length in 65-byte slot Packet Counter of Port 4
00004498	RL128PC_P4	32	RX packet Length in 128-byte slot Packet Counter of Port 4
0000449C	RL256PC_P4	32	RX packet Length in 256-byte slot Packet Counter of Port 4
000044A0	RL512PC_P4	32	RX packet Length in 512-byte slot Packet Counter of Port 4
000044A4	RL1024PC_P4	32	RX packet Length in 1024-byte slot Packet Counter of Port 4
000044A8	ROCL_P4	32	RX Octet Counter Low double word of Port 4
000044AC	ROCH_P4	32	Rx Octet Counter High double word of Port 4
000044B0	RDPC_CTRL_P4	32	RX CTRL Drop Packet Counter of Port 4
000044B4	RDPC_ING_P4	32	RX Ingress Drop Packet Counter of Port 4
000044B8	RDPC_ARL_P4	32	RX ARL Drop Packet Counter of Port 4
000044D0	TMIB_HF_STS_P4	32	TX Port MIB Counter Half Full Status of Port 4
000044D4	RMIB_HF_STS_P4	32	RX Port MIB Counter Half Full Status of Port 4
00004500	TDPC_P5	32	TX Drop Packet Counter of Port 5
00004504	TCRC_P5	32	TX CRC Packet Counter of Port 5
00004508	TUPC_P5	32	TX Unicast Packet Counter of Port 5
0000450C	TMPC_P5	32	TX Multicast Packet Counter of Port 5
00004510	TBPC_P5	32	TX Broadcast Packet Counter of Port 5
00004514	TCEC_P5	32	TX Collision Event Counter of Port 5
00004518	TSCEC_P5	32	TX Single Collision Event Counter of Port 5
0000451C	TMCEC_P5	32	TX Multiple Collision Event Counter of Port 5
00004520	TDEC_P5	32	TX Deferred Event Counter of Port 5

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00004524	TLCEC_P5	32	TX Late Collision Event Counter of Port 5
00004528	TXCEC_P5	32	TX excessive Collision Event Counter of Port 5
0000452C	TPPC_P5	32	TX Pause Packet Counter of Port 5
00004530	TL64PC_P5	32	TX packet Length in 64-byte slot Packet Counter of Port 5
00004534	TL65PC_P5	32	TX packet Length in 65-byte slot Packet Counter of Port 5
00004538	TL128PC_P5	32	TX packet Length in 128-byte slot Packet Counter of Port 5
0000453C	TL256PC_P5	32	TX packet Length in 256-byte slot Packet Counter of Port 5
00004540	TL512PC_P5	32	TX packet Length in 512-byte slot Packet Counter of Port 5
00004544	TL1024PC_P5	32	TX packet Length in 1024-byte slot Packet Counter of Port 5
00004548	TOCL_P5	32	TX Octet Counter Low double word of Port 5
0000454C	TOCH_P5	32	TX Octet Counter High double word of Port 5
00004560	RDPC_P5	32	RX Drop Packet Counter of Port 5
00004564	RFPC_P5	32	RX Filtering Packet Counter of Port 5
00004568	RUPC_P5	32	RX Unicast Packet Counter of Port 5
0000456C	RMPC_P5	32	RX Multicast Packet Counter of Port 5
00004570	RBPC_P5	32	RX Broadcast Packet Counter of Port 5
00004574	RAEPC_P5	32	RX Alignment Error Packet Counter of Port 5
00004578	RCEPC_P5	32	RX CRC(FCS) Error Packet Counter of Port 5
0000457C	RUSPC_P5	32	RX Undersize Packet Counter of Port 5
00004580	RFEPC_P5	32	RX Fragment Error Packet Counter of Port 5
00004584	ROSPC_P5	32	RX Oversize Packet Counter of Port 5
00004588	RJEPC_P5	32	RX Jabber Error Packet Counter of Port 5
0000458C	RPPC_P5	32	RX Pause Packet Counter of Port 5
00004590	RL64PC_P5	32	RX packet Length in 64-byte slot Packet Counter of Port 5
00004594	RL65PC_P5	32	RX packet Length in 65-byte slot Packet Counter of Port 5
00004598	RL128PC_P5	32	RX packet Length in 128-byte slot Packet Counter of Port 5
0000459C	RL256PC_P5	32	RX packet Length in 256-byte slot Packet Counter of Port 5
000045A0	RL512PC_P5	32	RX packet Length in 512-byte slot Packet Counter of Port 5
000045A4	RL1024PC_P5	32	RX packet Length in 1024-byte slot Packet Counter of Port 5
000045A8	ROCL_P5	32	RX Octet Counter Low double word of Port 5
000045AC	ROCH_P5	32	Rx Octet Counter High double word of Port 5
000045B0	RDPC_CTRL_P5	32	RX CTRL Drop Packet Counter of Port 5
000045B4	RDPC_ING_P5	32	RX Ingress Drop Packet Counter of Port 5
000045B8	RDPC_ARL_P5	32	RX ARL Drop Packet Counter of Port 5
000045D0	TMIB_HF_STS_P5	32	TX Port MIB Counter Half Full Status of Port 5
000045D4	RMIB_HF_STS_P5	32	RX Port MIB Counter Half Full Status of Port 5
00004600	TDPC_P6	32	TX Drop Packet Counter of Port 6
00004604	TCRC_P6	32	TX CRC Packet Counter of Port 6
00004608	TUPC_P6	32	TX Unicast Packet Counter of Port 6
0000460C	TMPC_P6	32	TX Multicast Packet Counter of Port 6
00004610	TBPC_P6	32	TX Broadcast Packet Counter of Port 6
00004614	TCEC_P6	32	TX Collision Event Counter of Port 6
00004618	TSCEC_P6	32	TX Single Collision Event Counter of Port 6
0000461C	TMCEC_P6	32	TX Multiple Collision Event Counter of Port 6
00004620	TDEC_P6	32	TX Deferred Event Counter of Port 6
00004624	TLCEC_P6	32	TX Late Collision Event Counter of Port 6
00004628	TXCEC_P6	32	TX excessive Collision Event Counter of Port 6

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0000462C	TPPC_P6	32	TX Pause Packet Counter of Port 6
00004630	TL64PC_P6	32	TX packet Length in 64-byte slot Packet Counter of Port 6
00004634	TL65PC_P6	32	TX packet Length in 65-byte slot Packet Counter of Port 6
00004638	TL128PC_P6	32	TX packet Length in 128-byte slot Packet Counter of Port 6
0000463C	TL256PC_P6	32	TX packet Length in 256-byte slot Packet Counter of Port 6
00004640	TL512PC_P6	32	TX packet Length in 512-byte slot Packet Counter of Port 6
00004644	TL1024PC_P6	32	TX packet Length in 1024-byte slot Packet Counter of Port 6
00004648	TOCL_P6	32	TX Octet Counter Low double word of Port 6
0000464C	TOCH_P6	32	TX Octet Counter High double word of Port 6
00004660	RDPC_P6	32	RX Drop Packet Counter of Port 6
00004664	RFPC_P6	32	RX Filtering Packet Counter of Port 6
00004668	RUPC_P6	32	RX Unicast Packet Counter of Port 6
0000466C	RMPC_P6	32	RX Multicast Packet Counter of Port 6
00004670	RBPC_P6	32	RX Broadcast Packet Counter of Port 6
00004674	RAEPC_P6	32	RX Alignment Error Packet Counter of Port 6
00004678	RCEPC_P6	32	RX CRC(FCS) Error Packet Counter of Port 6
0000467C	RUSPC_P6	32	RX Undersize Packet Counter of Port 6
00004680	RFEPC_P6	32	RX Fragment Error Packet Counter of Port 6
00004684	ROSPC_P6	32	RX Oversize Packet Counter of Port 6
00004688	RJEPC_P6	32	RX Jabber Error Packet Counter of Port 6
0000468C	RPPC_P6	32	RX Pause Packet Counter of Port 6
00004690	RL64PC_P6	32	RX packet Length in 64-byte slot Packet Counter of Port 6
00004694	RL65PC_P6	32	RX packet Length in 65-byte slot Packet Counter of Port 6
00004698	RL128PC_P6	32	RX packet Length in 128-byte slot Packet Counter of Port 6
0000469C	RL256PC_P6	32	RX packet Length in 256-byte slot Packet Counter of Port 6
000046A0	RL512PC_P6	32	RX packet Length in 512-byte slot Packet Counter of Port 6
000046A4	RL1024PC_P6	32	RX packet Length in 1024-byte slot Packet Counter of Port 6
000046A8	ROCL_P6	32	RX Octet Counter Low double word of Port 6
000046AC	ROCH_P6	32	Rx Octet Counter High double word of Port 6
000046B0	RDPC_CTRL_P6	32	RX CTRL Drop Packet Counter of Port 6
000046B4	RDPC_ING_P6	32	RX Ingress Drop Packet Counter of Port 6
000046B8	RDPC_ARL_P6	32	RX ARL Drop Packet Counter of Port 6
000046D0	TMIB_HF_STS_P6	32	TX Port MIB Counter Half Full Status of Port 6
000046D4	RMIB_HF_STS_P6	32	RX Port MIB Counter Half Full Status of Port 6
00004F00	AE0CNT	32	ACL Event 0 Counter
00004F04	AE1CNT	32	ACL Event 1 Counter
00004F08	AE2CNT	32	ACL Event 2 Counter
00004F0C	AE3CNT	32	ACL Event 3 Counter
00004F10	AE4CNT	32	ACL Event 4 Counter
00004F14	AE5CNT	32	ACL Event 5 Counter
00004F18	AE6CNT	32	ACL Event 6 Counter
00004F1C	AE7CNT	32	ACL Event 7 Counter
00004FE0	MIBCCR	32	MIB Counter Control
00004FE4	AECCR	32	ARL Event Counter Control
00004FE8	AEMIB_HF_STS	32	ARL Event MIB Counter Half Full Status
00004FF0	MIBHF_INT_EN	32	Port/ARL MIB Counter Half Full Interrupt Enable
00004FF4	MIBHF_INT_STS	32	Port/ARL MIB Counter Half Full Interrupt Status

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00007000	SYS_CTRL	32	System Control
00007004	PM_CTRL	32	Power Management Control
00007008	SYS_INT_EN	32	System Interrupt Enable
0000700C	SYS_INT_STS	32	System Interrupt Status
00007018	PHY_POLL	32	PHY Polling and SMI Master Control Register
0000701C	PHY_IAC	32	PHY Indirect Access Control
00007020	PSR_P3_P0	32	PHY Status Register for Port 3 ~ Port 0
00007024	PSR_P6_P4	32	PHY Status Register for Port 6 ~ Port 4
00007028	PAUSE_CAP_P6_P0	32	MAC Pause TX/RX Capability Register for Port 6 ~ Port 0
00007034	DBG_SIG	32	Debug Signals
00007038	DBGSEL0	32	Debug Signals Selection Group
00007120	EEPR_IND	32	EEPROM INDIRECT ACCESS CONTROL REGISTER
00007124	EEPR_STS	32	EEPROM STATUS REGISTER
00007200	TICKER_CR	32	TICKER CONFIGURATION REGISTER
00007204	DELSEL_CTRL	32	DELSEL OF SRAM CONFIGURATION REGISTER
00007800	HWTRAP	32	Hardware Trap Status Register
00007804	MHWTRAP	32	Modified Hardware Trap Status Register
00007808	TOP_SIG_CTRL_CR	32	TOP Signals Control Register
00007810	IO_DRV_CR	32	IO Driving Strength Control Register
00007814	P5_TX_IO_DUTY_CR	32	P5 TX IO Duty Cycle Control Register
00007818	P5_RX_IO_DUTY_CR	32	P5 RX IO Duty Cycle Control Register
00007820	IOTEST_Output_0	32	IOTEST Output Control Register 1
00007824	IOTEST_Output_1	32	IOTEST Output Control Register 2
00007828	IOTEST_Intput_0	32	IOTEST Input Record Register 1
0000782C	IOTEST_Intput_1	32	IOTEST Input Record Register 2
00007830	P6ECR	32	P6 Extend Control Register
00007A00	TRGMII_RCK_CTRL	32	TRGMII RXC CONTROL REGISTER
00007A04	TRGMII_RCK_RTT	32	TRGMII RXC ODT REGISTER
00007A10	TRGMII_RD0	32	TRGMII RD0 CONTROL REGISTER
00007A14	TRGMII_RD0_RTT	32	TRGMII RD0 RTT REGISTER
00007A18	TRGMII_RD1	32	TRGMII RD1 CONTROL REGISTER
00007A1C	TRGMII_RD1_RTT	32	TRGMII RD1 RTT REGISTER
00007A20	TRGMII_RD2	32	TRGMII RD2 CONTROL REGISTER
00007A24	TRGMII_RD2_RTT	32	TRGMII RD2 RTT REGISTER
00007A28	TRGMII_RD3	32	TRGMII RD3 CONTROL REGISTER
00007A2C	TRGMII_RD3_RTT	32	TRGMII RD3 RTT REGISTER
00007A30	TRGMII_RXCTL	32	TRGMII RXCTL CONTROL REGISTER
00007A34	TRGMII_RXCTL_RTT	32	TRGMII RXCTL RTT REGISTER
00007A40	TRGMII_TXCTRL	32	TRGMII TX CONTROL REGISTER
00007A50	TRGMII_TD0_CTRL	32	TRGMII TD0 CTRL REGISTER
00007A54	TRGMII_TD0_ODT	32	TRGMII TD0 ODT REGISTER
00007A58	TRGMII_TD1_CTRL	32	TRGMII TD1 CTRL REGISTER
00007A5C	TRGMII_TD1_ODT	32	TRGMII TD1 ODT REGISTER
00007A60	TRGMII_TD2_CTRL	32	TRGMII TD2 CTRL REGISTER
00007A64	TRGMII_TD2_ODT	32	TRGMII TD2 ODT REGISTER
00007A68	TRGMII_TD3_CTRL	32	TRGMII TD3 CTRL REGISTER
00007A6C	TRGMII_TD3_ODT	32	TRGMII TD3 ODT REGISTER

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00007A70	TRGMII_TXCTL_CTRL	32	TRGMII TXCTL CTRL REGISTER
00007A74	TRGMII_TXCTL_ODT	32	TRGMII TXCTL ODT REGISTER
00007A78	TRGMII_TCK_CTRL	32	TRGMII TCK CTRL REGISTER
00007A7C	TRGMII_TCK_ODT	32	TRGMII TCK ODT REGISTER
00007B00	P5RGMIIRXCR	32	P5 RGMII Wrapper RX Clock Control Register
00007B04	P5RGMIITXCR	32	P5 RGMII Wrapper TX Clock Control Register
00007B08	P5RGMIICKCR	32	P5 RGMII Wrapper Clock Enable Control Register
00007D00	LED_EN	32	LED I/O function enable
00007D04	LED_IO_MODE	32	LED I/O Mode
00007D08	LED_HW_MODE	32	LED Hardware Mode
00007D0C	LED_SRC	32	LED Source Selection
00007E00	GLB_PRB_CR	32	Global Probing Control Register
00007E04	GLB_PRB_SR	32	Global Probing Status Register
00007E10	TOP_PRB_CR	32	TOP Probing Control Register
00007E14	TOP_PRB_SR	32	TOP Probing Status Register
00007E20	TRGMII_PRB_CR	32	TRGMII Probing Control Register
00007E24	TRGMII_PRB_SR	32	TRGMII Probing Status Register
00007E30	RGMII_PRB_CR	32	RGMII Probing Control Register
00007E34	RGMII_PRB_SR	32	RGMII Probing Status Register
00007FFC	CREV	32	Chip Revision

00000000 MISC0 MISC 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[31:16]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[15:0]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	REV0	Reserved

00000004 MISC1 MISC 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[31:16]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[15:0]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	REV0	Reserved

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00000008 AISR ACL Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_ISR[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACL_ISR[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ACL_ISR	**ACL Interrupt Status for entry 0~31** (Refer to ACL Rule Control Table)

0000000C AGC ARL Global Control 00071819

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MLDv2_int_en	REV0												ACL_INT	VLAN_INT	ADDR_INT
Type	RW	DC												RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATE_COMP	COMP_BNUM							LOCAL_EN	ARL_PADDING	ACL_MULTI	L2LEN_CHK	CTRL_DROP	VLAN4CPU	ARL_PRI	ALR_RST_N
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1

Bit(s)	Name	Description
31	MLDv2_int_en	**MLDv2 interrupt enable** 0: Disable 1: Enable
30:19	REV0	**Reserved**
18	ACL_INT	**Access Control List (ACL) Table Initialization Done** 0: ACL Table is busy. 1: ACL Table is cleared.
17	VLAN_INT	**VLAN Table Initialization Done** 0: VLAN Table is busy. 1: VLAN Table is cleaned.
16	ADDR_INT	**ADDR Table Initialization Done** 0: ADDR Table is busy. 1: ADDR Table is cleaned.
15	RATE_COMP	**Rate Limit Compensation** Add or subtract the specific byte number while calculating the packet length. 0: Add 1: Minus
14:8	COMP_BNUM	**Compensation Byte Number** The added/subtracted byte number for the rate limit or the meter table
7	LOCAL_EN	**Local Port Forwarding Enable** 0: Drop frames at the local port. 1: Allow frame forwarding to the local port.
6	ARL_PADDING	**ARL Data Padding** Set ARL to add byte padding up to 46 bytes when the length of the data field of the

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		incoming frame is less than 46 bytes. 0: Disable (default) 1: Enable
5	ACL_MULTI	**Enable Multiple ACL Hit** 0: Only the first hit ACL entry 1: Allow multiple ACL hit entries on Rate, Interrupt, and MIB.
4	L2LEN_CHK	**Layer 2 Frame Length Check** Enable a length check on length-encapsulated frame. Drop length error frames when the value of the ELEN field of this frame is bigger than the length of the data field. 0: Disable 1: Enable
3	CTRL_DROP	**MAC Control Frame Drop** Drop MAC control frames with ETYPE=0x8808. 0: Disable (default) 1: Enable
2	VLAN4CPU	**TO_CPU VLAN Member** Set the TO_CPU frame to check VLAN members. 0: Ignore VLAN members. 1: Check VLAN members.
1	ARL_PRI	**ARL Resolution Priority** 0: P0 is the lowest priority. 1: P0 is the highest priority.
0	ALR_RST_N	**ARL Enable (Soft Reset)** 0: Reset the ARL engine. 1: Enable ARL engine.

00000010 MFC MAC Forward Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BC_FFP								UNM_FFP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNU_FFP								CPU_EN	CPU_PORT			MIRROR_EN	MIRROR_PORT		
Type	RW								RW	RW			RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BC_FFP	**Broadcast Frame Flooding Ports** If MAC receives broadcast frames, this field indicates the flooding ports. [NOTE] 1. The flooding port excludes the received port on the switch. 2. Frame dropped though BC_FFP=6'b0
23:16	UNM_FFP	**Unknown Multicast Frame Flooding Ports** If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports. [NOTE] 1. The flooding port will exclude the received port by HW. 2. Frame dropped though UNM_FFP=6'b0.
15:8	UNU_FFP	**Unknown Unicast Frame Flooding Ports** If MAC receives the unicast or multicast frames which can not be found on the ARL. The field indicates the flooding port. [NOTE] 1. The flooding port will excludes the received port by HW 2. Frame dropped though UNM_FFP=6'b0
7	CPU_EN	**CPU Port Enable** Enable the CPU port specified in CPU_PORT.

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		0: No CPU port exists. 1: Enable
6:4	CPU_PORT	**CPU Port Number** Set the CPU port number. 3'h0: Port 0 ... 3'h7: Port 7
3	MIRROR_EN	**Mirror Port Enable** Enable the mirror port specified in MIRROR_PORT. 0: No mirror available 1: Enable mirror
2:0	MIRROR_PORT	**Mirror Port Number** Set the mirror port number. 3'h0: Port 0 ... 3'h7: Port 7

00000014 VTC VLAN TAG Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0														MC_ARL_LKYV	UC_ARL_LKYV
Type	DC														RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1								GUEST_MEM							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:18	REV0	**Reserved**
17	MC_ARL_LKYV	**Multicast Frame ARL Leaky VLAN Enable** 1: Use LEAKY_EN in ARL to control the multicast frames. 0: Use PVC.MC_LKYV_EN in Port Control register to control the multicast frames
16	UC_ARL_LKYV	**Unicast Frame ARL Leaky VLAN Enable** 1: Use LEAKY_EN in ARL to control the unicast frames 0: Use PVC.UC_LKYV_EN in Port Control register to control the unicast frames
15:8	REV1	**Reserved**
7:0	GUEST_MEM	**Guest VLAN Member** The assigned VLAN member for the frames which cannot pass 802.1x authentication

00000018 ISC IGMP Snooping Control 7F027D7F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRN_RP								REV0			DWN_GRADE_EN	MLD_RP_EN	IGMP_RP_EN	ROBUST_VAR	
Type	RO								DC			RW	RW	RW	RW	
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QRY_INTL								DEF_RP							
Type	RW								RW							
Reset	0	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1

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Bit(s)	Name	Description
31:24	LRN_RP	**Learned Router Ports** Show the router ports for IGMP/MDL messages including the default and learned ports.
23:21	REV0	**Reserved**
20	DWN_GRADE_EN	**IGMP v2 to v1 Auto-Downgrade Enable** Enable an automatic downgrade from IGMPv2 to v1 due to a IGMPv1 report message. 0: Disable 1: Enable
19	MLD_RP_EN	**MLD Router Port Learning Enable** Enable automatic router port learning automatically based on MLD queries. 0: Disable 1: Enable
18	IGMP_RP_EN	**IGMP Router Port Learning** Enable automatic router port learning based on IGMP queries. 0: Disable 1: Enable
17:16	ROBUST_VAR	**Robustness Variable** Define the maximum allowable number of IGMP Query messages that may be lost consecutively. 0: Reserved 1: One time 2: Two times (default) 3: Three times
15:8	QRY_INTL	**Query Interval** Together with the Robustness Variable, the Query Interval sets the age-out time for router ports automatically learned from IGMP Query frames. Age-out time = (QRY_INTL * ROBUST_VAR) (unit: sec)
7:0	DEF_RP	**Default Router Port** Set the default router port which will not be aged out when IGMP/MLD router port learning is enabled.

0000001C IMC IGMP/MLD Message Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MDL_RPT_MIR	MLD_RPT_FW			MLD_MANG_FR	MLD_PAE_FR	MLD_BPDU_FR	MLD_EG_TAG			MLD_LKY_VLAN	MLD_PRI_HIGH	MLD_QUE_MIR	MLD_QUE_FW		
Type	RW	RW			RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGMP_RPT_MIR	IGMP_RPT_FW			IGMP_MANG_FR	IGMP_PAE_FR	IGMP_BPDU_FR	IGMP_EG_TAG			IGMP_LKY_VLAN	IGMP_PRI_HIGH	IGMP_QUE_MIR	IGMP_QUE_FW		
Type	RW	RW			RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	MDL_RPT_MIR	**MLD Report/Done Message to Mirror Port** 0: Disable 1: Frame copied to Mirror port
30:28	MLD_RPT_FW	**MLD Report/Done Message TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped

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27	MLD_MANG_FR	**MLD Message as Management Frame** 0: Disable 1: Regarded as management frame
26	MLD_PAE_FR	**MLD Message as PAE Frame** 0: Disable 1: Regarded as PAE frame
25	MLD_BPDU_FR	**MLD Message as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	MLD_EG_TAG	**MLD Message Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	MLD_LKY_VLAN	**MLD Leaky VLAN Enable** 0: Disable 1: Enable
20	MLD_PRI_HIGH	**MLD Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	MLD_QUE_MIR	**MLD Query Message to Mirror Port** 0: Disable 1: Frame copied to Mirror port
18:16	MLD_QUE_FW	**MLD Query Message TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15	IGMP_RPT_MIR	**IGMP Report/Done Message to Mirror Port** 0: Disable 1: Frame copied to Mirror port
14:12	IGMP_RPT_FW	**IGMP Report/Done Message TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped
11	IGMP_MANG_FR	**IGMP Message as Management Frame** 0: Disable 1: Regarded as management frame
10	IGMP_PAE_FR	**IGMP Message as PAE Frame** 0: Disable 1: Regarded as PAE frame
9	IGMP_BPDU_FR	**IGMP Message as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	IGMP_EG_TAG	**IGMP Message Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	IGMP_LKY_VLAN	**IGMP Leaky VLAN Enable**

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		0: Disable 1: Enable
4	IGMP_PRI_HIGH	**IGMP Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	IGMP_QUE_MIR	**IGMP Query Message to Mirror Port** 0: Disable 1: Frame copied to Mirror port
2:0	IGMP_QUE_FW	**IGMP Query Message TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000020 APC ARP and PPPoE Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				PPP_MANG_FR	PPP_PAE_FR	PPP_BPDU_FR	PPP_EG_TAG			PPP_LKY_VLAN	PPP_PRI_HIGH	PPP_MIR	PPP_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				ARP_MANG_FR	ARP_PAE_FR	ARP_BPDU_FR	ARP_EG_TAG			ARP_LKY_VLAN	ARP_PRI_HIGH	ARP_MIR	ARP_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	**Reserved**
27	PPP_MANG_FR	**PPPoE Discovery as Management Frame** 0: Disable 1: Regarded as management frame
26	PPP_PAE_FR	**PPPoE Discovery as PAE Frame** 0: Disable 1: Regarded as PAE frame
25	PPP_BPDU_FR	**PPPoE Discovery as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	PPP_EG_TAG	**PPPoE Discovery Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	PPP_LKY_VLAN	**PPPoE Discovery Leaky VLAN Enable** 0: Disable 1: Enable
20	PPP_PRI_HIGH	**PPPoE Discovery Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	PPP_MIR	**PPPoE Discovery to Mirror Port** 0: Disable

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		1: Frame copied to Mirror port
18:16	PPP_PORT_FW	**PPPoE Discovery TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	**Reserved**
11	ARP_MANG_FR	**ARP/RARP Discovery as Management Frame** 0: Disable 1: Regarded as management frame
10	ARP_PAE_FR	**ARP/RARP Discovery as PAE Frame** 0: Disable 1: Regarded as PAE frame
9	ARP_BPDU_FR	**ARP/RARP Discovery as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	ARP_EG_TAG	**ARP/RARP Discovery Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	ARP_LKY_VLAN	**ARP/RARP Discovery Leaky VLAN Enable** 0: Disable 1: Enable
4	ARP_PRI_HIGH	**ARP/RARP Discovery Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	ARP_MIR	**ARP/RARP Discovery to Mirror Port** 0: Disable 1: Frame copied to Mirror port
2:0	ARP_PORT_FW	**ARP/RARP Discovery TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000024 BPC BPDU and PAE Control 0C100A10

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				PAE_MANG_FR	PAE_PAE_FR	PAE_BPDU_FR	PAE_EG_TAG			PAE_LKY_VLAN	PAE_PRI_HIGH	PAE_MIR	PAE_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				BPDU_MANG_FR	BPDU_PAE_FR	BPDU_BPDU_FR	BPDU_EG_TAG			BPDU_LKY_VLAN	BPDU_PRI_HIGH	BPDU_MIR	BPDU_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description

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31:28	REV0	**Reserved**
27	PAE_MANG_FR	**PAE as Management Frame** 0: Disable 1: Regarded as management frame
26	PAE_PAE_FR	**PAE as PAE Frame** 0: Disable 1: Regarded as PAE frame
25	PAE_BPDU_FR	**PAE as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	PAE_EG_TAG	**PAE Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	PAE_LKY_VLAN	**PAE Leaky VLAN Enable** 0: Disable 1: Enable
20	PAE_PRI_HIGH	**PAE Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	PAE_MIR	**PAE to Mirror Port** 0: Disable 1: Frame copied to Mirror port
18:16	PAE_PORT_FW	**PAE TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	**Reserved**
11	BPDU_MANG_FR	**BPDU as Management Frame** 0: Disable 1: Regarded as management frame
10	BPDU_PAE_FR	**BPDU as PAE Frame** 0: Disable 1: Regarded as PAE frame
9	BPDU_BPDU_FR	**BPDU as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	BPDU_EG_TAG	**BPDU Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	BPDU_LKY_VLAN	**BPDU Leaky VLAN Enable** 0: Disable 1: Enable
4	BPDU_PRI_HIGH	**BPDU Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	BPDU_MIR	**BPDU to Mirror Port** 0: Disable

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		1: Frame copied to Mirror port
2:0	BPDU_PORT_FW	**BPDU TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000028 RGAC1 REV_01 and REV_02 Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				R02_MANG_FR	R02_PAE_FR	R02_BPDU_FR	R02_EG_TAG			R02_LKY_VLAN	R02_PRI_HIGH	R02_MIR	R02_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R01_MANG_FR	R01_PAE_FR	R01_BPDU_FR	R01_EG_TAG			R01_LKY_VLAN	R01_PRI_HIGH	R01_MIR	R01_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	**Reserved**
27	R02_MANG_FR	**REV_02 as Management Frame** 0: Disable 1: Regarded as management frame
26	R02_PAE_FR	**REV_02 as PAE Frame** 0: Disable 1: Regarded as PAE frame
25	R02_BPDU_FR	**REV_02 as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	R02_EG_TAG	**REV_02 Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	R02_LKY_VLAN	**REV_02 Leaky VLAN Enable** 0: Disable 1: Enable
20	R02_PRI_HIGH	**REV_02 Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	R02_MIR	**REV_02 to Mirror Port** 0: Disable 1: Frame copied to Mirror port
18:16	R02_PORT_FW	**REV_02 TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

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15:12	REV1	**Reserved**
11	R01_MANG_FR	**REV_01 as Management Frame** 0: Disable 1: Regarded as management frame
10	R01_PAE_FR	**REV_01 as PAE Frame** 0: Disable 1: Regarded as PAE frame
9	R01_BPDU_FR	**REV_01 as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R01_EG_TAG	**REV_01 Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R01_LKY_VLAN	**REV_01 Leaky VLAN Enable** 0: Disable 1: Enable
4	R01_PRI_HIGH	**REV_01 Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	R01_MIR	**REV_01 to Mirror Port** 0: Disable 1: Frame copied to Mirror port
2:0	R01_PORT_FW	**REV_01 TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

0000002C RGAC2 REV_03 and REV_0E Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				R0E_MANG_FR	R0E_PAE_FR	R0E_BPDU_FR	R0E_EG_TAG			R0E_LKY_VLAN	R0E_PRI_HIGH	R0E_MIR	R0E_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R03_MANG_FR	R03_PAE_FR	R03_BPDU_FR	R03_EG_TAG			R03_LKY_VLAN	R03_PRI_HIGH	R03_MIR	R03_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	**Reserved**
27	R0E_MANG_FR	**REV_0E as Management Frame** 0: Disable 1: Regarded as management frame
26	R0E_PAE_FR	**REV_0E as PAE Frame** 0: Disable 1: Regarded as PAE frame

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25	R0E_BPDU_FR	**REV_0E as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	R0E_EG_TAG	**REV_0E Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	R0E_LKY_VLAN	**REV_0E Leaky VLAN Enable** 0: Disable 1: Enable
20	R0E_PRI_HIGH	**REV_0E Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	R0E_MIR	**REV_0E to Mirror Port** 0: Disable 1: Frame copied to Mirror port
18:16	R0E_PORT_FW	**REV_0E TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	**Reserved**
11	R03_MANG_FR	**REV_03 as Management Frame** 0: Disable 1: Regarded as management frame
10	R03_PAE_FR	**REV_03 as PAE Frame** 0: Disable 1: Regarded as PAE frame
9	R03_BPDU_FR	**REV_03 as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R03_EG_TAG	**REV_03 Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R03_LKY_VLAN	**REV_03 Leaky VLAN Enable** 0: Disable 1: Enable
4	R03_PRI_HIGH	**REV_03 Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	R03_MIR	**REV_03 to Mirror Port** 0: Disable 1: Frame copied to Mirror port
2:0	R03_PORT_FW	**REV_03 TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

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00000030 RGAC3 REV_10 and REV_20 Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				R20_MANG_FR	R20_PAE_FR	R20_BPDU_FR	R20_EG_TAG			R20_LKY_VLAN	R20_PRI_HIGH	R20_MIR	R20_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R10_MANG_FR	R10_PAE_FR	R10_BPDU_FR	R10_EG_TAG			R10_LKY_VLAN	R10_PRI_HIGH	R10_MIR	R10_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	**Reserved**
27	R20_MANG_FR	**REV_20 as Management Frame** 0: Disable 1: Regarded as management frame
26	R20_PAE_FR	**REV_20 as PAE Frame** 0: Disable 1: Regarded as PAE frame
25	R20_BPDU_FR	**REV_20 as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	R20_EG_TAG	**REV_20 Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	R20_LKY_VLAN	**REV_20 Leaky VLAN Enable** 0: Disable 1: Enable
20	R20_PRI_HIGH	**REV_20 Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	R20_MIR	**REV_20 to Mirror Port** 0: Disable 1: Frame copied to Mirror port
18:16	R20_PORT_FW	**REV_20 TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	**Reserved**
11	R10_MANG_FR	**REV_10 as Management Frame** 0: Disable 1: Regarded as management frame
10	R10_PAE_FR	**REV_10 as PAE Frame** 0: Disable 1: Regarded as PAE frame

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9	R10_BPDU_FR	**REV_10 as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R10_EG_TAG	**REV_10 Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R10_LKY_VLAN	**REV_10 Leaky VLAN Enable** 0: Disable 1: Enable
4	R10_PRI_HIGH	**REV_10 Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	R10_MIR	**REV_10 to Mirror Port** 0: Disable 1: Frame copied to Mirror port
2:0	R10_PORT_FW	**REV_10 TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000034 RGAC4 REV_21 and REV_UN Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				RUN_MANG_FR	RUN_PAE_FR	RUN_BPDU_FR	RUN_EG_TAG			RUN_LKY_VLAN	RUN_PRI_HIGH	RUN_MIR	RUN_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R21_MANG_FR	R21_PAE_FR	R21_BPDU_FR	R21_EG_TAG			R21_LKY_VLAN	R21_PRI_HIGH	R21_MIR	R21_PORT_FW		
Type	DC				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	**Reserved**
27	RUN_MANG_FR	**REV_20 as Management Frame** 0: Disable 1: Regarded as management frame
26	RUN_PAE_FR	**REV_20 as PAE Frame** 0: Disable 1: Regarded as PAE frame
25	RUN_BPDU_FR	**REV_20 as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	RUN_EG_TAG	**REV_20 Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged

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		3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	RUN_LKY_VLAN	**REV_20 Leaky VLAN Enable** 0: Disable 1: Enable
20	RUN_PRI_HIGH	**REV_20 Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
19	RUN_MIR	**REV_20 to Mirror Port** 0: Disable 1: Frame copied to Mirror port
18:16	RUN_PORT_FW	**REV_20 TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	**Reserved**
11	R21_MANG_FR	**REV_UN as Management Frame** 0: Disable 1: Regarded as management frame
10	R21_PAE_FR	**REV_UN as PAE Frame** 0: Disable 1: Regarded as PAE frame
9	R21_BPDU_FR	**REV_UN as BPDU Frame** 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R21_EG_TAG	**REV_UN Egress VLAN Tag Attribution** 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R21_LKY_VLAN	**REV_UN Leaky VLAN Enable** 0: Disable 1: Enable
4	R21_PRI_HIGH	**REV_UN Force the Highest Priority** 0: System default 1: Assigned to the highest priority queue.
3	R21_MIR	**REV_UN to Mirror Port** 0: Disable 1: Frame copied to Mirror port
2:0	R21_PORT_FW	**REV_UN TO_CPU Forwarding** 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000038 **PMC** **Protocol Match Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TYPE3_EN	TYPE3_VLD	TYPE3_ENCAP				REV1		TYPE2_EN	TYPE2_VLD	TYPE2_ENCAP			

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Type	DC		RW	RW	RW				DC		RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2		TYPE1_EN	TYPE1_VLD	TYPE1_ENCAP				REV3							
Type	DC		RW	RW	RW				DC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29	TYPE3_EN	**TYPE 3 Match Enable**
28	TYPE3_VLD	**TYPE 3 Value Va**
27:24	TYPE3_ENCAP	**Encapsulated Frame Type Value**
23:22	REV1	**Reserved**
21	TYPE2_EN	**TYPE 2 Match Enable**
20	TYPE2_VLD	**TYPE 2 Value Va**
19:16	TYPE2_ENCAP	**Encapsulated Frame Type Value**
15:14	REV2	**Reserved**
13	TYPE1_EN	**TYPE 1 Match Enable**
12	TYPE1_VLD	**TYPE 1 Value Va** 0: TYPE 1 Value in register PBG.TYPE1 is "don't care", i.e. it has no effect. 1: TYPE 1 Value in register PBG.TYPE1 is valid.
11:8	TYPE1_ENCAP	**Encapsulated Frame Type Value** Bit0: Ethernet II Bit1: RFC_1042 Bit2: IPX Raw 802.3 Bit3: 802.2/802.3 Length Encapsulated
7:0	REV3	**Reserved**

0000003C PBG1 Protocol Based Group ID-1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TYPE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TYPE1	**TYPE 1 Value** Ethernet II: Matched with EtherType RFC_1042: Matched with SNAP Type IPX Raw 802.3: "Don't care" 802.2/802.3 Length Encapsulate: Matched with DSAP[15:8] and SSAP[7:0]
15:0	REV0	**Reserved**

00000040 PBG2 Protocol Based Group ID-2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TYPE3															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TYPE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TYPE3	**TYPE 3 Value**
15:0	TYPE2	**TYPE 2 Value**

00000044 UPW User Priority Weight 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0									ARL_UPW			REV1	PORT_UPW		
Type	DC									RW			DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	DC	RW			DC	RW			DC	RW			DC	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
31:23	REV0	**Reserved**
22:20	ARL_UPW	**ARL User Priority Weight (MAC/DIP Hit)**
19	REV1	**Reserved**
18:16	PORT_UPW	**Port-Based User Priority Weight Value** Weights range from 0x0 to 0x7.
15	REV2	**Reserved**
14:12	DSCP_UPW	**DSCP Priority Weight (IPv4)**
11	REV3	**Reserved**
10:8	TAG_UPW	**Priority Tag User Priority Weight**
7	REV4	**Reserved**
6:4	STAG_UPW	**Special Tag User Priority Weight**
3	REV5	**Reserved**
2:0	ACL_UPW	**ACL User Priority Weight (ACL Hit)**

00000048 PEM1 User Priority Egress Mapping I 08480240

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_1			QUE_CPU_1			QUE_LAN_1		DSCP_PRI_1					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_0			QUE_CPU_0			QUE_LAN_0		DSCP_PRI_0					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_1	**User Priority 1 Priority Tag Value**
26:24	QUE_CPU_1	**User Priority 1 CPU Queue Selectio**

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23:22	QUE_LAN_1	**User Priority 1 LAN Queue Selection**
21:16	DSCP_PRI_1	**User Priority 1 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_0	**User Priority 0 Priority Tag Value**
10:8	QUE_CPU_0	**User Priority 0 CPU Queue Selectio**
7:6	QUE_LAN_0	**User Priority 0 LAN Queue Selection**
5:0	DSCP_PRI_0	**User Priority 0 DSCP Value**

0000004C PEM2 User Priority Egress Mapping II 1B581110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_3			QUE_CPU_3			QUE_LAN_3		DSCP_PRI_3					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	1	1	0	1	1	0	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_2			QUE_CPU_2			QUE_LAN_2		DSCP_PRI_2					
Type	DC		RW			RW			RW		RW					
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_3	**User Priority 3 Priority Tag Value**
26:24	QUE_CPU_3	**User Priority 3 CPU Queue Selectio**
23:22	QUE_LAN_3	**User Priority 3 LAN Queue Selection**
21:16	DSCP_PRI_3	**User Priority 3 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_2	**User Priority 2 Priority Tag Value**
10:8	QUE_CPU_2	**User Priority 2 CPU Queue Selectio**
7:6	QUE_LAN_2	**User Priority 2 LAN Queue Selection**
5:0	DSCP_PRI_2	**User Priority 2 DSCP Value**

00000050 PEM3 DSCP Priority Ingress Mapping VII 25A824A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_5			QUE_CPU_5			QUE_LAN_5		DSCP_PRI_5					
Type	DC		RW			RW			RW		RW					
Reset	0	0	1	0	0	1	0	1	1	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_4			QUE_CPU_4			QUE_LAN_4		DSCP_PRI_4					
Type	DC		RW			RW			RW		RW					
Reset	0	0	1	0	0	1	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_5	**User Priority 5 Priority Tag Value**
26:24	QUE_CPU_5	**User Priority 5 CPU Queue Selectio**
23:22	QUE_LAN_5	**User Priority 5 LAN Queue Selection**
21:16	DSCP_PRI_5	**User Priority 5 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_4	**User Priority 4 Priority Tag Value**

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10:8	QUE_CPU_4	**User Priority 4 CPU Queue Selectio**
7:6	QUE_LAN_4	**User Priority 4 LAN Queue Selection**
5:0	DSCP_PRI_4	**User Priority 4 DSCP Value**

00000054 PEM4 User Priority Egress Mapping IV 3FF836F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		TAG_PRI_7			QUE_CPU_7			QUE_LAN_7		DSCP_PRI_7					
Type	DC		RW			RW			RW		RW					
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1		TAG_PRI_6			QUE_CPU_6			QUE_LAN_6		DSCP_PRI_6					
Type	DC		RW			RW			RW		RW					
Reset	0	0	1	1	0	1	1	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	TAG_PRI_7	**User Priority 7 Priority Tag Value**
26:24	QUE_CPU_7	**User Priority 7 CPU Queue Selectio**
23:22	QUE_LAN_7	**User Priority 7 LAN Queue Selection**
21:16	DSCP_PRI_7	**User Priority 7 DSCP Value**
15:14	REV1	**Reserved**
13:11	TAG_PRI_6	**User Priority 6 Priority Tag Value**
10:8	QUE_CPU_6	**User Priority 6 CPU Queue Selectio**
7:6	QUE_LAN_6	**User Priority 6 LAN Queue Selection**
5:0	DSCP_PRI_6	**User Priority 6 DSCP Value**

00000058 PIM1 DSCP Priority Ingress Mapping I 09000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_09			PRI_DSCP_08			PRI_DSCP_07			PRI_DSCP_06			PRI_DSCP_05[2:1]	
Type	DC		RW			RW			RW			RW			RW	
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DSCP_05[0:0]	PRI_DSCP_04			PRI_DSCP_03			PRI_DSCP_02			PRI_DSCP_01			PRI_DSCP_00		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	PRI_DSCP_09	**User Priority for Differentiated Services Code Point (DSCP) 0b001_001**
26:24	PRI_DSCP_08	**User Priority for DSCP 0b001_000**
23:21	PRI_DSCP_07	**User Priority for DSCP 0b000_111**
20:18	PRI_DSCP_06	**User Priority for DSCP 0b000_110**
17:15	PRI_DSCP_05	**User Priority for DSCP 0b000_101**
14:12	PRI_DSCP_04	**User Priority for DSCP 0b000_100**
11:9	PRI_DSCP_03	**User Priority for DSCP 0b000_011**

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8:6	PRI_DSCP_02	**User Priority for DSCP 0b000_010**
5:3	PRI_DSCP_01	**User Priority for DSCP 0b000_001**
2:0	PRI_DSCP_00	**User Priority for DSCP 0b000_000**

0000005C PIM2 DSCP Priority Ingress Mapping II 12489249

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_19			PRI_DSCP_18			PRI_DSCP_17			PRI_DSCP_16			PRI_DSCP_15[2:1]	
Type	DC		RW			RW			RW			RW			RW	
Reset	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DSCP_15[0:0]	PRI_DSCP_14			PRI_DSCP_13			PRI_DSCP_12			PRI_DSCP_11			PRI_DSCP_10		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	PRI_DSCP_19	**User Priority for DSCP 0b010_011**
26:24	PRI_DSCP_18	**User Priority for DSCP 0b010_010**
23:21	PRI_DSCP_17	**User Priority for DSCP 0b010_001**
20:18	PRI_DSCP_16	**User Priority for DSCP 0b010_000**
17:15	PRI_DSCP_15	**User Priority for DSCP 0b001_111**
14:12	PRI_DSCP_14	**User Priority for DSCP 0b001_110**
11:9	PRI_DSCP_13	**User Priority for DSCP 0b001_101**
8:6	PRI_DSCP_12	**User Priority for DSCP 0b001_100**
5:3	PRI_DSCP_11	**User Priority for DSCP 0b001_011**
2:0	PRI_DSCP_10	**User Priority for DSCP 0b001_010**

00000060 PIM3 DSCP Priority Ingress Mapping III 1B6DB492

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_29			PRI_DSCP_28			PRI_DSCP_27			PRI_DSCP_26			PRI_DSCP_25[2:1]	
Type	DC		RW			RW			RW			RW			RW	
Reset	0	0	0	1	1	0	1	1	0	1	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DSCP_25[0:0]	PRI_DSCP_24			PRI_DSCP_23			PRI_DSCP_22			PRI_DSCP_21			PRI_DSCP_20		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	0	1	1	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	PRI_DSCP_29	**User Priority for DSCP 0b011_101**
26:24	PRI_DSCP_28	**User Priority for DSCP 0b011_100**
23:21	PRI_DSCP_27	**User Priority for DSCP 0b011_011**

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20:18	PRI_DSCP_26	**User Priority for DSCP 0b011_010**
17:15	PRI_DSCP_25	**User Priority for DSCP 0b011_001**
14:12	PRI_DSCP_24	**User Priority for DSCP 0b011_000**
11:9	PRI_DSCP_23	**User Priority for DSCP 0b010_111**
8:6	PRI_DSCP_22	**User Priority for DSCP 0b010_110**
5:3	PRI_DSCP_21	**User Priority for DSCP 0b010_101**
2:0	PRI_DSCP_20	**User Priority for DSCP 0b010_100**

00000064 PIM4 DSCP Priority Ingress Mapping IV 2492491B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_39			PRI_DSCP_38			PRI_DSCP_37			PRI_DSCP_36			PRI_DSCP_35[2:1]	
Type	DC		RW			RW			RW			RW			RW	
Reset	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DSCP_35[0:0]	PRI_DSCP_34			PRI_DSCP_33			PRI_DSCP_32			PRI_DSCP_31			PRI_DSCP_30		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	1	0	0	1	0	0	1	0	0	0	1	1	0	1	1

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	PRI_DSCP_39	**User Priority for DSCP 0b100_111**
26:24	PRI_DSCP_38	**User Priority for DSCP 0b100_110**
23:21	PRI_DSCP_37	**User Priority for DSCP 0b100_101**
20:18	PRI_DSCP_36	**User Priority for DSCP 0b100_100**
17:15	PRI_DSCP_35	**User Priority for DSCP 0b100_011**
14:12	PRI_DSCP_34	**User Priority for DSCP 0b100_010**
11:9	PRI_DSCP_33	**User Priority for DSCP 0b100_001**
8:6	PRI_DSCP_32	**User Priority for DSCP 0b100_000**
5:3	PRI_DSCP_31	**User Priority for DSCP 0b011_111**
2:0	PRI_DSCP_30	**User Priority for DSCP 0b011_110**

00000068 PIM5 DSCP Priority Ingress Mapping V 36B6DB6D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_49			PRI_DSCP_48			PRI_DSCP_47			PRI_DSCP_46			PRI_DSCP_45[2:1]	
Type	DC		RW			RW			RW			RW			RW	
Reset	0	0	1	1	0	1	1	0	1	0	1	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DSCP_45[0:0]	PRI_DSCP_44			PRI_DSCP_43			PRI_DSCP_42			PRI_DSCP_41			PRI_DSCP_40		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1

Bit(s)	Name	Description

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31:30	REV0	**Reserved**
29:27	PRI_DSCP_49	**User Priority for DSCP 0b110_001**
26:24	PRI_DSCP_48	**User Priority for DSCP 0b110_000**
23:21	PRI_DSCP_47	**User Priority for DSCP 0b101_111**
20:18	PRI_DSCP_46	**User Priority for DSCP 0b101_110**
17:15	PRI_DSCP_45	**User Priority for DSCP 0b101_101**
14:12	PRI_DSCP_44	**User Priority for DSCP 0b101_100**
11:9	PRI_DSCP_43	**User Priority for DSCP 0b101_011**
8:6	PRI_DSCP_42	**User Priority for DSCP 0b101_010**
5:3	PRI_DSCP_41	**User Priority for DSCP 0b101_001**
2:0	PRI_DSCP_40	**User Priority for DSCP 0b101_000**

0000006C PIM6 DSCP Priority Ingress Mapping VI 3FFF6DB6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_59			PRI_DSCP_58			PRI_DSCP_57			PRI_DSCP_56			PRI_DSCP_55[2:1]	
Type	DC		RW			RW			RW			RW			RW	
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DSCP_55[0:0]	PRI_DSCP_54			PRI_DSCP_53			PRI_DSCP_52			PRI_DSCP_51			PRI_DSCP_50		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0

Bit(s)	Name	Description
31:30	REV0	**Reserved**
29:27	PRI_DSCP_59	**User Priority for DSCP 0b111_011**
26:24	PRI_DSCP_58	**User Priority for DSCP 0b111_010**
23:21	PRI_DSCP_57	**User Priority for DSCP 0b111_001**
20:18	PRI_DSCP_56	**User Priority for DSCP 0b111_000**
17:15	PRI_DSCP_55	**User Priority for DSCP 0b110_111**
14:12	PRI_DSCP_54	**User Priority for DSCP 0b110_110**
11:9	PRI_DSCP_53	**User Priority for DSCP 0b110_101**
8:6	PRI_DSCP_52	**User Priority for DSCP 0b110_100**
5:3	PRI_DSCP_51	**User Priority for DSCP 0b110_011**
2:0	PRI_DSCP_50	**User Priority for DSCP 0b110_010**

00000070 PIM7 DSCP Priority Ingress Mapping VII 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0[19:4]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[3:0]				PRI_DSCP_63			PRI_DSCP_62			PRI_DSCP_61			PRI_DSCP_60		
Type	DC				RW			RW			RW			RW		
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

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Bit(s)	Name	Description
31:12	REV0	**Reserved**
11:9	PRI_DSCP_63	**User Priority for DSCP 0b111_111**
8:6	PRI_DSCP_62	**User Priority for DSCP 0b111_110**
5:3	PRI_DSCP_61	**User Priority for DSCP 0b111_101**
2:0	PRI_DSCP_60	**User Priority for DSCP 0b111_100**

00000074 ATA1 Address Table Access I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[47:40] / Destination IP(DIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[39:32] / Destination IP(DIP) Address [23:16]**
15:8	BYTE_2	**MAC Address[31:24] / Destination IP(DIP) Address [15:8]**
7:0	BYTE_3	**MAC Address[23:16] / Destination IP(DIP) Address [7:0]**

00000078 ATA2 Address Table Access II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[15:8] / Source IP(SIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[7:0] / Source IP(SIP) Address [23:16]**
15:8	BYTE_2	**SIP Address [15: 8] or** bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table.
7:0	BYTE_3	**SIP Address[7:0] or CVID[7:0]**

0000007C ATWD Address Table Write Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	**Table Write Data**

00000080 ATC Address Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				ADDR											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSY	SRCH_END	SRCH_HIT	ADDR_INVLD	AC_MAT				REV1		AC_SAT		REV2	AC_CMD		
Type	W1C	RO	RO	RO	RW				DC		RW		DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	**Reserved**
27:16	ADDR	**Address Table Access Index** The actual address table access index which is calculated from a 48-bit MAC address, a 32-bit DIP, and a SIP address. (for debugging purposes)
15	BUSY	**Address Table Is Busy** SW can set this bit to 1 only if this bit is reset. After ATWD registers are written and this bit is set, this chip will perform the corresponding function according to AC_CMD, AC_SAT, and AC_MAT included in this register.
14	SRCH_END	**Linear Search End** The linear search has reached the index end of the address table.
13	SRCH_HIT	**Linear Search Hit** The linear search has find the target based on AC_MAT and return the data on TSRA1,2 and ATRD.
12	ADDR_INVLD	**Address Entry is not Valid** The specified entry is not valid for read or removal access. The specified entry can not be modified or added for write access. (hash collision)
11:8	AC_MAT	**Address Table Multiple Access Target** Whenever MATC register is written and bit.15 is set, this chip will perform the corresponding function on the Address table based on AC_CMD bits. 4'b0000: All MAC address entries 4'b0001: All DIP/GA address entries 4'b0010: All SIP address entries 4'b0011: All valid address entry 4'b0100: All non-static MAC address entries. 4'b0101: All non-static DIP address entries. 4'b0110: All static MAC address entries 4'b0111: All static DIP address entries 4'b1000: All relative SIP address entries based on the specific DIP from ATA2 register. 4'b1001: All relative SIP address entries based on the specific SIP from ATA2 register. 4'b1010: All MAC Address entries with the customer VID specified in ATA2.CVID[11:0] 4'b1010: All MAC address entries with the Filter ID specified in ATA2.FID[2:0] 4'b1100: All MAC Address entries with the source ports specified in ATA1.PORT[7:0] 4'b1101 to 4'b1111: Reserved
7:6	REV1	**Reserved**

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5:4	AC_SAT	**Address Table Single Access Target** Whenever MATC register is written and bit.31 is set, this chip will perform the corresponding function on the Address table based on FUNC bits. 2'b00: Specified MAC address entry 2'b01: Specified DIP address entry 2'b10: Specified SIP address entry 2'b11: Specified address entry(read only)
3	REV2	**Reserved**
2:0	AC_CMD	**Address Table Access Command** 3'b000: Read command (single entry) 3'b001: Write command (single entry) NOTE: Supports modify, add, and remove 3'b010: Clean command (multiple entries) 3'b011: Reserved 3'b100: Start Search command (reset to 1st entry) 3'b101: Next Search command (next entry) 3'b110 to 3'b111: Reserved

00000084 TSRA1 Table Search Read Address I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[47:40] / Destination IP(DIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[39:32] / Destination IP(DIP) Address [23:16]**
15:8	BYTE_2	**MAC Address[31:24] / Destination IP(DIP) Address [15:8]**
7:0	BYTE_3	**MAC Address[23:16] / Destination IP(DIP) Address [7:0]**

00000088 TSRA2 Table Search Read Address II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	**MAC Address[15:8] / Source IP(SIP) Address [31:24]**
23:16	BYTE_1	**MAC Address[7:0] / Source IP(SIP) Address [23:16]**
15:8	BYTE_2	**SIP Address [15: 8] or** bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table.

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7:0	BYTE_3	**SIP Address[7:0] or CVID[7:0]**

0000008C ATRD Address Table Read Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDATA[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDATA[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RDATA	**Table Read Data**

00000090 VTCR VLAN Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_INVLD
Type	W1C	DC														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BUSY	**VLAN Table Is Busy** SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.
30:17	REV0	**Reserved**
16	IDX_INVLD	**Entry is not Valid** This index for the access control is out of the valid index.
15:12	FUNC	**Access Control Function** Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits . 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry. 4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved
11:0	VID	**1. VLAN ID Number: 0x0 to 0x1F (16)** 2. ACL table index: 0x0 to 0x3F (64)

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3. ACL mask control: 0x0 to 0x3F (32 or 64)

00000094 VAWD1 VLAN and ACL Write Data I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	**VLAN Table Write Data I**

00000098 VAWD2 VLAN and ACL Write Data II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	**VLAN Table Write Data II**

0000009C TRTCM Two Rate Three Color Mark 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRTCM_EN	REV0[30:16]														
Type	DC	DC														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0[15:0]															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TRTCM_EN	**Two Rate Three Color Marker (trTCM) Enable** When this bit is enabled, the meter table will be updated based on Peak Information Rate (PIR) and Committed Information Rate (CIR). The color marker will also be enabled when ACL is hit. 0: Disable 1: Enable
30:0	REV0	**Reserved**

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000000A0 AAC Address Age Control 00095001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0											AGE_DIS	AGE_CNT[7:4]			
Type	DC											RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_CNT[3:0]				AGE_UNIT											
Type	RW				RW											
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:21	REV0	**Reserved**
20	AGE_DIS	**Address Table Aging Disable** Disable or pause MAC address aging.
19:12	AGE_CNT	**Address Table Age Count** This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds.
11:0	AGE_UNIT	**Address Table Age Unit** The applied aging unit is equal to (AGE_UNIT+1) seconds.

000000A8 AISR_EXT ACL Extension Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_ISR_EXT[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACL_ISR_EXT[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ACL_ISR_EXT	**ACL Interrupt Status for entry 32~63** (if total entry of ACL table is 32, the register will be set to 0)

000000AC MISR MLDv2 Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MLDv2_ISR[31:16]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MLDv2_ISR[15:0]															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MLDv2_ISR	**MLDv2 Interrupt Status** (the bit [31:16] is only for total entries of MLDv2 table is 32) 0: Not hit 1: Hit

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00001000 MMSCR0_Q0P0 Max-Min Scheduler Control Register 0 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P0				MIN_RATE_CTRL_EXP_Q0_P0					MIN_RATE_CTRL_MAN_Q0_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P0	**Port 0 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P0	**Port 0 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass (infinite rate). 1: Queue 0 min. rate limit control is enabled.
11:8	MIN_RATE_CTRL_EXP_Q0_P0	**Exponent part of Port 0 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P0	**Mantissa part of Port 0 Queue 0 min. shaper rate limit control** Value range: 1..100

00001004 MMSCR1_Q0P0 Max-Min Scheduler Control Register 1 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P0				MAX_WEIGHT_Q0_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P0				MAX_RATE_CTRL_EXP_Q0_P0					MAX_RATE_CTRL_MAN_Q0_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P0	**Port 0 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P0	**Port 0 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**

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15	MAX_RATE_EN_Q0_P0	**Port 0 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate). 1: Queue 0 maximum shaper rate limit is enabled.
11:8	MAX_RATE_CTRL_EXP_Q0_P0	**Exponent part of Port 0 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P0	**Mantissa part of Port 0 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001008 MMSCR0_Q1P0 Max-Min Scheduler Control Register 0 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P0				MIN_RATE_CTRL_EXP_Q1_P0					MIN_RATE_CTRL_MAN_Q1_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P0	**Port 0 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P0	**Port 0 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P0	**Exponent part of Port 0 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P0	**Mantissa part of Port 0 Queue 1 min. shaper rate limit control** Value range: 1..127

0000100C MMSCR1_Q1P0 Max-Min Scheduler Control Register 1 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P0				MAX_WEIGHT_Q1_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P0				MAX_RATE_CTRL_EXP_Q1_P0					MAX_RATE_CTRL_MAN_Q1_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P0	**Port 0 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P0	**Port 0 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P0	**Port 0 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P0	**Exponent part of Port 0 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P0	**Mantissa part of Port 0 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001010 MMSCR0_Q2P0 Max-Min Scheduler Control Register 0 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P0				MIN_RATE_CTRL_EXP_Q2_P0					MIN_RATE_CTRL_MAN_Q2_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P0	**Port 0 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P0	**Port 0 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P0	**Exponent part of Port 0 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P0	**Mantissa part of Port 0 Queue 2 min. shaper rate limit control** Value range: 1..127

00001014 MMSCR1_Q2P0 Max-Min Scheduler Control Register 1 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P0				MAX_WEIGHT_Q2_P0											

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Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P0				MAX_RATE_CTRL_EXP_Q2_P0					MAX_RATE_CTRL_MAN_Q2_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P0	**Port 0 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P0	**Port 0 Queue 2 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P0	**Port 0 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P0	**Exponent part of Port 0 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P0	**Mantissa part of Port 0 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001018 MMSCR0_Q3P0 Max-Min Scheduler Control Register 0 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P0				MIN_RATE_CTRL_EXP_Q3_P0					MIN_RATE_CTRL_MAN_Q3_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P0	**Port 0 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P0	**Port 0 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P0	**Exponent part of Port 0 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P0	**Mantissa part of Port 0 Queue 3 min. shaper rate limit control** Value range: 1..127

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0000101C MMSCR1_Q3P0 Max-Min Scheduler Control Register 1 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P0				MAX_WEIGHT_Q3_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P0				MAX_RATE_CTRL_EXP_Q3_P0					MAX_RATE_CTRL_MAN_Q3_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P0	**Port 0 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P0	**Port 0 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P0	**Port 0 Queue 3 maximum shaper rate limit control is enabled.** 0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P0	**Exponent part of Port 0 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P0	**Mantissa part of Port 0 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001020 MMSCR0_Q4P0 Max-Min Scheduler Control Register 0 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P0				MIN_RATE_CTRL_EXP_Q4_P0					MIN_RATE_CTRL_MAN_Q4_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P0	**Port 0 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P0	**Port 0 Queue 4 minimum shaper rate limit control is enabled.**

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		0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P0	**Exponent part of Port 0 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P0	**Mantissa part of Port 0 Queue 4 min. shaper rate limit control** Value range: 1..127

00001024 MMSCR1_Q4P0 Max-Min Scheduler Control Register 1 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P0				MAX_WEIGHT_Q4_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P0				MAX_RATE_CTRL_EXP_Q4_P0					MAX_RATE_CTRL_MAN_Q4_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P0	**Port 0 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P0	**Port 0 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P0	**Port 0 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P0	**Exponent part of Port 0 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P0	**Mantissa part of Port 0 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001028 MMSCR0_Q5P0 Max-Min Scheduler Control Register 0 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P0				MIN_RATE_CTRL_EXP_Q5_P0					MIN_RATE_CTRL_MAN_Q5_P0						
Type	RW				RW					RW						

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Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P0	**Port 0 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P0	**Port 0 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P0	**Exponent part of Port 0 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P0	**Mantissa part of Port 0 Queue 5 min. shaper rate limit control** Value range: 1..127

0000102C MMSCR1_Q5P0 Max-Min Scheduler Control Register 1 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P0				MAX_WEIGHT_Q5_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P0				MAX_RATE_CTRL_EXP_Q5_P0					MAX_RATE_CTRL_MAN_Q5_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P0	**Port 0 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P0	**Port 0 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P0	**Port 0 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P0	**Exponent part of Port 0 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P0	**Mantissa part of Port 0 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001030 MMSCR0_Q6P0 Max-Min Scheduler Control Register 0 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WR															

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	R_Q6_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P0				MIN_RATE_CTRL_EXP_Q6_P0					MIN_RATE_CTRL_MAN_Q6_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P0	**Port 0 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P0	**Port 0 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P0	**Exponent part of Port 0 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P0	**Mantissa part of Port 0 Queue 6 min. shaper rate limit control** Value range: 1..127

00001034 MMSCR1_Q6P0 Max-Min Scheduler Control Register 1 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P0				MAX_WEIGHT_Q6_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P0				MAX_RATE_CTRL_EXP_Q6_P0					MAX_RATE_CTRL_MAN_Q6_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P0	**Port 0 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P0	**Port 0 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P0	**Port 0 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P0	**Exponent part of Port 0 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P0	**Mantissa part of Port 0 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001038 MMSCR0_Q7P0 Max-Min Scheduler Control Register 0 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P0				MIN_RATE_CTRL_EXP_Q7_P0					MIN_RATE_CTRL_MAN_Q7_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P0	**Port 0 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P0	**Port 0 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P0	**Exponent part of Port 0 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P0	**Mantissa part of Port 0 Queue 7 min. shaper rate limit control** Value range: 1..127

0000103C MMSCR1_Q7P0 Max-Min Scheduler Control Register 1 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P0				MAX_WEIGHT_Q7_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P0				MAX_RATE_CTRL_EXP_Q7_P0					MAX_RATE_CTRL_MAN_Q7_P0						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P0	**Port 0 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P0	**Port 0 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**

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15	MAX_RATE_EN_Q7_P0	**Port 0 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P0	**Exponent part of Port 0 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P0	**Mantissa part of Port 0 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001040 ERLCR_P0 Egress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P0			EGC_RATE_CIR_16_P0	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0				EGC_TB_EN_P0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P0	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P0	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P0	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P0	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0	**Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and

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Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

000010E0 GERLCR Global Egress Rate Limit Control Register 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EGC_MFRM_EX	EGC_IPG_OP	EGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
9	EGC_MFRM_EX	**When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)** 0: Include management frames 1: Exclude management frames
8	EGC_IPG_OP	**Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	EGC_IPG_BYTE	**Egress Rate IPG Byte Count** Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC (default) 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble

00001100 MMSCR0_Q0P1 Max-Min Scheduler Control Register 0 of Queue 0/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P1				MIN_RATE_CTRL_EXP_Q0_P1					MIN_RATE_CTRL_MAN_Q0_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P1	**Port 1 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P1	**Port 1 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 min. rate limit control enable

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11:8	MIN_RATE_CTRL_EXP_Q0_P1	**Exponent part of Port 1 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P1	**Mantissa part of Port 1 Queue 0 min. shaper rate limit control** Value range: 1..100

00001104 MMSCR1_Q0P1 Max-Min Scheduler Control Register 1 of Queue 0/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P1				MAX_WEIGHT_Q0_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P1				MAX_RATE_CTRL_EXP_Q0_P1					MAX_RATE_CTRL_MAN_Q0_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P1	**Port 1 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P1	**Port 1 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P1	**Port 1 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q0_P1	**Exponent part of Port 1 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P1	**Mantissa part of Port 1 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001108 MMSCR0_Q1P1 Max-Min Scheduler Control Register 0 of Queue 1/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P1				MIN_RATE_CTRL_EXP_Q1_P1					MIN_RATE_CTRL_MAN_Q1_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P1	**Port 1 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P1	**Port 1 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P1	**Exponent part of Port 1 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P1	**Mantissa part of Port 1 Queue 1 min. shaper rate limit control** Value range: 1..127

0000110C MMSCR1_Q1P1 Max-Min Scheduler Control Register 1 of Queue 1/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P1				MAX_WEIGHT_Q1_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P1				MAX_RATE_CTRL_EXP_Q1_P1					MAX_RATE_CTRL_MAN_Q1_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P1	**Port 1 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P1	**Port 1 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P1	**Port 1 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P1	**Exponent part of Port 1 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P1	**Mantissa part of Port 1 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001110 MMSCR0_Q2P1 Max-Min Scheduler Control Register 0 of Queue 2/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P1															
Type	RW															

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Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P1				MIN_RATE_CTRL_EXP_Q2_P1					MIN_RATE_CTRL_MAN_Q2_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P1	**Port 1 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P1	**Port 1 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 2 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P1	**Exponent part of Port 1 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P1	**Mantissa part of Port 1 Queue 2 min. shaper rate limit control** Value range: 1..127

00001114 MMSCR1_Q2P1 Max-Min Scheduler Control Register 1 of Queue 2/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P1				MAX_WEIGHT_Q2_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P1				MAX_RATE_CTRL_EXP_Q2_P1					MAX_RATE_CTRL_MAN_Q2_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P1	**Port 1 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P1	**Port 1 Queue 2 weighted value for maximum WFQ weighted value is (q2_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P1	**Port 1 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P1	**Exponent part of Port 1 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P1	**Mantissa part of Port 1 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001118 MMSCR0_Q3P1 Max-Min Scheduler Control Register 0 of Queue 3/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P1				MIN_RATE_CTRL_EXP_Q3_P1					MIN_RATE_CTRL_MAN_Q3_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P1	**Port 1 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P1	**Port 1 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P1	**Exponent part of Port 1 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P1	**Mantissa part of Port 1 Queue 3 min. shaper rate limit control** Value range: 1..127

0000111C MMSCR1_Q3P1 Max-Min Scheduler Control Register 1 of Queue 3/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P1				MAX_WEIGHT_Q3_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P1				MAX_RATE_CTRL_EXP_Q3_P1					MAX_RATE_CTRL_MAN_Q3_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P1	**Port 1 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P1	**Port 1 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P1	**Port 1 Queue 3 maximum shaper rate limit control is enabled.** 0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P1	**Exponent part of Port 1 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P1	**Mantissa part of Port 1 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001120 MMSCR0_Q4P1 Max-Min Scheduler Control Register 0 of Queue 4/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P1				MIN_RATE_CTRL_EXP_Q4_P1					MIN_RATE_CTRL_MAN_Q4_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P1	**Port 1 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P1	**Port 1 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P1	**Exponent part of Port 1 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P1	**Mantissa part of Port 1 Queue 4 min. shaper rate limit control** Value range: 1..127

00001124 MMSCR1_Q4P1 Max-Min Scheduler Control Register 1 of Queue 4/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P1				MAX_WEIGHT_Q4_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P1				MAX_RATE_CTRL_EXP_Q4_P1					MAX_RATE_CTRL_MAN_Q4_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description

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31	MAX_SP_WFQ_Q4_P1	**Port 1 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P1	**Port 1 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P1	**Port 1 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P1	**Exponent part of Port 1 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P1	**Mantissa part of Port 1 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001128 MMSCR0_Q5P1 Max-Min Scheduler Control Register 0 of Queue 5/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P1				MIN_RATE_CTRL_EXP_Q5_P1					MIN_RATE_CTRL_MAN_Q5_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P1	**Port 1 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P1	**Port 1 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P1	**Exponent part of Port 1 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P1	**Mantissa part of Port 1 Queue 5 min. shaper rate limit control** Value range: 1..127

0000112C MMSCR1_Q5P1 Max-Min Scheduler Control Register 1 of Queue 5/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P1				MAX_WEIGHT_Q5_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	MAX_RATE_EN_Q5_P1				MAX_RATE_CTRL_EXP_Q5_P1					MAX_RATE_CTRL_MAN_Q5_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P1	**Port 1 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P1	**Port 1 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P1	**Port 1 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P1	**Exponent part of Port 1 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P1	**Mantissa part of Port 1 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001130 MMSCR0_Q6P1 Max-Min Scheduler Control Register 0 of Queue 6/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P1				MIN_RATE_CTRL_EXP_Q6_P1					MIN_RATE_CTRL_MAN_Q6_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P1	**Port 1 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P1	**Port 1 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P1	**Exponent part of Port 1 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P1	**Mantissa part of Port 1 Queue 6 min. shaper rate limit control** Value range: 1..127

00001134 MMSCR1_Q6P1 Max-Min Scheduler Control Register 1 of Queue 6/Port 00000000

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1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P1				MAX_WEIGHT_Q6_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P1				MAX_RATE_CTRL_EXP_Q6_P1					MAX_RATE_CTRL_MAN_Q6_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P1	**Port 1 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P1	**Port 1 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P1	**Port 1 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P1	**Exponent part of Port 1 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P1	**Mantissa part of Port 1 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001138 MMSCR0_Q7P1 Max-Min Scheduler Control Register 0 of Queue 7/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P1				MIN_RATE_CTRL_EXP_Q7_P1					MIN_RATE_CTRL_MAN_Q7_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P1	**Port 1 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P1	**Port 1 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 min. rate limit control enable

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11:8	MIN_RATE_CTRL_EXP_Q7_P1	**Exponent part of Port 1 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P1	**Mantissa part of Port 1 Queue 7 min. shaper rate limit control** Value range: 1..127

0000113C MMSCR1_Q7P1 Max-Min Scheduler Control Register 1 of Queue 7/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P1				MAX_WEIGHT_Q7_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P1				MAX_RATE_CTRL_EXP_Q7_P1					MAX_RATE_CTRL_MAN_Q7_P1						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P1	**Port 1 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P1	**Port 1 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P1	**Port 1 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P1	**Exponent part of Port 1 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P1	**Mantissa part of Port 1 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001140 ERLCR_P1 Egress Rate Limit Control Register of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P1			EGC_RATE_CIR_16_P1	EG_RATE_LIMIT_EXP_P1_EGC_TB_T_P1				EGC_TB_EN_P1	EG_RATE_LIMIT_MAN_P1_EGC_TB_CBS_P1						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support**

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	P1	**32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P1	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P1	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P1_EGC_TB_T_P1	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P1	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P1_EGC_TB_CBS_P1	**Mantissa part of port 1 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001200 MMSCR0_Q0P2 Max-Min Scheduler Control Register 0 of Queue 0/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P2				MIN_RATE_CTRL_EXP_Q0_P2					MIN_RATE_CTRL_MAN_Q0_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P2	**Port 2 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P2	**Port 2 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 0 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q0_P2	**Exponent part of Port 2 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P2	**Mantissa part of Port 2 Queue 0 min. shaper rate limit control** Value range: 1..100

00001204 MMSCR1_Q0P2 Max-Min Scheduler Control Register 1 of Queue 0/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P2				MAX_WEIGHT_Q0_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P2				MAX_RATE_CTRL_EXP_Q0_P2					MAX_RATE_CTRL_MAN_Q0_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P2	**Port 2 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P2	**Port 2 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P2	**Port 2 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q0_P2	**Exponent part of Port 2 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P2	**Mantissa part of Port 2 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001208 MMSCR0_Q1P2 Max-Min Scheduler Control Register 0 of Queue 1/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P2				MIN_RATE_CTRL_EXP_Q1_P2					MIN_RATE_CTRL_MAN_Q1_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P2	**Port 2 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P2	**Port 2 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P2	**Exponent part of Port 2 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P2	**Mantissa part of Port 2 Queue 1 min. shaper rate limit control** Value range: 1..127

0000120C MMSCR1_Q1P2 Max-Min Scheduler Control Register 1 of Queue 1/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P2				MAX_WEIGHT_Q1_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P2				MAX_RATE_CTRL_EXP_Q1_P2					MAX_RATE_CTRL_MAN_Q1_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P2	**Port 2 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P2	**Port 2 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P2	**Port 2 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P2	**Exponent part of Port 2 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P2	**Mantissa part of Port 2 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001210 MMSCR0_Q2P2 Max-Min Scheduler Control Register 0 of Queue 2/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P2															

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Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P2				MIN_RATE_CTRL_EXP_Q2_P2					MIN_RATE_CTRL_MAN_Q2_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P2	**Port 2 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P2	**Port 2 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 2 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P2	**Exponent part of Port 2 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P2	**Mantissa part of Port 2 Queue 2 min. shaper rate limit control** Value range: 1..127

00001214 MMSCR1_Q2P2 Max-Min Scheduler Control Register 1 of Queue 2/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P2				MAX_WEIGHT_Q2_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P2				MAX_RATE_CTRL_EXP_Q2_P2					MAX_RATE_CTRL_MAN_Q2_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P2	**Port 2 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P2	**Port 2 Queue 2 weighted value for maximum WFQ weighted value is (q2_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P2	**Port 2 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P2	**Exponent part of Port 2 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P2	**Mantissa part of Port 2 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001218 MMSCR0_Q3P2 Max-Min Scheduler Control Register 0 of Queue 3/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P2				MIN_RATE_CTRL_EXP_Q3_P2					MIN_RATE_CTRL_MAN_Q3_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P2	**Port 2 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P2	**Port 2 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P2	**Exponent part of Port 2 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P2	**Mantissa part of Port 2 Queue 3 min. shaper rate limit control** Value range: 1..127

0000121C MMSCR1_Q3P2 Max-Min Scheduler Control Register 1 of Queue 3/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P2				MAX_WEIGHT_Q3_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P2				MAX_RATE_CTRL_EXP_Q3_P2					MAX_RATE_CTRL_MAN_Q3_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P2	**Port 2 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P2	**Port 2 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P2	**Port 2 Queue 3 maximum shaper rate limit control is enabled.**

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		0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P2	**Exponent part of Port 2 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P2	**Mantissa part of Port 2 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001220 MMSCR0_Q4P2 Max-Min Scheduler Control Register 0 of Queue 4/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P2				MIN_RATE_CTRL_EXP_Q4_P2					MIN_RATE_CTRL_MAN_Q4_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P2	**Port 2 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P2	**Port 2 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P2	**Exponent part of Port 2 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P2	**Mantissa part of Port 2 Queue 4 min. shaper rate limit control** Value range: 1..127

00001224 MMSCR1_Q4P2 Max-Min Scheduler Control Register 1 of Queue 4/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P2				MAX_WEIGHT_Q4_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P2				MAX_RATE_CTRL_EXP_Q4_P2					MAX_RATE_CTRL_MAN_Q4_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P2	**Port 2 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P2	**Port 2 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P2	**Port 2 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P2	**Exponent part of Port 2 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P2	**Mantissa part of Port 2 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001228 MMSCR0_Q5P2 Max-Min Scheduler Control Register 0 of Queue 5/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P2				MIN_RATE_CTRL_EXP_Q5_P2					MIN_RATE_CTRL_MAN_Q5_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P2	**Port 2 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P2	**Port 2 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P2	**Exponent part of Port 2 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P2	**Mantissa part of Port 2 Queue 5 min. shaper rate limit control** Value range: 1..127

0000122C MMSCR1_Q5P2 Max-Min Scheduler Control Register 1 of Queue 5/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P2				MAX_WEIGHT_Q5_P2											
Type	RW				RW											

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Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P2				MAX_RATE_CTRL_EXP_Q5_P2					MAX_RATE_CTRL_MAN_Q5_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P2	**Port 2 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P2	**Port 2 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P2	**Port 2 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P2	**Exponent part of Port 2 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P2	**Mantissa part of Port 2 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001230 MMSCR0_Q6P2 Max-Min Scheduler Control Register 0 of Queue 6/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P2				MIN_RATE_CTRL_EXP_Q6_P2					MIN_RATE_CTRL_MAN_Q6_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P2	**Port 2 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P2	**Port 2 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P2	**Exponent part of Port 2 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P2	**Mantissa part of Port 2 Queue 6 min. shaper rate limit control** Value range: 1..127

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00001234 MMSCR1_Q6P2 Max-Min Scheduler Control Register 1 of Queue 6/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P2				MAX_WEIGHT_Q6_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P2				MAX_RATE_CTRL_EXP_Q6_P2					MAX_RATE_CTRL_MAN_Q6_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P2	**Port 2 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P2	**Port 2 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P2	**Port 2 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P2	**Exponent part of Port 2 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P2	**Mantissa part of Port 2 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001238 MMSCR0_Q7P2 Max-Min Scheduler Control Register 0 of Queue 7/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P2				MIN_RATE_CTRL_EXP_Q7_P2					MIN_RATE_CTRL_MAN_Q7_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P2	**Port 2 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P2	**Port 2 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P2	**Exponent part of Port 2 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P2	**Mantissa part of Port 2 Queue 7 min. shaper rate limit control** Value range: 1..127

0000123C MMSCR1_Q7P2 Max-Min Scheduler Control Register 1 of Queue 7/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P2				MAX_WEIGHT_Q7_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P2				MAX_RATE_CTRL_EXP_Q7_P2					MAX_RATE_CTRL_MAN_Q7_P2						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P2	**Port 2 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P2	**Port 2 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P2	**Port 2 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P2	**Exponent part of Port 2 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P2	**Mantissa part of Port 2 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001240 ERLCR_P2 Egress Rate Limit Control Register of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P2			EGC_RATE_CIR_16_P2	EG_RATE_LIMIT_EXP_P2_EGC_TB_T_P2				EGC_TB_EN_P2	EG_RATE_LIMIT_MAN_P2_EGC_TB_CBS_P2						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:16	EGC_RATE_CIR_15_0_P2	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P2	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P2	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P2_EGC_TB_T_P2	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P2	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P2_EGC_TB_CBS_P2	**Mantissa part of port 2 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001300 MMSCR0_Q0P3 Max-Min Scheduler Control Register 0 of Queue 0/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P3				MIN_RATE_CTRL_EXP_Q0_P3					MIN_RATE_CTRL_MAN_Q0_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P3	**Port 3 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P3	**Port 3 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 0 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q0_P3	**Exponent part of Port 3 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P3	**Mantissa part of Port 3 Queue 0 min. shaper rate limit control** Value range: 1..100

00001304 MMSCR1_Q0P3 Max-Min Scheduler Control Register 1 of Queue 0/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P3				MAX_WEIGHT_Q0_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P3				MAX_RATE_CTRL_EXP_Q0_P3					MAX_RATE_CTRL_MAN_Q0_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P3	**Port 3 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P3	**Port 3 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P3	**Port 3 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q0_P3	**Exponent part of Port 3 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P3	**Mantissa part of Port 3 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001308 MMSCR0_Q1P3 Max-Min Scheduler Control Register 0 of Queue 1/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P3				MIN_RATE_CTRL_EXP_Q1_P3					MIN_RATE_CTRL_MAN_Q1_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P3	**Port 3 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P3	**Port 3 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P3	**Exponent part of Port 3 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P3	**Mantissa part of Port 3 Queue 1 min. shaper rate limit control** Value range: 1..127

0000130C MMSCR1_Q1P3 Max-Min Scheduler Control Register 1 of Queue 1/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P3				MAX_WEIGHT_Q1_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P3				MAX_RATE_CTRL_EXP_Q1_P3					MAX_RATE_CTRL_MAN_Q1_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P3	**Port 3 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P3	**Port 3 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P3	**Port 3 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P3	**Exponent part of Port 3 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P3	**Mantissa part of Port 3 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001310 MMSCR0_Q2P3 Max-Min Scheduler Control Register 0 of Queue 2/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P3															

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Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P3				MIN_RATE_CTRL_EXP_Q2_P3					MIN_RATE_CTRL_MAN_Q2_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P3	**Port 3 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P3	**Port 3 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 2 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P3	**Exponent part of Port 3 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P3	**Mantissa part of Port 3 Queue 2 min. shaper rate limit control** Value range: 1..127

00001314 MMSCR1_Q2P3 Max-Min Scheduler Control Register 1 of Queue 2/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P3				MAX_WEIGHT_Q2_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P3				MAX_RATE_CTRL_EXP_Q2_P3					MAX_RATE_CTRL_MAN_Q2_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P3	**Port 3 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P3	**Port 3 Queue 2 weighted value for maximum WFQ weighted value is (q2_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P3	**Port 3 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P3	**Exponent part of Port 3 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P3	**Mantissa part of Port 3 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001318 MMSCR0_Q3P3 Max-Min Scheduler Control Register 0 of Queue 3/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P3				MIN_RATE_CTRL_EXP_Q3_P3					MIN_RATE_CTRL_MAN_Q3_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P3	**Port 3 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P3	**Port 3 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P3	**Exponent part of Port 3 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P3	**Mantissa part of Port 3 Queue 3 min. shaper rate limit control** Value range: 1..127

0000131C MMSCR1_Q3P3 Max-Min Scheduler Control Register 1 of Queue 3/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P3				MAX_WEIGHT_Q3_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P3				MAX_RATE_CTRL_EXP_Q3_P3					MAX_RATE_CTRL_MAN_Q3_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P3	**Port 3 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P3	**Port 3 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P3	**Port 3 Queue 3 maximum shaper rate limit control is enabled.**

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		0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P3	**Exponent part of Port 3 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P3	**Mantissa part of Port 3 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001320 MMSCR0_Q4P3 Max-Min Scheduler Control Register 0 of Queue 4/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P3				MIN_RATE_CTRL_EXP_Q4_P3					MIN_RATE_CTRL_MAN_Q4_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P3	**Port 3 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P3	**Port 3 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P3	**Exponent part of Port 3 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P3	**Mantissa part of Port 3 Queue 4 min. shaper rate limit control** Value range: 1..127

00001324 MMSCR1_Q4P3 Max-Min Scheduler Control Register 1 of Queue 4/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P3				MAX_WEIGHT_Q4_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P3				MAX_RATE_CTRL_EXP_Q4_P3					MAX_RATE_CTRL_MAN_Q4_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P3	**Port 3 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P3	**Port 3 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P3	**Port 3 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P3	**Exponent part of Port 3 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P3	**Mantissa part of Port 3 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001328 MMSCR0_Q5P3 Max-Min Scheduler Control Register 0 of Queue 5/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P3				MIN_RATE_CTRL_EXP_Q5_P3					MIN_RATE_CTRL_MAN_Q5_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P3	**Port 3 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P3	**Port 3 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P3	**Exponent part of Port 3 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P3	**Mantissa part of Port 3 Queue 5 min. shaper rate limit control** Value range: 1..127

0000132C MMSCR1_Q5P3 Max-Min Scheduler Control Register 1 of Queue 5/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P3				MAX_WEIGHT_Q5_P3											
Type	RW				RW											

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Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P3				MAX_RATE_CTRL_EXP_Q5_P3					MAX_RATE_CTRL_MAN_Q5_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P3	**Port 3 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P3	**Port 3 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P3	**Port 3 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P3	**Exponent part of Port 3 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P3	**Mantissa part of Port 3 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001330 MMSCR0_Q6P3 Max-Min Scheduler Control Register 0 of Queue 6/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P3				MIN_RATE_CTRL_EXP_Q6_P3					MIN_RATE_CTRL_MAN_Q6_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P3	**Port 3 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P3	**Port 3 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P3	**Exponent part of Port 3 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P3	**Mantissa part of Port 3 Queue 6 min. shaper rate limit control** Value range: 1..127

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00001334 MMSCR1_Q6P3 Max-Min Scheduler Control Register 1 of Queue 6/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P3				MAX_WEIGHT_Q6_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P3				MAX_RATE_CTRL_EXP_Q6_P3					MAX_RATE_CTRL_MAN_Q6_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P3	**Port 3 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P3	**Port 3 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P3	**Port 3 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P3	**Exponent part of Port 3 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P3	**Mantissa part of Port 3 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001338 MMSCR0_Q7P3 Max-Min Scheduler Control Register 0 of Queue 7/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P3				MIN_RATE_CTRL_EXP_Q7_P3					MIN_RATE_CTRL_MAN_Q7_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P3	**Port 3 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P3	**Port 3 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P3	**Exponent part of Port 3 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P3	**Mantissa part of Port 3 Queue 7 min. shaper rate limit control** Value range: 1..127

0000133C MMSCR1_Q7P3 Max-Min Scheduler Control Register 1 of Queue 7/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P3				MAX_WEIGHT_Q7_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P3				MAX_RATE_CTRL_EXP_Q7_P3					MAX_RATE_CTRL_MAN_Q7_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P3	**Port 3 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P3	**Port 3 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P3	**Port 3 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P3	**Exponent part of Port 3 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P3	**Mantissa part of Port 3 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001340 ERLCR_P3 Egress Rate Limit Control Register of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P3			EGC_RATE_CIR_16_P3	EG_RATE_LIMIT_EXP_P3_EGC_TB_T_P3				EGC_TB_EN_P3	EG_RATE_LIMIT_MAN_P3_EGC_TB_CBS_P3						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:16	EGC_RATE_CIR_15_0_P3	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P3	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P3	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P3_EGC_TB_T_P3	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P3	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P3_EGC_TB_CBS_P3	**Mantissa part of port 3 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001400 MMSCR0_Q0P4 Max-Min Scheduler Control Register 0 of Queue 0/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P4				MIN_RATE_CTRL_EXP_Q0_P4					MIN_RATE_CTRL_MAN_Q0_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P4	**Port 4 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P4	**Port 4 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let

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		the pkt pass.(infinite rate) 1: Queue 0 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q0_P4	**Exponent part of Port 4 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P4	**Mantissa part of Port 4 Queue 0 min. shaper rate limit control** Value range: 1..100

00001404 MMSCR1_Q0P4 Max-Min Scheduler Control Register 1 of Queue 0/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P4				MAX_WEIGHT_Q0_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P4				MAX_RATE_CTRL_EXP_Q0_P4					MAX_RATE_CTRL_MAN_Q0_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P4	**Port 4 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P4	**Port 4 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P4	**Port 4 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q0_P4	**Exponent part of Port 4 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P4	**Mantissa part of Port 4 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001408 MMSCR0_Q1P4 Max-Min Scheduler Control Register 0 of Queue 1/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P4				MIN_RATE_CTRL_EXP_Q1_P4					MIN_RATE_CTRL_MAN_Q1_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P4	**Port 4 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P4	**Port 4 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P4	**Exponent part of Port 4 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P4	**Mantissa part of Port 4 Queue 1 min. shaper rate limit control** Value range: 1..127

0000140C MMSCR1_Q1P4 Max-Min Scheduler Control Register 1 of Queue 1/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P4				MAX_WEIGHT_Q1_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P4				MAX_RATE_CTRL_EXP_Q1_P4					MAX_RATE_CTRL_MAN_Q1_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P4	**Port 4 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P4	**Port 4 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P4	**Port 4 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P4	**Exponent part of Port 4 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P4	**Mantissa part of Port 4 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001410 MMSCR0_Q2P4 Max-Min Scheduler Control Register 0 of Queue 2/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P4															

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Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P4				MIN_RATE_CTRL_EXP_Q2_P4					MIN_RATE_CTRL_MAN_Q2_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P4	**Port 4 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P4	**Port 4 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 2 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P4	**Exponent part of Port 4 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P4	**Mantissa part of Port 4 Queue 2 min. shaper rate limit control** Value range: 1..127

00001414 MMSCR1_Q2P4 Max-Min Scheduler Control Register 1 of Queue 2/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P4				MAX_WEIGHT_Q2_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P4				MAX_RATE_CTRL_EXP_Q2_P4					MAX_RATE_CTRL_MAN_Q2_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P4	**Port 4 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P4	**Port 4 Queue 2 weighted value for maximum WFQ weighted value is (q2_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P4	**Port 4 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P4	**Exponent part of Port 4 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P4	**Mantissa part of Port 4 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001418 MMSCR0_Q3P4 Max-Min Scheduler Control Register 0 of Queue 3/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P4				MIN_RATE_CTRL_EXP_Q3_P4					MIN_RATE_CTRL_MAN_Q3_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P4	**Port 4 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P4	**Port 4 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P4	**Exponent part of Port 4 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P4	**Mantissa part of Port 4 Queue 3 min. shaper rate limit control** Value range: 1..127

0000141C MMSCR1_Q3P4 Max-Min Scheduler Control Register 1 of Queue 3/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P4				MAX_WEIGHT_Q3_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P4				MAX_RATE_CTRL_EXP_Q3_P4					MAX_RATE_CTRL_MAN_Q3_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P4	**Port 4 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P4	**Port 4 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P4	**Port 4 Queue 3 maximum shaper rate limit control is enabled.**

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		0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P4	**Exponent part of Port 4 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P4	**Mantissa part of Port 4 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001420 MMSCR0_Q4P4 Max-Min Scheduler Control Register 0 of Queue 4/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P4				MIN_RATE_CTRL_EXP_Q4_P4					MIN_RATE_CTRL_MAN_Q4_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P4	**Port 4 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P4	**Port 4 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P4	**Exponent part of Port 4 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P4	**Mantissa part of Port 4 Queue 4 min. shaper rate limit control** Value range: 1..127

00001424 MMSCR1_Q4P4 Max-Min Scheduler Control Register 1 of Queue 4/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P4				MAX_WEIGHT_Q4_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P4				MAX_RATE_CTRL_EXP_Q4_P4					MAX_RATE_CTRL_MAN_Q4_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P4	**Port 4 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P4	**Port 4 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P4	**Port 4 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P4	**Exponent part of Port 4 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P4	**Mantissa part of Port 4 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001428 MMSCR0_Q5P4 Max-Min Scheduler Control Register 0 of Queue 5/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P4				MIN_RATE_CTRL_EXP_Q5_P4					MIN_RATE_CTRL_MAN_Q5_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P4	**Port 4 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P4	**Port 4 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P4	**Exponent part of Port 4 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P4	**Mantissa part of Port 4 Queue 5 min. shaper rate limit control** Value range: 1..127

0000142C MMSCR1_Q5P4 Max-Min Scheduler Control Register 1 of Queue 5/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P4				MAX_WEIGHT_Q5_P4											
Type	RW				RW											

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Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P4				MAX_RATE_CTRL_EXP_Q5_P4					MAX_RATE_CTRL_MAN_Q5_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P4	**Port 4 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P4	**Port 4 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P4	**Port 4 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P4	**Exponent part of Port 4 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P4	**Mantissa part of Port 4 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001430 MMSCR0_Q6P4 Max-Min Scheduler Control Register 0 of Queue 6/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P4				MIN_RATE_CTRL_EXP_Q6_P4					MIN_RATE_CTRL_MAN_Q6_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P4	**Port 4 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P4	**Port 4 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P4	**Exponent part of Port 4 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P4	**Mantissa part of Port 4 Queue 6 min. shaper rate limit control** Value range: 1..127

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00001434 MMSCR1_Q6P4 Max-Min Scheduler Control Register 1 of Queue 6/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P4				MAX_WEIGHT_Q6_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P4				MAX_RATE_CTRL_EXP_Q6_P4					MAX_RATE_CTRL_MAN_Q6_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P4	**Port 4 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P4	**Port 4 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P4	**Port 4 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P4	**Exponent part of Port 4 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P4	**Mantissa part of Port 4 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001438 MMSCR0_Q7P4 Max-Min Scheduler Control Register 0 of Queue 7/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P4				MIN_RATE_CTRL_EXP_Q7_P4					MIN_RATE_CTRL_MAN_Q7_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P4	**Port 4 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P4	**Port 4 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P4	**Exponent part of Port 4 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P4	**Mantissa part of Port 4 Queue 7 min. shaper rate limit control** Value range: 1..127

0000143C MMSCR1_Q7P4 Max-Min Scheduler Control Register 1 of Queue 7/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P4				MAX_WEIGHT_Q7_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P4				MAX_RATE_CTRL_EXP_Q7_P4					MAX_RATE_CTRL_MAN_Q7_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P4	**Port 4 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P4	**Port 4 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P4	**Port 4 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P4	**Exponent part of Port 4 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P4	**Mantissa part of Port 4 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001440 ERLCR_P4 Egress Rate Limit Control Register of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P4			EGC_RATE_CIR_16_P4	EG_RATE_LIMIT_EXP_P4_EGC_TB_T_P4				EGC_TB_EN_P4	EG_RATE_LIMIT_MAN_P4_EGC_TB_CBS_P4						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:16	EGC_RATE_CIR_15_0_P4	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P4	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P4	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P4_EGC_TB_T_P4	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P4	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P4_EGC_TB_CBS_P4	**Mantissa part of port 4 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001500 MMSCR0_Q0P5 Max-Min Scheduler Control Register 0 of Queue 0/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P5				MIN_RATE_CTRL_EXP_Q0_P5					MIN_RATE_CTRL_MAN_Q0_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P5	**Port 5 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P5	**Port 5 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let

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		the pkt pass.(infinite rate) 1: Queue 0 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q0_P5	**Exponent part of Port 5 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P5	**Mantissa part of Port 5 Queue 0 min. shaper rate limit control** Value range: 1..100

00001504 MMSCR1_Q0P5 Max-Min Scheduler Control Register 1 of Queue 0/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P5				MAX_WEIGHT_Q0_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P5				MAX_RATE_CTRL_EXP_Q0_P5					MAX_RATE_CTRL_MAN_Q0_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P5	**Port 5 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P5	**Port 5 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P5	**Port 5 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q0_P5	**Exponent part of Port 5 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P5	**Mantissa part of Port 5 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001508 MMSCR0_Q1P5 Max-Min Scheduler Control Register 0 of Queue 1/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P5				MIN_RATE_CTRL_EXP_Q1_P5					MIN_RATE_CTRL_MAN_Q1_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P5	**Port 5 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P5	**Port 5 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P5	**Exponent part of Port 5 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P5	**Mantissa part of Port 5 Queue 1 min. shaper rate limit control** Value range: 1..127

0000150C MMSCR1_Q1P5 Max-Min Scheduler Control Register 1 of Queue 1/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P5				MAX_WEIGHT_Q1_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P5				MAX_RATE_CTRL_EXP_Q1_P5					MAX_RATE_CTRL_MAN_Q1_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P5	**Port 5 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P5	**Port 5 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P5	**Port 5 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P5	**Exponent part of Port 5 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P5	**Mantissa part of Port 5 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001510 MMSCR0_Q2P5 Max-Min Scheduler Control Register 0 of Queue 2/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P5															

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Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P5				MIN_RATE_CTRL_EXP_Q2_P5					MIN_RATE_CTRL_MAN_Q2_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P5	**Port 5 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P5	**Port 5 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 2 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P5	**Exponent part of Port 5 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P5	**Mantissa part of Port 5 Queue 2 min. shaper rate limit control** Value range: 1..127

00001514 MMSCR1_Q2P5 Max-Min Scheduler Control Register 1 of Queue 2/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P5				MAX_WEIGHT_Q2_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P5				MAX_RATE_CTRL_EXP_Q2_P5					MAX_RATE_CTRL_MAN_Q2_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P5	**Port 5 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P5	**Port 5 Queue 2 weighted value for maximum WFQ weighted value is (q2_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P5	**Port 5 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P5	**Exponent part of Port 5 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P5	**Mantissa part of Port 5 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001518 MMSCR0_Q3P5 Max-Min Scheduler Control Register 0 of Queue 3/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P5				MIN_RATE_CTRL_EXP_Q3_P5					MIN_RATE_CTRL_MAN_Q3_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P5	**Port 5 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P5	**Port 5 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P5	**Exponent part of Port 5 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P5	**Mantissa part of Port 5 Queue 3 min. shaper rate limit control** Value range: 1..127

0000151C MMSCR1_Q3P5 Max-Min Scheduler Control Register 1 of Queue 3/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P5				MAX_WEIGHT_Q3_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P5				MAX_RATE_CTRL_EXP_Q3_P5					MAX_RATE_CTRL_MAN_Q3_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P5	**Port 5 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P5	**Port 5 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P5	**Port 5 Queue 3 maximum shaper rate limit control is enabled.**

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		0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P5	**Exponent part of Port 5 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P5	**Mantissa part of Port 5 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001520 MMSCR0_Q4P5 Max-Min Scheduler Control Register 0 of Queue 4/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P5				MIN_RATE_CTRL_EXP_Q4_P5					MIN_RATE_CTRL_MAN_Q4_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P5	**Port 5 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P5	**Port 5 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P5	**Exponent part of Port 5 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P5	**Mantissa part of Port 5 Queue 4 min. shaper rate limit control** Value range: 1..127

00001524 MMSCR1_Q4P5 Max-Min Scheduler Control Register 1 of Queue 4/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P5				MAX_WEIGHT_Q4_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P5				MAX_RATE_CTRL_EXP_Q4_P5					MAX_RATE_CTRL_MAN_Q4_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P5	**Port 5 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P5	**Port 5 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P5	**Port 5 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P5	**Exponent part of Port 5 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P5	**Mantissa part of Port 5 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001528 MMSCR0_Q5P5 Max-Min Scheduler Control Register 0 of Queue 5/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P5				MIN_RATE_CTRL_EXP_Q5_P5					MIN_RATE_CTRL_MAN_Q5_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P5	**Port 5 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P5	**Port 5 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P5	**Exponent part of Port 5 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P5	**Mantissa part of Port 5 Queue 5 min. shaper rate limit control** Value range: 1..127

0000152C MMSCR1_Q5P5 Max-Min Scheduler Control Register 1 of Queue 5/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P5				MAX_WEIGHT_Q5_P5											
Type	RW				RW											

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Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P5				MAX_RATE_CTRL_EXP_Q5_P5					MAX_RATE_CTRL_MAN_Q5_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P5	**Port 5 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P5	**Port 5 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P5	**Port 5 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P5	**Exponent part of Port 5 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P5	**Mantissa part of Port 5 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001530 MMSCR0_Q6P5 Max-Min Scheduler Control Register 0 of Queue 6/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P5				MIN_RATE_CTRL_EXP_Q6_P5					MIN_RATE_CTRL_MAN_Q6_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P5	**Port 5 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P5	**Port 5 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P5	**Exponent part of Port 5 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P5	**Mantissa part of Port 5 Queue 6 min. shaper rate limit control** Value range: 1..127

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00001534 MMSCR1_Q6P5 Max-Min Scheduler Control Register 1 of Queue 6/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P5				MAX_WEIGHT_Q6_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P5				MAX_RATE_CTRL_EXP_Q6_P5					MAX_RATE_CTRL_MAN_Q6_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P5	**Port 5 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P5	**Port 5 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P5	**Port 5 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P5	**Exponent part of Port 5 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P5	**Mantissa part of Port 5 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001538 MMSCR0_Q7P5 Max-Min Scheduler Control Register 0 of Queue 7/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P5				MIN_RATE_CTRL_EXP_Q7_P5					MIN_RATE_CTRL_MAN_Q7_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P5	**Port 5 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P5	**Port 5 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P5	**Exponent part of Port 5 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P5	**Mantissa part of Port 5 Queue 7 min. shaper rate limit control** Value range: 1..127

0000153C MMSCR1_Q7P5 Max-Min Scheduler Control Register 1 of Queue 7/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P5				MAX_WEIGHT_Q7_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P5				MAX_RATE_CTRL_EXP_Q7_P5					MAX_RATE_CTRL_MAN_Q7_P5						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P5	**Port 5 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P5	**Port 5 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P5	**Port 5 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P5	**Exponent part of Port 5 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P5	**Mantissa part of Port 5 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001540 ERLCR_P5 Egress Rate Limit Control Register of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P5			EGC_RATE_CIR_16_P5	EG_RATE_LIMIT_EXP_P5_EGC_TB_T_P5				EGC_TB_EN_P5	EG_RATE_LIMIT_MAN_P5_EGC_TB_CBS_P5						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:16	EGC_RATE_CIR_15_0_P5	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P5	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P5	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P5_EGC_TB_T_P5	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P5	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P5_EGC_TB_CBS_P5	**Mantissa part of port 5 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001600 MMSCR0_Q0P6 Max-Min Scheduler Control Register 0 of Queue 0/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P6				MIN_RATE_CTRL_EXP_Q0_P6					MIN_RATE_CTRL_MAN_Q0_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P6	**Port 6 Queue 0 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q0_P6	**Port 6 Queue 0 minimum shaper rate limit control is enabled.** 0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let

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		the pkt pass.(infinite rate) 1: Queue 0 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q0_P6	**Exponent part of Port 6 Queue 0 min. shaper rate limit control** Value range: 0..4
6:0	MIN_RATE_CTRL_MAN_Q0_P6	**Mantissa part of Port 6 Queue 0 min. shaper rate limit control** Value range: 1..100

00001604 MMSCR1_Q0P6 Max-Min Scheduler Control Register 1 of Queue 0/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P6				MAX_WEIGHT_Q0_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P6				MAX_RATE_CTRL_EXP_Q0_P6					MAX_RATE_CTRL_MAN_Q0_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P6	**Port 6 Queue 0 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P6	**Port 6 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)**
15	MAX_RATE_EN_Q0_P6	**Port 6 Queue 0 maximum shaper rate limit control is enabled.** 0: Queue 0 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 0 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q0_P6	**Exponent part of Port 6 Queue 0 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q0_P6	**Mantissa part of Port 6 Queue 0 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001608 MMSCR0_Q1P6 Max-Min Scheduler Control Register 0 of Queue 1/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P6				MIN_RATE_CTRL_EXP_Q1_P6					MIN_RATE_CTRL_MAN_Q1_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P6	**Port 6 Queue 1 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q1_P6	**Port 6 Queue 1 minimum shaper rate limit control is enabled.** 0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q1_P6	**Exponent part of Port 6 Queue 1 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q1_P6	**Mantissa part of Port 6 Queue 1 min. shaper rate limit control** Value range: 1..127

0000160C MMSCR1_Q1P6 Max-Min Scheduler Control Register 1 of Queue 1/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P6				MAX_WEIGHT_Q1_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P6				MAX_RATE_CTRL_EXP_Q1_P6					MAX_RATE_CTRL_MAN_Q1_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P6	**Port 6 Queue 1 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P6	**Port 6 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)**
15	MAX_RATE_EN_Q1_P6	**Port 6 Queue 1 maximum shaper rate limit control is enabled.** 0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 1 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q1_P6	**Exponent part of Port 6 Queue 1 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q1_P6	**Mantissa part of Port 6 Queue 1 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001610 MMSCR0_Q2P6 Max-Min Scheduler Control Register 0 of Queue 2/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P6															

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Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P6				MIN_RATE_CTRL_EXP_Q2_P6					MIN_RATE_CTRL_MAN_Q2_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P6	**Port 6 Queue 2 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q2_P6	**Port 6 Queue 2 minimum shaper rate limit control is enabled.** 0: Queue 2 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q2_P6	**Exponent part of Port 6 Queue 2 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q2_P6	**Mantissa part of Port 6 Queue 2 min. shaper rate limit control** Value range: 1..127

00001614 MMSCR1_Q2P6 Max-Min Scheduler Control Register 1 of Queue 2/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P6				MAX_WEIGHT_Q2_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P6				MAX_RATE_CTRL_EXP_Q2_P6					MAX_RATE_CTRL_MAN_Q2_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P6	**Port 6 Queue 2 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P6	**Port 6 Queue 2 weighted value for maximum WFQ weighted value is (q2_max_weight+1'b1)**
15	MAX_RATE_EN_Q2_P6	**Port 6 Queue 2 maximum shaper rate limit control is enabled.** 0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 2 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q2_P6	**Exponent part of Port 6 Queue 2 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q2_P6	**Mantissa part of Port 6 Queue 2 maximum shaper rate limit control** Value range: 0..127 (7-bit)

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00001618 MMSCR0_Q3P6 Max-Min Scheduler Control Register 0 of Queue 3/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P6				MIN_RATE_CTRL_EXP_Q3_P6					MIN_RATE_CTRL_MAN_Q3_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P6	**Port 6 Queue 3 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q3_P6	**Port 6 Queue 3 minimum shaper rate limit control is enabled.** 0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q3_P6	**Exponent part of Port 6 Queue 3 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q3_P6	**Mantissa part of Port 6 Queue 3 min. shaper rate limit control** Value range: 1..127

0000161C MMSCR1_Q3P6 Max-Min Scheduler Control Register 1 of Queue 3/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P6				MAX_WEIGHT_Q3_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P6				MAX_RATE_CTRL_EXP_Q3_P6					MAX_RATE_CTRL_MAN_Q3_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P6	**Port 6 Queue 3 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P6	**Port 6 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)**
15	MAX_RATE_EN_Q3_P6	**Port 6 Queue 3 maximum shaper rate limit control is enabled.**

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		0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 3 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q3_P6	**Exponent part of Port 6 Queue 3 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q3_P6	**Mantissa part of Port 6 Queue 3 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001620 MMSCR0_Q4P6 Max-Min Scheduler Control Register 0 of Queue 4/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P6				MIN_RATE_CTRL_EXP_Q4_P6					MIN_RATE_CTRL_MAN_Q4_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P6	**Port 6 Queue 4 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q4_P6	**Port 6 Queue 4 minimum shaper rate limit control is enabled.** 0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q4_P6	**Exponent part of Port 6 Queue 4 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q4_P6	**Mantissa part of Port 6 Queue 4 min. shaper rate limit control** Value range: 1..127

00001624 MMSCR1_Q4P6 Max-Min Scheduler Control Register 1 of Queue 4/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P6				MAX_WEIGHT_Q4_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P6				MAX_RATE_CTRL_EXP_Q4_P6					MAX_RATE_CTRL_MAN_Q4_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P6	**Port 6 Queue 4 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P6	**Port 6 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)**
15	MAX_RATE_EN_Q4_P6	**Port 6 Queue 4 maximum shaper rate limit control is enabled.** 0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 4 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q4_P6	**Exponent part of Port 6 Queue 4 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q4_P6	**Mantissa part of Port 6 Queue 4 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001628 MMSCR0_Q5P6 Max-Min Scheduler Control Register 0 of Queue 5/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P6				MIN_RATE_CTRL_EXP_Q5_P6					MIN_RATE_CTRL_MAN_Q5_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P6	**Port 6 Queue 5 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q5_P6	**Port 6 Queue 5 minimum shaper rate limit control is enabled.** 0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q5_P6	**Exponent part of Port 6 Queue 5 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q5_P6	**Mantissa part of Port 6 Queue 5 min. shaper rate limit control** Value range: 1..127

0000162C MMSCR1_Q5P6 Max-Min Scheduler Control Register 1 of Queue 5/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P6				MAX_WEIGHT_Q5_P6											
Type	RW				RW											

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Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P6				MAX_RATE_CTRL_EXP_Q5_P6					MAX_RATE_CTRL_MAN_Q5_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P6	**Port 6 Queue 5 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P6	**Port 6 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)**
15	MAX_RATE_EN_Q5_P6	**Port 6 Queue 5 maximum shaper rate limit control is enabled.** 0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 5 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q5_P6	**Exponent part of Port 6 Queue 5 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q5_P6	**Mantissa part of Port 6 Queue 5 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001630 MMSCR0_Q6P6 Max-Min Scheduler Control Register 0 of Queue 6/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P6				MIN_RATE_CTRL_EXP_Q6_P6					MIN_RATE_CTRL_MAN_Q6_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P6	**Port 6 Queue 6 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q6_P6	**Port 6 Queue 6 minimum shaper rate limit control is enabled.** 0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q6_P6	**Exponent part of Port 6 Queue 6 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q6_P6	**Mantissa part of Port 6 Queue 6 min. shaper rate limit control** Value range: 1..127

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00001634 MMSCR1_Q6P6 Max-Min Scheduler Control Register 1 of Queue 6/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P6				MAX_WEIGHT_Q6_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P6				MAX_RATE_CTRL_EXP_Q6_P6					MAX_RATE_CTRL_MAN_Q6_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P6	**Port 6 Queue 6 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P6	**Port 6 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)**
15	MAX_RATE_EN_Q6_P6	**Port 6 Queue 6 maximum shaper rate limit control is enabled.** 0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 6 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q6_P6	**Exponent part of Port 6 Queue 6 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q6_P6	**Mantissa part of Port 6 Queue 6 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001638 MMSCR0_Q7P6 Max-Min Scheduler Control Register 0 of Queue 7/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P6				MIN_RATE_CTRL_EXP_Q7_P6					MIN_RATE_CTRL_MAN_Q7_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P6	**Port 6 Queue 7 min. traffic arbitration scheme** 0: Strict Priority (SP) 1: Round-Robin (RR)
15	MIN_RATE_EN_Q7_P6	**Port 6 Queue 7 minimum shaper rate limit control is enabled.** 0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)

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		1: Queue 7 min. rate limit control enable
11:8	MIN_RATE_CTRL_EXP_Q7_P6	**Exponent part of Port 6 Queue 7 min. shaper rate limit control** Value range: 0..13
6:0	MIN_RATE_CTRL_MAN_Q7_P6	**Mantissa part of Port 6 Queue 7 min. shaper rate limit control** Value range: 1..127

0000163C MMSCR1_Q7P6 Max-Min Scheduler Control Register 1 of Queue 7/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P6				MAX_WEIGHT_Q7_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P6				MAX_RATE_CTRL_EXP_Q7_P6					MAX_RATE_CTRL_MAN_Q7_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P6	**Port 6 Queue 7 maximum traffic arbitration scheme** 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P6	**Port 6 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)**
15	MAX_RATE_EN_Q7_P6	**Port 6 Queue 7 maximum shaper rate limit control is enabled.** 0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) 1: Queue 7 maximum rate limit enable
11:8	MAX_RATE_CTRL_EXP_Q7_P6	**Exponent part of Port 6 Queue 7 maximum shaper rate limit control** Value range: 0..13 (4-bit)
6:0	MAX_RATE_CTRL_MAN_Q7_P6	**Mantissa part of Port 6 Queue 7 maximum shaper rate limit control** Value range: 0..127 (7-bit)

00001640 ERLCR_P6 Egress Rate Limit Control Register of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P6			EGC_RATE_CIR_16_P6	EG_RATE_LIMIT_EXP_P6_EGC_TB_T_P6				EGC_TB_EN_P6	EG_RATE_LIMIT_MAN_P6_EGC_TB_CBS_P6						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:16	EGC_RATE_CIR_15_0_P6	**Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	EG_RATE_LIMIT_EN_P6	**EXP: egress_rate_limit_exp** MAN: egress_rate_limit_man Egress port rate limitation: MAN*10^(EXP)*1Kbps 0: Egress rate limit control disable 1: Enable
12	EGC_RATE_CIR_16_P6	**Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	EG_RATE_LIMIT_EXP_P6_EGC_TB_T_P6	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	EGC_TB_EN_P6	**When this bit is disabled, the Egress rate control acts like a leaky bucket principle.** Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	EG_RATE_LIMIT_MAN_P6_EGC_TB_CBS_P6	**Mantissa part of port 6 Egress rate limit control Value range: 0..127 (7-bit),** when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001800 IRLCR_P0 Ingress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P0			IGC_RATE_CIR_16_P0	IGC_RATE_EXP_P0_IGC_TB_T_P0				IGC_TB_EN_P0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P0	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P0	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P0	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**

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11:8	IGC_RATE_EXP_P0_IGC_TB_T_P0	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P0	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0	**Mantissa part of port 0 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001804 FPC_RXCTRL_P0 Free Page Count at RX_CTRL of Port 0 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P0		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P0	**It indicates the free page count at RX_CTRL module.**

0000180C MMDPR_10_Q0_P0 Drop Precedence control 10 of Q0 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P0_DP_en					P0Q0_pr_dp10						P0Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp10[3:0]							P0Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31	P0_DP_en	**Enable Drop Precedence function of P0. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P0Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P0Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P0Q0_lt_dp10 <= queue depth < P0Q0_ht_dp10, the drop probability of incoming packet is based on the setting P0Q0_pr_dp10. 0: Disable 1: Enable
26:24	P0Q0_pr_dp10	**Drop probability of P0 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q0_ht_dp10	**High threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q0_lt_dp10	**Low threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001810 MMDPR_10_Q1 P0 Drop Precedence control 10 of Q1 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q1_pr_dp10						P0Q1_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q1_ht_dp10[3:0]							P0Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q1_pr_dp10	**Drop probability of P0 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q1_ht_dp10	**High threshold of P0 Q1 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q1_lt_dp10	**Low threshold of P0 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001814 MMDPR_10_Q2 P0 Drop Precedence control 10 of Q2 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q2_pr_dp10						P0Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q2_ht_dp10[3:0]							P0Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q2_pr_dp10	**Drop probability of P0 Q2 for drop precedence = 2'b10.** 0x0: 0%

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		0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q2_ht_dp10	**High threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q2_lt_dp10	**Low threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size**

00001818 MMDPR_10_Q3 P0 Drop Precedence control 10 of Q3 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q3_pr_dp10						P0Q3_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q3_ht_dp10[3:0]							P0Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q3_pr_dp10	**Drop probability of P0 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q3_ht_dp10	**High threshold of P0 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q3_lt_dp10	**Low threshold of P0 Q3 depth for drop precedence = 2'b10. Unit: page size**

0000181C MMDPR_10_Q4 P0 Drop Precedence control 10 of Q4 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q4_pr_dp10						P0Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q4_ht_dp10[3:0]							P0Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q4_pr_dp10	**Drop probability of P0 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q4_ht_dp10	**High threshold of P0 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q4_lt_dp10	**Low threshold of P0 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001820 MMDPR_10_Q5 Drop Precedence control 10 of Q5 Port 0 00000000

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P0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q5_pr_dp10						P0Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q5_ht_dp10[3:0]							P0Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q5_pr_dp10	**Drop probability of P0 Q5 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q5_ht_dp10	**High threshold of P0 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q5_lt_dp10	**Low threshold of P0 Q5 depth for drop precedence = 2'b10. Unit: page size**

00001824 MMDPR_10_Q6 P0 Drop Precedence control 10 of Q6 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q6_pr_dp10						P0Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q6_ht_dp10[3:0]							P0Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q6_pr_dp10	**Drop probability of P0 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q6_ht_dp10	**High threshold of P0 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q6_lt_dp10	**Low threshold of P0 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001828 MMDPR_10_Q7 P0 Drop Precedence control 10 of Q7 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q7_pr_dp10						P0Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q7_ht_dp10[3:0]							P0Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:24	P0Q7_pr_dp10	**Drop probability of P0 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q7_ht_dp10	**High threshold of P0 Q7 depth for drop precedence = 2'b10. Unit: page size**
8:0	P0Q7_lt_dp10	**Low threshold of P0 Q7 depth for drop precedence = 2'b10. Unit: page size**

0000182C MMDPR_11_Q0P0 Drop Precedence control 11 of Q0 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q0_pr_dp11						P0Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp11[3:0]							P0Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q0_pr_dp11	**Drop probability of P0 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q0_ht_dp11	**High threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q0_lt_dp11	**Low threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size**

00001830 MMDPR_11_Q1P0 Drop Precedence control 11 of Q1 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q1_pr_dp11						P0Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q1_ht_dp11[3:0]							P0Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q1_pr_dp11	**Drop probability of P0 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q1_ht_dp11	**High threshold of P0 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q1_lt_dp11	**Low threshold of P0 Q1 depth for drop precedence = 2'b11. Unit: page size**

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00001834 MMDPR_11_Q2 P0 Drop Precedence control 11 of Q2 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q2_pr_dp11						P0Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q2_ht_dp11[3:0]							P0Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q2_pr_dp11	**Drop probability of P0 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q2_ht_dp11	**High threshold of P0 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q2_lt_dp11	**Low threshold of P0 Q2 depth for drop precedence = 2'b11. Unit: page size**

00001838 MMDPR_11_Q3 P0 Drop Precedence control 11 of Q3 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q3_pr_dp11						P0Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q3_ht_dp11[3:0]							P0Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q3_pr_dp11	**Drop probability of P0 Q3 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q3_ht_dp11	**High threshold of P0 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q3_lt_dp11	**Low threshold of P0 Q3 depth for drop precedence = 2'b11. Unit: page size**

0000183C MMDPR_11_Q4 P0 Drop Precedence control 11 of Q4 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q4_pr_dp11						P0Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q4_ht_dp11[3:0]							P0Q4_lt_dp11								
Type	RW							RW								

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Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q4_pr_dp11	**Drop probability of P0 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q4_ht_dp11	**High threshold of P0 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q4_lt_dp11	**Low threshold of P0 Q4 depth for drop precedence = 2'b11. Unit: page size**

00001840 MMDPR_11_Q5 P0 Drop Precedence control 11 of Q5 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q5_pr_dp11						P0Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q5_ht_dp11[3:0]							P0Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q5_pr_dp11	**Drop probability of P0 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q5_ht_dp11	**High threshold of P0 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q5_lt_dp11	**Low threshold of P0 Q5 depth for drop precedence = 2'b11. Unit: page size**

00001844 MMDPR_11_Q6 P0 Drop Precedence control 11 of Q6 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q6_pr_dp11						P0Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q6_ht_dp11[3:0]							P0Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q6_pr_dp11	**Drop probability of P0 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q6_ht_dp11	**High threshold of P0 Q6 depth for drop precedence = 2'b11. Unit: page size**

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8:0	P0Q6_lt_dp11	**Low threshold of P0 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001848 MMDPR_11_Q7 P0 Drop Precedence control 11 of Q7 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q7_pr_dp11						P0Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q7_ht_dp11[3:0]							P0Q7_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q7_pr_dp11	**Drop probability of P0 Q7 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P0Q7_ht_dp11	**High threshold of P0 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P0Q7_lt_dp11	**Low threshold of P0 Q7 depth for drop precedence = 2'b11. Unit: page size**

00001900 IRLCR_P1 Ingress Rate Limit Control Register of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P1			IGC_RATE_CIR_16_P1	IGC_RATE_EXP_P1_IGC_TB_T_P1				IGC_TB_EN_P1	IGC_RATE_MAN_P1_IGC_TB_CBS_P1						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P1	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P1	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control Disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P1	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P1_IGC_TB_T_P1	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms

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		6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P1	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P1_IGC_TB_CBS_P1	**Mantissa part of port 1 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001904 FPC_RXCTRL_P1 Free Page Count at RX_CTRL of Port 1 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P1		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P1	**It indicates the free page count at RX_CTRL module.**

0000190C MMDPR_10_Q0_P1 Drop Precedence control 10 of Q0 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_DP_en					P1Q0_pr_dp10						P1Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q0_ht_dp10[3:0]							P1Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P1_DP_en	**Enable Drop Precedence function of P1. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P1Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P1Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P1Q0_lt_dp10 <= queue depth < P1Q0_ht_dp10, the drop probability of incoming packet is based on the setting P1Q0_pr_dp10. 0: Disable

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		1: Enable
26:24	P1Q0_pr_dp10	**Drop probability of P1 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q0_ht_dp10	**High threshold of P1 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q0_lt_dp10	**Low threshold of P1 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001910 MMDPR_10_Q1 P1 Drop Precedence control 10 of Q1 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q1_pr_dp10						P1Q1_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q1_ht_dp10[3:0]							P1Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q1_pr_dp10	**Drop probability of P1 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q1_ht_dp10	**High threshold of P1 Q1 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q1_lt_dp10	**Low threshold of P1 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001914 MMDPR_10_Q2 P1 Drop Precedence control 10 of Q2 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q2_pr_dp10						P1Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q2_ht_dp10[3:0]							P1Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q2_pr_dp10	**Drop probability of P1 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q2_ht_dp10	**High threshold of P1 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q2_lt_dp10	**Low threshold of P1 Q2 depth for drop precedence = 2'b10. Unit: page size**

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00001918 MMDPR_10_Q3 P1 Drop Precedence control 10 of Q3 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q3_pr_dp10						P1Q3_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q3_ht_dp10[3:0]							P1Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q3_pr_dp10	**Drop probability of P1 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q3_ht_dp10	**High threshold of P1 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q3_lt_dp10	**Low threshold of P1 Q3 depth for drop precedence = 2'b10. Unit: page size**

0000191C MMDPR_10_Q4 P1 Drop Precedence control 10 of Q4 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q4_pr_dp10						P1Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q4_ht_dp10[3:0]							P1Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q4_pr_dp10	**Drop probability of P1 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q4_ht_dp10	**High threshold of P1 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q4_lt_dp10	**Low threshold of P1 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001920 MMDPR_10_Q5 P1 Drop Precedence control 10 of Q5 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q5_pr_dp10						P1Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q5_ht_dp10[3:0]							P1Q5_lt_dp10								
Type	RW							RW								

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Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q5_pr_dp10	**Drop probability of P1 Q5 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q5_ht_dp10	**High threshold of P1 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q5_lt_dp10	**Low threshold of P1 Q5 depth for drop precedence = 2'b10. Unit: page size**

00001924 MMDPR_10_Q6 P1 Drop Precedence control 10 of Q6 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q6_pr_dp10						P1Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q6_ht_dp10[3:0]							P1Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q6_pr_dp10	**Drop probability of P1 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q6_ht_dp10	**High threshold of P1 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P1Q6_lt_dp10	**Low threshold of P1 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001928 MMDPR_10_Q7 P1 Drop Precedence control 10 of Q7 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q7_pr_dp10						P1Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q7_ht_dp10[3:0]							P1Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q7_pr_dp10	**Drop probability of P1 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q7_ht_dp10	**High threshold of P1 Q7 depth for drop precedence = 2'b10. Unit: page size**

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8:0	P1Q7_lt_dp10	**Low threshold of P1 Q7 depth for drop precedence = 2'b10. Unit: page size**

0000192C MMDPR_11_Q0 P1 Drop Precedence control 11 of Q0 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q0_pr_dp11						P1Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q0_ht_dp11[3:0]							P1Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q0_pr_dp11	**Drop probability of P1 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q0_ht_dp11	**High threshold of P1 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q0_lt_dp11	**Low threshold of P1 Q0 depth for drop precedence = 2'b11. Unit: page size**

00001930 MMDPR_11_Q1 P1 Drop Precedence control 11 of Q1 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q1_pr_dp11						P1Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q1_ht_dp11[3:0]							P1Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q1_pr_dp11	**Drop probability of P1 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q1_ht_dp11	**High threshold of P1 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q1_lt_dp11	**Low threshold of P1 Q1 depth for drop precedence = 2'b11. Unit: page size**

00001934 MMDPR_11_Q2 P1 Drop Precedence control 11 of Q2 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q2_pr_dp11						P1Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q2_ht_dp11[3:0]							P1Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q2_pr_dp11	**Drop probability of P1 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q2_ht_dp11	**High threshold of P1 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q2_lt_dp11	**Low threshold of P1 Q2 depth for drop precedence = 2'b11. Unit: page size**

00001938 MMDPR_11_Q3 P1 Drop Precedence control 11 of Q3 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q3_pr_dp11						P1Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q3_ht_dp11[3:0]							P1Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q3_pr_dp11	**Drop probability of P1 Q3 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q3_ht_dp11	**High threshold of P1 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q3_lt_dp11	**Low threshold of P1 Q3 depth for drop precedence = 2'b11. Unit: page size**

0000193C MMDPR_11_Q4 P1 Drop Precedence control 11 of Q4 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q4_pr_dp11						P1Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q4_ht_dp11[3:0]							P1Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q4_pr_dp11	**Drop probability of P1 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%

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		(n=2~6)
20:12	P1Q4_ht_dp11	**High threshold of P1 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q4_lt_dp11	**Low threshold of P1 Q4 depth for drop precedence = 2'b11. Unit: page size**

00001940 MMDPR_11_Q5 P1 Drop Precedence control 11 of Q5 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q5_pr_dp11						P1Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q5_ht_dp11[3:0]							P1Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q5_pr_dp11	**Drop probability of P1 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q5_ht_dp11	**High threshold of P1 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q5_lt_dp11	**Low threshold of P1 Q5 depth for drop precedence = 2'b11. Unit: page size**

00001944 MMDPR_11_Q6 P1 Drop Precedence control 11 of Q6 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q6_pr_dp11						P1Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q6_ht_dp11[3:0]							P1Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q6_pr_dp11	**Drop probability of P1 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q6_ht_dp11	**High threshold of P1 Q6 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q6_lt_dp11	**Low threshold of P1 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001948 MMDPR_11_Q7 P1 Drop Precedence control 11 of Q7 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						P1Q7_pr_dp11						P1Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q7_ht_dp11[3:0]							P1Q7_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q7_pr_dp11	**Drop probability of P1 Q7 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P1Q7_ht_dp11	**High threshold of P1 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P1Q7_lt_dp11	**Low threshold of P1 Q7 depth for drop precedence = 2'b11. Unit: page size**

00001A00 IRLCR_P2 Ingress Rate Limit Control Register of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P2			IGC_RATE_CIR_16_P2	IGC_RATE_EXP_P2_IGC_TB_T_P2				IGC_TB_EN_P2	IGC_RATE_MAN_P2_IGC_TB_CBS_P2						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P2	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P2	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control Disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P2	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P2_IGC_TB_T_P2	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms

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7	IGC_TB_EN_P2	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P2_IGC_TB_CBS_P2	**Mantissa part of port 2 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001A04 FPC_RXCTRL_P2 Free Page Count at RX_CTRL of Port 2 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P2		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P2	**It indicates the free page count at RX_CTRL module.**

00001A0C MMDPR_10_Q0P2 Drop Precedence control 10 of Q0 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_DP_en					P2Q0_pr_dp10						P2Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q0_ht_dp10[3:0]							P2Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P2_DP_en	**Enable Drop Precedence function of P2. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P2Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P2Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P2Q0_lt_dp10 <= queue depth < P2Q0_ht_dp10, the drop probability of incoming packet is based on the setting P2Q0_pr_dp10. 0: Disable 1: Enable
26:24	P2Q0_pr_dp10	**Drop probability of P2 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)

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20:12	P2Q0_ht_dp10	**High threshold of P2 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q0_lt_dp10	**Low threshold of P2 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001A10 MMDPR_10_Q1 P2 Drop Precedence control 10 of Q1 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q1_pr_dp10						P2Q1_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q1_ht_dp10[3:0]							P2Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q1_pr_dp10	**Drop probability of P2 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q1_ht_dp10	**High threshold of P2 Q1 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q1_lt_dp10	**Low threshold of P2 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001A14 MMDPR_10_Q2 P2 Drop Precedence control 10 of Q2 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q2_pr_dp10						P2Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q2_ht_dp10[3:0]							P2Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q2_pr_dp10	**Drop probability of P2 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q2_ht_dp10	**High threshold of P2 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q2_lt_dp10	**Low threshold of P2 Q2 depth for drop precedence = 2'b10. Unit: page size**

00001A18 MMDPR_10_Q3 P2 Drop Precedence control 10 of Q3 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q3_pr_dp10						P2Q3_ht_dp10[8:4]				

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Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q3_ht_dp10[3:0]							P2Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q3_pr_dp10	**Drop probability of P2 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q3_ht_dp10	**High threshold of P2 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q3_lt_dp10	**Low threshold of P2 Q3 depth for drop precedence = 2'b10. Unit: page size**

00001A1C MMDPR_10_Q4 P2 Drop Precedence control 10 of Q4 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q4_pr_dp10						P2Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q4_ht_dp10[3:0]							P2Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q4_pr_dp10	**Drop probability of P2 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q4_ht_dp10	**High threshold of P2 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q4_lt_dp10	**Low threshold of P2 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001A20 MMDPR_10_Q5 P2 Drop Precedence control 10 of Q5 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q5_pr_dp10						P2Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q5_ht_dp10[3:0]							P2Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q5_pr_dp10	**Drop probability of P2 Q5 for drop precedence = 2'b10.** 0x0: 0%

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		0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q5_ht_dp10	**High threshold of P2 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q5_lt_dp10	**Low threshold of P2 Q5 depth for drop precedence = 2'b10. Unit: page size**

00001A24 MMDPR_10_Q6 P2 Drop Precedence control 10 of Q6 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q6_pr_dp10						P2Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q6_ht_dp10[3:0]							P2Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q6_pr_dp10	**Drop probability of P2 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q6_ht_dp10	**High threshold of P2 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q6_lt_dp10	**Low threshold of P2 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001A28 MMDPR_10_Q7 P2 Drop Precedence control 10 of Q7 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q7_pr_dp10						P2Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q7_ht_dp10[3:0]							P2Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q7_pr_dp10	**Drop probability of P2 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q7_ht_dp10	**High threshold of P2 Q7 depth for drop precedence = 2'b10. Unit: page size**
8:0	P2Q7_lt_dp10	**Low threshold of P2 Q7 depth for drop precedence = 2'b10. Unit: page size**

00001A2C MMDPR_11_Q0 Drop Precedence control 11 of Q0 Port 2 00000000

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P2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q0_pr_dp11						P2Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q0_ht_dp11[3:0]							P2Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q0_pr_dp11	**Drop probability of P2 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q0_ht_dp11	**High threshold of P2 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q0_lt_dp11	**Low threshold of P2 Q0 depth for drop precedence = 2'b11. Unit: page size**

00001A30 MMDPR_11_Q1 P2 Drop Precedence control 11 of Q1 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q1_pr_dp11						P2Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q1_ht_dp11[3:0]							P2Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q1_pr_dp11	**Drop probability of P2 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q1_ht_dp11	**High threshold of P2 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q1_lt_dp11	**Low threshold of P2 Q1 depth for drop precedence = 2'b11. Unit: page size**

00001A34 MMDPR_11_Q2 P2 Drop Precedence control 11 of Q2 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q2_pr_dp11						P2Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q2_ht_dp11[3:0]							P2Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:24	P2Q2_pr_dp11	**Drop probability of P2 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q2_ht_dp11	**High threshold of P2 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q2_lt_dp11	**Low threshold of P2 Q2 depth for drop precedence = 2'b11. Unit: page size**

00001A38 MMDPR_11_Q3P2 Drop Precedence control 11 of Q3 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q3_pr_dp11						P2Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q3_ht_dp11[3:0]							P2Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q3_pr_dp11	**Drop probability of P2 Q3 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q3_ht_dp11	**High threshold of P2 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q3_lt_dp11	**Low threshold of P2 Q3 depth for drop precedence = 2'b11. Unit: page size**

00001A3C MMDPR_11_Q4P2 Drop Precedence control 11 of Q4 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q4_pr_dp11						P2Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q4_ht_dp11[3:0]							P2Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q4_pr_dp11	**Drop probability of P2 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q4_ht_dp11	**High threshold of P2 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q4_lt_dp11	**Low threshold of P2 Q4 depth for drop precedence = 2'b11. Unit: page size**

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00001A40 MMDPR_11_Q5P2 Drop Precedence control 11 of Q5 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q5_pr_dp11						P2Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q5_ht_dp11[3:0]							P2Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q5_pr_dp11	**Drop probability of P2 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q5_ht_dp11	**High threshold of P2 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q5_lt_dp11	**Low threshold of P2 Q5 depth for drop precedence = 2'b11. Unit: page size**

00001A44 MMDPR_11_Q6P2 Drop Precedence control 11 of Q6 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q6_pr_dp11						P2Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q6_ht_dp11[3:0]							P2Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q6_pr_dp11	**Drop probability of P2 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q6_ht_dp11	**High threshold of P2 Q6 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q6_lt_dp11	**Low threshold of P2 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001A48 MMDPR_11_Q7P2 Drop Precedence control 11 of Q7 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q7_pr_dp11						P2Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q7_ht_dp11[3:0]							P2Q7_lt_dp11								
Type	RW							RW								

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Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q7_pr_dp11	**Drop probability of P2 Q7 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P2Q7_ht_dp11	**High threshold of P2 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P2Q7_lt_dp11	**Low threshold of P2 Q7 depth for drop precedence = 2'b11. Unit: page size**

00001B00 IRLCR_P3 Ingress Rate Limit Control Register of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P3			IGC_RATE_CIR_16_P3	IGC_RATE_EXP_P3_IGC_TB_T_P3				IGC_TB_EN_P3	IGC_RATE_MAN_P3_IGC_TB_CBS_P3						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P3	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P3	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control Disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P3	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P3_IGC_TB_T_P3	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P3	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable

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		1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P3_IGC_TB_CBS_P3	**Mantissa part of port 3 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001B04 FPC_RXCTRL_P3 Free Page Count at RX_CTRL of Port 3 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P3		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P3	**It indicates the free page count at RX_CTRL module.**

00001B0C MMDPR_10_Q0P3 Drop Precedence control 10 of Q0 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P3_DP_en					P3Q0_pr_dp10						P3Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q0_ht_dp10[3:0]							P3Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P3_DP_en	**Enable Drop Precedence function of P3. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P3Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P3Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P3Q0_lt_dp10 <= queue depth < P3Q0_ht_dp10, the drop probability of incoming packet is based on the setting P3Q0_pr_dp10. 0: Disable 1: Enable
26:24	P3Q0_pr_dp10	**Drop probability of P3 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q0_ht_dp10	**High threshold of P3 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q0_lt_dp10	**Low threshold of P3 Q0 depth for drop precedence = 2'b10. Unit: page size**

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00001B10 MMDPR_10_Q1 P3 Drop Precedence control 10 of Q1 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q1_pr_dp10						P3Q1_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q1_ht_dp10[3:0]							P3Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q1_pr_dp10	**Drop probability of P3 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q1_ht_dp10	**High threshold of P3 Q1 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q1_lt_dp10	**Low threshold of P3 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001B14 MMDPR_10_Q2 P3 Drop Precedence control 10 of Q2 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q2_pr_dp10						P3Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q2_ht_dp10[3:0]							P3Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q2_pr_dp10	**Drop probability of P3 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q2_ht_dp10	**High threshold of P3 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q2_lt_dp10	**Low threshold of P3 Q2 depth for drop precedence = 2'b10. Unit: page size**

00001B18 MMDPR_10_Q3 P3 Drop Precedence control 10 of Q3 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q3_pr_dp10						P3Q3_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q3_ht_dp10[3:0]							P3Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:24	P3Q3_pr_dp10	**Drop probability of P3 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q3_ht_dp10	**High threshold of P3 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q3_lt_dp10	**Low threshold of P3 Q3 depth for drop precedence = 2'b10. Unit: page size**

00001B1C MMDPR_10_Q4 P3 Drop Precedence control 10 of Q4 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q4_pr_dp10						P3Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q4_ht_dp10[3:0]							P3Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q4_pr_dp10	**Drop probability of P3 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q4_ht_dp10	**High threshold of P3 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q4_lt_dp10	**Low threshold of P3 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001B20 MMDPR_10_Q5 P3 Drop Precedence control 10 of Q5 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q5_pr_dp10						P3Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q5_ht_dp10[3:0]							P3Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q5_pr_dp10	**Drop probability of P3 Q5 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q5_ht_dp10	**High threshold of P3 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q5_lt_dp10	**Low threshold of P3 Q5 depth for drop precedence = 2'b10. Unit: page size**

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00001B24 MMDPR_10_Q6 P3 Drop Precedence control 10 of Q6 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q6_pr_dp10						P3Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q6_ht_dp10[3:0]							P3Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q6_pr_dp10	**Drop probability of P3 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q6_ht_dp10	**High threshold of P3 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q6_lt_dp10	**Low threshold of P3 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001B28 MMDPR_10_Q7 P3 Drop Precedence control 10 of Q7 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q7_pr_dp10						P3Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q7_ht_dp10[3:0]							P3Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q7_pr_dp10	**Drop probability of P3 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q7_ht_dp10	**High threshold of P3 Q7 depth for drop precedence = 2'b10. Unit: page size**
8:0	P3Q7_lt_dp10	**Low threshold of P3 Q7 depth for drop precedence = 2'b10. Unit: page size**

00001B2C MMDPR_11_Q0 P3 Drop Precedence control 11 of Q0 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q0_pr_dp11						P3Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	P3Q0_ht_dp11[3:0]							P3Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q0_pr_dp11	**Drop probability of P3 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q0_ht_dp11	**High threshold of P3 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q0_lt_dp11	**Low threshold of P3 Q0 depth for drop precedence = 2'b11. Unit: page size**

00001B30 MMDPR_11_Q1 P3 Drop Precedence control 11 of Q1 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q1_pr_dp11						P3Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q1_ht_dp11[3:0]							P3Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q1_pr_dp11	**Drop probability of P3 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q1_ht_dp11	**High threshold of P3 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q1_lt_dp11	**Low threshold of P3 Q1 depth for drop precedence = 2'b11. Unit: page size**

00001B34 MMDPR_11_Q2 P3 Drop Precedence control 11 of Q2 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q2_pr_dp11						P3Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q2_ht_dp11[3:0]							P3Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q2_pr_dp11	**Drop probability of P3 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%

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		(n=2~6)
20:12	P3Q2_ht_dp11	**High threshold of P3 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q2_lt_dp11	**Low threshold of P3 Q2 depth for drop precedence = 2'b11. Unit: page size**

00001B38 MMDPR_11_Q3 P3 Drop Precedence control 11 of Q3 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q3_pr_dp11						P3Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q3_ht_dp11[3:0]							P3Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q3_pr_dp11	**Drop probability of P3 Q3 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q3_ht_dp11	**High threshold of P3 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q3_lt_dp11	**Low threshold of P3 Q3 depth for drop precedence = 2'b11. Unit: page size**

00001B3C MMDPR_11_Q4 P3 Drop Precedence control 11 of Q4 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q4_pr_dp11						P3Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q4_ht_dp11[3:0]							P3Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q4_pr_dp11	**Drop probability of P3 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q4_ht_dp11	**High threshold of P3 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q4_lt_dp11	**Low threshold of P3 Q4 depth for drop precedence = 2'b11. Unit: page size**

00001B40 MMDPR_11_Q5 P3 Drop Precedence control 11 of Q5 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						P3Q5_pr_dp11						P3Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q5_ht_dp11[3:0]							P3Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q5_pr_dp11	**Drop probability of P3 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q5_ht_dp11	**High threshold of P3 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q5_lt_dp11	**Low threshold of P3 Q5 depth for drop precedence = 2'b11. Unit: page size**

00001B44 MMDPR_11_Q6 P3 Drop Precedence control 11 of Q6 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q6_pr_dp11						P3Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q6_ht_dp11[3:0]							P3Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q6_pr_dp11	**Drop probability of P3 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q6_ht_dp11	**High threshold of P3 Q6 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q6_lt_dp11	**Low threshold of P3 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001B48 MMDPR_11_Q7 P3 Drop Precedence control 11 of Q7 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q7_pr_dp11						P3Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q7_ht_dp11[3:0]							P3Q7_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q7_pr_dp11	**Drop probability of P3 Q7 for drop precedence = 2'b11.**

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		0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P3Q7_ht_dp11	**High threshold of P3 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P3Q7_lt_dp11	**Low threshold of P3 Q7 depth for drop precedence = 2'b11. Unit: page size**

00001C00 IRLCR_P4 Ingress Rate Limit Control Register of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P4			IGC_RATE_CIR_16_P4	IGC_RATE_EXP_P4_IGC_TB_T_P4				IGC_TB_EN_P4	IGC_RATE_MAN_P4_IGC_TB_CBS_P4						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P4	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P4	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control Disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P4	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P4_IGC_TB_T_P4	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P4	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P4_IGC_TB_CBS_P4	**Mantissa part of port 4 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

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00001C04 FPC_RXCTRL_P4 Free Page Count at RX_CTRL of Port 4 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P4		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P4	**It indicates the free page count at RX_CTRL module.**

00001C0C MMDPR_10_Q0P4 Drop Precedence control 10 of Q0 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P4_DP_en					P4Q0_pr_dp10						P4Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q0_ht_dp10[3:0]							P4Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P4_DP_en	**Enable Drop Precedence function of P4. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P4Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P4Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P4Q0_lt_dp10 <= queue depth < P4Q0_ht_dp10, the drop probability of incoming packet is based on the setting P4Q0_pr_dp10. 0: Disable 1: Enable
26:24	P4Q0_pr_dp10	**Drop probability of P4 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q0_ht_dp10	**High threshold of P4 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q0_lt_dp10	**Low threshold of P4 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001C10 MMDPR_10_Q1P4 Drop Precedence control 10 of Q1 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q1_pr_dp10						P4Q1_ht_dp10[8:4]				
Type						RW						RW				

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Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q1_ht_dp10[3:0]							P4Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q1_pr_dp10	**Drop probability of P4 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q1_ht_dp10	**High threshold of P4 Q1 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q1_lt_dp10	**Low threshold of P4 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001C14 MMDPR_10_Q2 P4 Drop Precedence control 10 of Q2 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q2_pr_dp10						P4Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q2_ht_dp10[3:0]							P4Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q2_pr_dp10	**Drop probability of P4 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q2_ht_dp10	**High threshold of P4 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q2_lt_dp10	**Low threshold of P4 Q2 depth for drop precedence = 2'b10. Unit: page size**

00001C18 MMDPR_10_Q3 P4 Drop Precedence control 10 of Q3 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q3_pr_dp10						P4Q3_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q3_ht_dp10[3:0]							P4Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q3_pr_dp10	**Drop probability of P4 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5%

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		0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q3_ht_dp10	**High threshold of P4 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q3_lt_dp10	**Low threshold of P4 Q3 depth for drop precedence = 2'b10. Unit: page size**

00001C1C MMDPR_10_Q4 P4 Drop Precedence control 10 of Q4 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q4_pr_dp10						P4Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q4_ht_dp10[3:0]							P4Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q4_pr_dp10	**Drop probability of P4 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q4_ht_dp10	**High threshold of P4 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q4_lt_dp10	**Low threshold of P4 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001C20 MMDPR_10_Q5 P4 Drop Precedence control 10 of Q5 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q5_pr_dp10						P4Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q5_ht_dp10[3:0]							P4Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q5_pr_dp10	**Drop probability of P4 Q5 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q5_ht_dp10	**High threshold of P4 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q5_lt_dp10	**Low threshold of P4 Q5 depth for drop precedence = 2'b10. Unit: page size**

00001C24 MMDPR_10_Q6 P4 Drop Precedence control 10 of Q6 Port 4 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q6_pr_dp10						P4Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q6_ht_dp10[3:0]							P4Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q6_pr_dp10	**Drop probability of P4 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q6_ht_dp10	**High threshold of P4 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q6_lt_dp10	**Low threshold of P4 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001C28 MMDPR_10_Q7 P4 Drop Precedence control 10 of Q7 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q7_pr_dp10						P4Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q7_ht_dp10[3:0]							P4Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q7_pr_dp10	**Drop probability of P4 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q7_ht_dp10	**High threshold of P4 Q7 depth for drop precedence = 2'b10. Unit: page size**
8:0	P4Q7_lt_dp10	**Low threshold of P4 Q7 depth for drop precedence = 2'b10. Unit: page size**

00001C2C MMDPR_11_Q0 P4 Drop Precedence control 11 of Q0 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q0_pr_dp11						P4Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q0_ht_dp11[3:0]							P4Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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26:24	P4Q0_pr_dp11	**Drop probability of P4 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q0_ht_dp11	**High threshold of P4 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q0_lt_dp11	**Low threshold of P4 Q0 depth for drop precedence = 2'b11. Unit: page size**

00001C30 MMDPR_11_Q1 P4 Drop Precedence control 11 of Q1 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q1_pr_dp11						P4Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q1_ht_dp11[3:0]							P4Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q1_pr_dp11	**Drop probability of P4 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q1_ht_dp11	**High threshold of P4 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q1_lt_dp11	**Low threshold of P4 Q1 depth for drop precedence = 2'b11. Unit: page size**

00001C34 MMDPR_11_Q2 P4 Drop Precedence control 11 of Q2 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q2_pr_dp11						P4Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q2_ht_dp11[3:0]							P4Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q2_pr_dp11	**Drop probability of P4 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q2_ht_dp11	**High threshold of P4 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q2_lt_dp11	**Low threshold of P4 Q2 depth for drop precedence = 2'b11. Unit: page size**

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00001C38 MMDPR_11_Q3 P4 Drop Precedence control 11 of Q3 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q3_pr_dp11						P4Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q3_ht_dp11[3:0]							P4Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q3_pr_dp11	**Drop probability of P4 Q3 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q3_ht_dp11	**High threshold of P4 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q3_lt_dp11	**Low threshold of P4 Q3 depth for drop precedence = 2'b11. Unit: page size**

00001C3C MMDPR_11_Q4 P4 Drop Precedence control 11 of Q4 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q4_pr_dp11						P4Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q4_ht_dp11[3:0]							P4Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q4_pr_dp11	**Drop probability of P4 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q4_ht_dp11	**High threshold of P4 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q4_lt_dp11	**Low threshold of P4 Q4 depth for drop precedence = 2'b11. Unit: page size**

00001C40 MMDPR_11_Q5 P4 Drop Precedence control 11 of Q5 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q5_pr_dp11						P4Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q5_ht_dp11[3:0]							P4Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:24	P4Q5_pr_dp11	**Drop probability of P4 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q5_ht_dp11	**High threshold of P4 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q5_lt_dp11	**Low threshold of P4 Q5 depth for drop precedence = 2'b11. Unit: page size**

00001C44 MMDPR_11_Q6 P4 Drop Precedence control 11 of Q6 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q6_pr_dp11						P4Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q6_ht_dp11[3:0]							P4Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q6_pr_dp11	**Drop probability of P4 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q6_ht_dp11	**High threshold of P4 Q6 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q6_lt_dp11	**Low threshold of P4 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001C48 MMDPR_11_Q7 P4 Drop Precedence control 11 of Q7 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q7_pr_dp11						P4Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q7_ht_dp11[3:0]							P4Q7_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q7_pr_dp11	**Drop probability of P4 Q7 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q7_ht_dp11	**High threshold of P4 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P4Q7_lt_dp11	**Low threshold of P4 Q7 depth for drop precedence = 2'b11. Unit: page size**

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00001D00 IRLCR_P5 Ingress Rate Limit Control Register of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P5			IGC_RATE_CIR_16_P5	IGC_RATE_EXP_P5_IGC_TB_T_P5				IGC_TB_EN_P5	IGC_RATE_MAN_P5_IGC_TB_CBS_P5						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P5	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P5	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control Disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P5	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P5_IGC_TB_T_P5	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P5	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P5_IGC_TB_CBS_P5	**Mantissa part of port 5 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001D04 FPC_RXCTRL_P5 Free Page Count at RX_CTRL of Port 5 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P5		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P5	**It indicates the free page count at RX_CTRL module.**

00001D0C MMDPR_10_Q0 P5 Drop Precedence control 10 of Q0 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P5_DP_en					P5Q0_pr_dp10						P5Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q0_ht_dp10[3:0]							P5Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P5_DP_en	**Enable Drop Precedence function of P5. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P5Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P5Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P5Q0_lt_dp10 <= queue depth < P5Q0_ht_dp10, the drop probability of incoming packet is based on the setting P5Q0_pr_dp10. 0: Disable 1: Enable
26:24	P5Q0_pr_dp10	**Drop probability of P5 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q0_ht_dp10	**High threshold of P5 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q0_lt_dp10	**Low threshold of P5 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001D10 MMDPR_10_Q1 P5 Drop Precedence control 10 of Q1 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q1_pr_dp10						P5Q1_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q1_ht_dp10[3:0]							P5Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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26:24	P5Q1_pr_dp10	**Drop probability of P5 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q1_ht_dp10	**High threshold of P5 Q1 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q1_lt_dp10	**Low threshold of P5 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001D14 MMDPR_10_Q2 P5 Drop Precedence control 10 of Q2 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q2_pr_dp10						P5Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q2_ht_dp10[3:0]							P5Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q2_pr_dp10	**Drop probability of P5 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q2_ht_dp10	**High threshold of P5 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q2_lt_dp10	**Low threshold of P5 Q2 depth for drop precedence = 2'b10. Unit: page size**

00001D18 MMDPR_10_Q3 P5 Drop Precedence control 10 of Q3 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q3_pr_dp10						P5Q3_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q3_ht_dp10[3:0]							P5Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q3_pr_dp10	**Drop probability of P5 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q3_ht_dp10	**High threshold of P5 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q3_lt_dp10	**Low threshold of P5 Q3 depth for drop precedence = 2'b10. Unit: page size**

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00001D1C MMDPR_10_Q4 P5 Drop Precedence control 10 of Q4 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q4_pr_dp10						P5Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q4_ht_dp10[3:0]							P5Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q4_pr_dp10	**Drop probability of P5 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q4_ht_dp10	**High threshold of P5 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q4_lt_dp10	**Low threshold of P5 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001D20 MMDPR_10_Q5 P5 Drop Precedence control 10 of Q5 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q5_pr_dp10						P5Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q5_ht_dp10[3:0]							P5Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q5_pr_dp10	**Drop probability of P5 Q5 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q5_ht_dp10	**High threshold of P5 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q5_lt_dp10	**Low threshold of P5 Q5 depth for drop precedence = 2'b10. Unit: page size**

00001D24 MMDPR_10_Q6 P5 Drop Precedence control 10 of Q6 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q6_pr_dp10						P5Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q6_ht_dp10[3:0]							P5Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
26:24	P5Q6_pr_dp10	**Drop probability of P5 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q6_ht_dp10	**High threshold of P5 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q6_lt_dp10	**Low threshold of P5 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001D28 MMDPR_10_Q7 P5 Drop Precedence control 10 of Q7 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q7_pr_dp10						P5Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q7_ht_dp10[3:0]							P5Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q7_pr_dp10	**Drop probability of P5 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q7_ht_dp10	**High threshold of P5 Q7 depth for drop precedence = 2'b10. Unit: page size**
8:0	P5Q7_lt_dp10	**Low threshold of P5 Q7 depth for drop precedence = 2'b10. Unit: page size**

00001D2C MMDPR_11_Q0 P5 Drop Precedence control 11 of Q0 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q0_pr_dp11						P5Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q0_ht_dp11[3:0]							P5Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q0_pr_dp11	**Drop probability of P5 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q0_ht_dp11	**High threshold of P5 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q0_lt_dp11	**Low threshold of P5 Q0 depth for drop precedence = 2'b11. Unit: page size**

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00001D30 MMDPR_11_Q1 P5 Drop Precedence control 11 of Q1 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q1_pr_dp11						P5Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q1_ht_dp11[3:0]							P5Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q1_pr_dp11	**Drop probability of P5 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q1_ht_dp11	**High threshold of P5 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q1_lt_dp11	**Low threshold of P5 Q1 depth for drop precedence = 2'b11. Unit: page size**

00001D34 MMDPR_11_Q2 P5 Drop Precedence control 11 of Q2 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q2_pr_dp11						P5Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q2_ht_dp11[3:0]							P5Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q2_pr_dp11	**Drop probability of P5 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q2_ht_dp11	**High threshold of P5 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q2_lt_dp11	**Low threshold of P5 Q2 depth for drop precedence = 2'b11. Unit: page size**

00001D38 MMDPR_11_Q3 P5 Drop Precedence control 11 of Q3 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q3_pr_dp11						P5Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	P5Q3_ht_dp11[3:0]							P5Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q3_pr_dp11	**Drop probability of P5 Q3 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q3_ht_dp11	**High threshold of P5 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q3_lt_dp11	**Low threshold of P5 Q3 depth for drop precedence = 2'b11. Unit: page size**

00001D3C MMDPR_11_Q4 P5 Drop Precedence control 11 of Q4 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q4_pr_dp11						P5Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q4_ht_dp11[3:0]							P5Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q4_pr_dp11	**Drop probability of P5 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q4_ht_dp11	**High threshold of P5 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q4_lt_dp11	**Low threshold of P5 Q4 depth for drop precedence = 2'b11. Unit: page size**

00001D40 MMDPR_11_Q5 P5 Drop Precedence control 11 of Q5 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q5_pr_dp11						P5Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q5_ht_dp11[3:0]							P5Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q5_pr_dp11	**Drop probability of P5 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%

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		(n=2~6)
20:12	P5Q5_ht_dp11	**High threshold of P5 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q5_lt_dp11	**Low threshold of P5 Q5 depth for drop precedence = 2'b11. Unit: page size**

00001D44 MMDPR_11_Q6 P5 Drop Precedence control 11 of Q6 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q6_pr_dp11						P5Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q6_ht_dp11[3:0]							P5Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q6_pr_dp11	**Drop probability of P5 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q6_ht_dp11	**High threshold of P5 Q6 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q6_lt_dp11	**Low threshold of P5 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001D48 MMDPR_11_Q7 P5 Drop Precedence control 11 of Q7 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q7_pr_dp11						P5Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q7_ht_dp11[3:0]							P5Q7_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q7_pr_dp11	**Drop probability of P5 Q7 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P5Q7_ht_dp11	**High threshold of P5 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P5Q7_lt_dp11	**Low threshold of P5 Q7 depth for drop precedence = 2'b11. Unit: page size**

00001E00 IRLCR_P6 Ingress Rate Limit Control Register of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P6															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P6			IGC_RATE_CIR_16_P6	IGC_RATE_EXP_P6_IGC_TB_T_P6				IGC_TB_EN_P6	IGC_RATE_MAN_P6_IGC_TB_CBS_P6						
Type	RW			RW	RW				RW	RW						
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P6	**Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps**
15	IGC_RATE_EN_P6	**EXP: ingress_rate_limit_exp** MAN: ingress_rate_limit_man The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps 0: Ingress rate limit control Disable 1: Ingress rate limit control Enable
12	IGC_RATE_CIR_16_P6	**Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value**
11:8	IGC_RATE_EXP_P6_IGC_TB_T_P6	**Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),** When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms 15: 128ms
7	IGC_TB_EN_P6	**When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.** Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
6:0	IGC_RATE_MAN_P6_IGC_TB_CBS_P6	**Mantissa part of port 6 ingress rate limit control Value range: 0..127 (7-bit),** when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001E04 FPC_RXCTRL_P6 Free Page Count at RX_CTRL of Port 6 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P6		
Type														RO		
Reset														0	1	1

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Bit(s)	Name	Description
2:0	FPC_RXCTRL_P6	**It indicates the free page count at RX_CTRL module.**

00001E0C MMDPR_10_Q0 P6 Drop Precedence control 10 of Q0 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P6_DP_en					P6Q0_pr_dp10						P6Q0_ht_dp10[8:4]				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q0_ht_dp10[3:0]							P6Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P6_DP_en	**Enable Drop Precedence function of P6. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)** **(1) When queue depth >= P6Q0_ht_dp10, the drop probability of the incoming packet is 100%.** (2) When queue depth < P6Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P6Q0_lt_dp10 <= queue depth < P6Q0_ht_dp10, the drop probability of incoming packet is based on the setting P6Q0_pr_dp10. 0: Disable 1: Enable
26:24	P6Q0_pr_dp10	**Drop probability of P6 Q0 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q0_ht_dp10	**High threshold of P6 Q0 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q0_lt_dp10	**Low threshold of P6 Q0 depth for drop precedence = 2'b10. Unit: page size**

00001E10 MMDPR_10_Q1 P6 Drop Precedence control 10 of Q1 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q1_pr_dp10						P6Q1_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q1_ht_dp10[3:0]							P6Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q1_pr_dp10	**Drop probability of P6 Q1 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q1_ht_dp10	**High threshold of P6 Q1 depth for drop precedence = 2'b10. Unit: page size**

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8:0	P6Q1_lt_dp10	**Low threshold of P6 Q1 depth for drop precedence = 2'b10. Unit: page size**

00001E14 MMDPR_10_Q2 P6 Drop Precedence control 10 of Q2 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q2_pr_dp10						P6Q2_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q2_ht_dp10[3:0]							P6Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q2_pr_dp10	**Drop probability of P6 Q2 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q2_ht_dp10	**High threshold of P6 Q2 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q2_lt_dp10	**Low threshold of P6 Q2 depth for drop precedence = 2'b10. Unit: page size**

00001E18 MMDPR_10_Q3 P6 Drop Precedence control 10 of Q3 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q3_pr_dp10						P6Q3_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q3_ht_dp10[3:0]							P6Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q3_pr_dp10	**Drop probability of P6 Q3 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q3_ht_dp10	**High threshold of P6 Q3 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q3_lt_dp10	**Low threshold of P6 Q3 depth for drop precedence = 2'b10. Unit: page size**

00001E1C MMDPR_10_Q4 P6 Drop Precedence control 10 of Q4 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q4_pr_dp10						P6Q4_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q4_ht_dp10[3:0]							P6Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q4_pr_dp10	**Drop probability of P6 Q4 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q4_ht_dp10	**High threshold of P6 Q4 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q4_lt_dp10	**Low threshold of P6 Q4 depth for drop precedence = 2'b10. Unit: page size**

00001E20 MMDPR_10_Q5 P6 Drop Precedence control 10 of Q5 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q5_pr_dp10						P6Q5_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q5_ht_dp10[3:0]							P6Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q5_pr_dp10	**Drop probability of P6 Q5 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q5_ht_dp10	**High threshold of P6 Q5 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q5_lt_dp10	**Low threshold of P6 Q5 depth for drop precedence = 2'b10. Unit: page size**

00001E24 MMDPR_10_Q6 P6 Drop Precedence control 10 of Q6 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q6_pr_dp10						P6Q6_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q6_ht_dp10[3:0]							P6Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q6_pr_dp10	**Drop probability of P6 Q6 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%

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		(n=2~6)
20:12	P6Q6_ht_dp10	**High threshold of P6 Q6 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q6_lt_dp10	**Low threshold of P6 Q6 depth for drop precedence = 2'b10. Unit: page size**

00001E28 MMDPR_10_Q7 P6 Drop Precedence control 10 of Q7 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q7_pr_dp10						P6Q7_ht_dp10[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q7_ht_dp10[3:0]							P6Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q7_pr_dp10	**Drop probability of P6 Q7 for drop precedence = 2'b10.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q7_ht_dp10	**High threshold of P6 Q7 depth for drop precedence = 2'b10. Unit: page size**
8:0	P6Q7_lt_dp10	**Low threshold of P6 Q7 depth for drop precedence = 2'b10. Unit: page size**

00001E2C MMDPR_11_Q0 P6 Drop Precedence control 11 of Q0 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q0_pr_dp11						P6Q0_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q0_ht_dp11[3:0]							P6Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q0_pr_dp11	**Drop probability of P6 Q0 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q0_ht_dp11	**High threshold of P6 Q0 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q0_lt_dp11	**Low threshold of P6 Q0 depth for drop precedence = 2'b11. Unit: page size**

00001E30 MMDPR_11_Q1 P6 Drop Precedence control 11 of Q1 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name						P6Q1_pr_dp11						P6Q1_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q1_ht_dp11[3:0]							P6Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q1_pr_dp11	**Drop probability of P6 Q1 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q1_ht_dp11	**High threshold of P6 Q1 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q1_lt_dp11	**Low threshold of P6 Q1 depth for drop precedence = 2'b11. Unit: page size**

00001E34 MMDPR_11_Q2 P6 Drop Precedence control 11 of Q2 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q2_pr_dp11						P6Q2_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q2_ht_dp11[3:0]							P6Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q2_pr_dp11	**Drop probability of P6 Q2 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q2_ht_dp11	**High threshold of P6 Q2 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q2_lt_dp11	**Low threshold of P6 Q2 depth for drop precedence = 2'b11. Unit: page size**

00001E38 MMDPR_11_Q3 P6 Drop Precedence control 11 of Q3 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q3_pr_dp11						P6Q3_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q3_ht_dp11[3:0]							P6Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q3_pr_dp11	**Drop probability of P6 Q3 for drop precedence = 2'b11.**

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		0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q3_ht_dp11	**High threshold of P6 Q3 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q3_lt_dp11	**Low threshold of P6 Q3 depth for drop precedence = 2'b11. Unit: page size**

00001E3C MMDPR_11_Q4 P6 Drop Precedence control 11 of Q4 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q4_pr_dp11						P6Q4_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q4_ht_dp11[3:0]							P6Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q4_pr_dp11	**Drop probability of P6 Q4 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q4_ht_dp11	**High threshold of P6 Q4 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q4_lt_dp11	**Low threshold of P6 Q4 depth for drop precedence = 2'b11. Unit: page size**

00001E40 MMDPR_11_Q5 P6 Drop Precedence control 11 of Q5 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q5_pr_dp11						P6Q5_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q5_ht_dp11[3:0]							P6Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q5_pr_dp11	**Drop probability of P6 Q5 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q5_ht_dp11	**High threshold of P6 Q5 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q5_lt_dp11	**Low threshold of P6 Q5 depth for drop precedence = 2'b11. Unit: page size**

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00001E44 MMDPR_11_Q6 P6 Drop Precedence control 11 of Q6 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q6_pr_dp11						P6Q6_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q6_ht_dp11[3:0]							P6Q6_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q6_pr_dp11	**Drop probability of P6 Q6 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q6_ht_dp11	**High threshold of P6 Q6 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q6_lt_dp11	**Low threshold of P6 Q6 depth for drop precedence = 2'b11. Unit: page size**

00001E48 MMDPR_11_Q7 P6 Drop Precedence control 11 of Q7 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q7_pr_dp11						P6Q7_ht_dp11[8:4]				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q7_ht_dp11[3:0]							P6Q7_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q7_pr_dp11	**Drop probability of P6 Q7 for drop precedence = 2'b11.** 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5% (n=2~6)
20:12	P6Q7_ht_dp11	**High threshold of P6 Q7 depth for drop precedence = 2'b11. Unit: page size**
8:0	P6Q7_lt_dp11	**Low threshold of P6 Q7 depth for drop precedence = 2'b11. Unit: page size**

00001F60 PTP_CTRL PTP CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TIMESTAMP_EN			INT_1PPS_MODE			TIMESTAMP_1PPS									
Type	RW			RW			RW									
Reset	0			0			0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		INT_RFIFO_EVEN	INT_TFIFO_EVEN	INT_1PPS_EVEN		INT_RFIFO_EN	INT_TFIFO_EN	INT_1PPS_EN		PTP6_EN	PTP5_EN	PTP4_EN	PTP3_EN	PTP2_EN	PTP1_EN	PTP0_EN

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		T	T	T												
Type		W1C	W1C	W1C		RW	RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0		0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TIMESTAMP_EN	0: Timestamp counter is disabled. 1: Timestamp counter is enabled.
28	INT_1PPS_MODE	0: PPS interrupt is generated at second boundary 1: PPS interrupt is generated at second and half-second boundary
25:24	TIMESTAMP_1PPS	00: Internal 1PPS source. 01: External 1PPS source from IO pad 10: Reserved 11: Reserved
14	INT_RFIFO_EVENT	**This bit is cleared when written as 1.** 1: Interrupt event occurred when Timestamp FIFO for RX is not empty.
13	INT_TFIFO_EVENT	**This bit is cleared when written as 1.** 1: Interrupt event occurred when Timestamp FIFO for TX is not empty.
12	INT_1PPS_EVENT	**This bit is cleared when written as 1.** 1: PPS Interrupt event occurred.
10	INT_RFIFO_EN	0: Interrupt disabled when Timestamp FIFO for RX is not empty. 1: Interrupt enabled when Timestamp FIFO for RX is not empty.
9	INT_TFIFO_EN	0: Interrupt disabled when Timestamp FIFO for TX is not empty. 1: Interrupt enabled when Timestamp FIFO for TX is not empty.
8	INT_1PPS_EN	0: PPS Interrupt disabled. 1: PPS Interrupt enabled.
6	PTP6_EN	0: PTP is disabled for port 6. 1: PTP is enabled for port 6.
5	PTP5_EN	0: PTP is disabled for port 5. 1: PTP is enabled for port 5.
4	PTP4_EN	0: PTP is disabled for port 4. 1: PTP is enabled for port 4.
3	PTP3_EN	0: PTP is disabled for port 3. 1: PTP is enabled for port 3.
2	PTP2_EN	0: PTP is disabled for port 2. 1: PTP is enabled for port 2.
1	PTP1_EN	0: PTP is disabled for port 1. 1: PTP is enabled for port 1.
0	PTP0_EN	0: PTP is disabled for port 0. 1: PTP is enabled for port 0.

00001F68 TIMESTAMP_LSB TIMESTAMP SECOND COUNTER LSB REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMSTMP_S_LSB				TMSTMP_NS[27:16]											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMSTMP_NS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	TMSTMP_S_LSB	**This register holds the 4 least significant bits of the "seconds" part of the PTP timestamp. The value is latched when PTP_CTRL is read.**

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27:0	TMSTMP_NS	**This register holds the 28-bit 4-nanoseconds counter of the PTP timestamp. This counter is increased every 4-nanoseconds. The maximum value is 28'hEE6_B27F (10^9/4-1). The value is latched when PTP_CTRL is read.**

00001F70 TIMESTAMP_OFFSET_MODE TIMESTAMP OFFSET MODE REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TMSTMP_OFFSET_DONE							TMSTMP_OFFSET_MODE
Type									RO							RW
Reset									0							0

Bit(s)	Name	Description
7	TMSTMP_OFFSET_DONE	**This bit is self clearing.** 0: The offset did not update the timestamp counter. 1: The offset updated the timestamp counter.
0	TMSTMP_OFFSET_MODE	**In ABSOLUTE mode, the offset range is 16 seconds. In ADD mode, the offset should be positive or negative within 1 second.** 0: ADD mode 1: ABSOLUTE mode

00001F78 TIMESTAMP_OFFSET_LSB TIMESTAMP SECOND OFFSET LSB REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMSTMP_OFFSET_LSB				TMSTMP_NS_OFFSET[27:16]											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMSTMP_NS_OFFSET[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	TMSTMP_OFFSET_LSB	**This is the least significant bit of the offset to the "seconds" counter. In ADD mode, the field should be all zeros for positive offset or all ones for negative offset.**
27:0	TMSTMP_NS_OFFSET	**This is the offset to the 4-nanoseconds counter.** When this register is written, the values of the OFFSET registers update the counter according to the mode that was configured in the TIMESTAMP_OFFSET_MODE register. This register is self clearing. For negative offset of ADD mode, this field should be 10s complement. Taking -0.6 as example, this field should be (1 - 0.6) * 10^9 / 4.

00001F90 TIMESTAMP_TF TIMESTAMP TX FIFO CONTROL REGISTER 00000000

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IFO_CTRL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TMSTMP_TFIFO_FULL	TMSTMP_TFIFO_EMPTY	TMSTMP_TFIFO_OVR				TMSTMP_TFIFO_RST	TMSTMP_TFIFO_LOAD
Type									RO	RO	W1C				RW	WO
Reset									0	0	0				0	0

Bit(s)	Name	Description
7	TMSTMP_TFIFO_FULL	**When FIFO is full, the item written to the FIFO is discarded.** 0: Timestamp FIFO for TX is not full. 1: Timestamp FIFO for TX is full.
6	TMSTMP_TFIFO_EMPTY	**When FIFO is not empty, the first item is presented to the TMSTMP_TFIFO_NS and TMSTMP_TFIFO_MSB register.** 0: Timestamp FIFO for TX is not empty. 1: Timestamp FIFO for TX is empty.
5	TMSTMP_TFIFO_OVR	**This bit is cleared when written as 1.** 1: An overrun condition occurred in the Timestamp FIFO for TX.
1	TMSTMP_TFIFO_RST	1: This is the reset control to the timestamp FIFO. When this register is written as 1, the FIFO is cleared, and no writing operation can be performed.
0	TMSTMP_TFIFO_LOAD	**This bit is toggled when written as 1.** 1: This is the load control to the timestamp FIFO. When this register is written as 1, the next item in the timestamp FIFO is loaded to the TMSTMP_TFIFO_NS and TMSTMP_TFIFO_MSB register. And the TMSTMP_TFIFO_EMPTY is updated.

00001F98 TMSTMP_TFIFO_MSB TIMESTAMP TX FIFO MSB REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TMSTMP_TFIFO_SEQ		
Type														RO		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TMSTMP_TFIFO_MSG	
Type															RO	
Reset															0	0

Bit(s)	Name	Description
18:16	TMSTMP_TFIFO_SEQ	**This field holds the 3-bit sequence ID of the Timestamp FIFO. The value is latched when TMSTMP_TFIFO_LOAD is written as 1.**
1:0	TMSTMP_TFIFO_MSG	**This field holds the type of the PTP event message associated with the timestamp in the FIFO. The value is latched when TMSTMP_TFIFO_LOAD is written as 1.** 0: SYNC 1: DELAY_REQ 2: PDELAY_REQ 3: PDELAY_RESP

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00001F9C TMSTMP_TFIFO_NS TIMESTAMP TX FIFO NS REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMSTMP_TFIFO_S_LSB				TMSTMP_TFIFO_NS[27:16]											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMSTMP_TFIFO_NS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	TMSTMP_TFIFO_S_LSB	**This field holds the 4 least significant bits of the "seconds" part of the Timestamp FIFO. The value is latched when TMSTMP_TFIFO_LOAD is written as 1.**
27:0	TMSTMP_TFIFO_NS	**This field holds the 28-bit 4-nanoseconds part of the Timestamp FIFO. The value is latched when TMSTMP_TFIFO_LOAD is written as 1.**

00001FA0 TIMESTAMP_RFIFO_CTRL TIMESTAMP RX FIFO CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TMSTMP_RFIFO_FULL	TMSTMP_RFIFO_EMPTY	TMSTMP_RFIFO_OVR				TMSTMP_RFIFO_RST	TMSTMP_RFIFO_LOAD
Type									RO	RO	W1C				RW	WO
Reset									0	0	0				0	0

Bit(s)	Name	Description
7	TMSTMP_RFIFO_FULL	**When FIFO is full, the item written to the FIFO is discarded.** 0: Timestamp FIFO for RX is not full. 1: Timestamp FIFO for RX is full.
6	TMSTMP_RFIFO_EMPTY	**When FIFO is not empty, the first item is presented to the TMSTMP_RFIFO_NS and TMSTMP_RFIFO_MSB register.** 0: Timestamp FIFO for RX is not empty. 1: Timestamp FIFO for RX is empty.
5	TMSTMP_RFIFO_OVR	**This bit is cleared when written as 1.** 1: An overrun condition occurred in the Timestamp FIFO for RX.
1	TMSTMP_RFIFO_RST	1: This is the reset control to the timestamp FIFO. When this register is written as 1, the FIFO is cleared, and no writing operation can be performed.
0	TMSTMP_RFIFO_LOAD	**This bit is toggled when written as 1.** 1: This is the load control to the timestamp FIFO for RX. When this register is written as 1, the next item in the timestamp FIFO is loaded to the TMSTMP_RFIFO_NS and TMSTMP_RFIFO_MSB register. The TMSTMP_TFIFO_EMPTY is updated.

00001FA8 TMSTMP_RFIFO_MSB TIMESTAMP RX FIFO MSB REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name														TMSTMP_RFIFO_SEQ		
Type														RO		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TMSTMP_RFIFO_MSG	
Type															RO	
Reset															0	0

Bit(s)	Name	Description
18:16	TMSTMP_RFIFO_SEQ	**This field holds the 3-bit sequence ID of the Timestamp FIFO. The value is latched when TMSTMP_RFIFO_LOAD is written as 1.**
1:0	TMSTMP_RFIFO_MSG	**This field holds the type of the PTP event message associated with the timestamp in the FIFO for RX. The value is latched when TMSTMP_RFIFO_LOAD is written as 1.** 0: SYNC 1: DELAY_REQ 2: PDELAY_REQ 3: PDELAY_RESP

00001FAC TMSTMP_RFIFO_NS TIMESTAMP RX FIFO NS REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TMSTMP_RFIFO_S_LSB				TMSTMP_RFIFO_NS[27:16]											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMSTMP_RFIFO_NS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	TMSTMP_RFIFO_S_LSB	**This field holds the 4 least significant bits of the "seconds" part of the Timestamp RFIFO. The value is latched when TMSTMP_RFIFO_LOAD is written as 1.**
27:0	TMSTMP_RFIFO_NS	**This field holds the 28-bit 4-nanoseconds part of the Timestamp FIFO for RX. The value is latched when TMSTMP_RFIFO_LOAD is written as 1.**

00001FC0 FPLC Free Page Link Count Register 01EE01EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MIN_FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0

Bit(s)	Name	Description
25:16	MIN_FREE_PL_CNT	**Minimal Free Page Link Count in LMU from last read access**
9:0	FREE_PL_CNT	**Free Page Link Count in LMU**

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00001FE0 GFCCR0 Global Flow_Control Control Register 0 A0087858

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_EN		FC_OFF2ON_OPT	FC_ON2OFF_OPT					FC_PORT_BLK_THD							
Type	RW		RW	RW					RW							
Reset	1		1	0					0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FC_FREE_BLK_HITHD								FC_FREE_BLK_LOTHD							
Type	RW								RW							
Reset	0	1	1	1	1	0	0	0	0	1	0	1	1	0	0	0

Bit(s)	Name	Description
31	FC_EN	0: Disable flow control 1: Enable flow control
29	FC_OFF2ON_OPT	**Flow control assertion option** 0: Disable 1: Enable aggressive frame discard option in flow control transition from OFF to ON
28	FC_ON2OFF_OPT	**Flow control de-assertion option** 0: Disable 1: Enable aggressive frame discard option in flow control transition from ON to OFF
23:16	FC_PORT_BLK_THD	**Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)**
15:8	FC_FREE_BLK_HITHD	**High water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.**
7:0	FC_FREE_BLK_LOTHD	**Low water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.**

00001FE4 GFCCR1 Global Flow_Control Control Register 1 44444444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_BLK_THD_Q7				FC_BLK_THD_Q6				FC_BLK_THD_Q5				FC_BLK_THD_Q4			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FC_BLK_THD_Q3				FC_BLK_THD_Q2				FC_BLK_THD_Q1				FC_BLK_THD_Q0			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	FC_BLK_THD_Q7	**TX Queue 7 block threshold for flow control**
27:24	FC_BLK_THD_Q6	**TX Queue 6 block threshold for flow control**
23:20	FC_BLK_THD_Q5	**TX Queue 5 block threshold for flow control**
19:16	FC_BLK_THD_Q4	**TX Queue 4 block threshold for flow control**
15:12	FC_BLK_THD_Q3	**TX Queue 3 block threshold for flow control**
11:8	FC_BLK_THD_Q2	**TX Queue 2 block threshold for flow control**
7:4	FC_BLK_THD_Q1	**TX Queue 1 block threshold for flow control**
3:0	FC_BLK_THD_Q0	**TX Queue 0 block threshold for flow control**

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00001FE8 FCBRCR0 Flow Control Block Reservation Control Register for group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_RSV_GRP0_EN								FC_RSV_GRP0_PMAP							
Type	RW								RW							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FC_RSV_GRP0_BLK_NUM				FC_RSV_GRP0_QMAP							
Type					RW				RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	FC_RSV_GRP0_EN	0: Disable 1: Enable queue block reservation group 0
23:16	FC_RSV_GRP0_PMAP	**When FC_RSV_GRP0_EN=1,** Port map for queue block reservation group 0 Note: assume 8 port TBD (unit size? Mapping method?)
11:8	FC_RSV_GRP0_BLK_NUM	**When FC_RSV_GRP0_EN=1,** Block size for queue block reservation group 0 Unit: TBD
7:0	FC_RSV_GRP0_QMAP	**When FC_RSV_GRP0_EN=1,** Queue map for queue block reservation group 0 Unit: TBD

00001FEC FCBRCR1 Flow Control Block Reservation Control Register for group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_RSV_GRP1_EN								FC_RSV_GRP1_PMAP							
Type	RW								RW							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FC_RSV_GRP1_BLK_NUM				FC_RSV_GRP1_QMAP							
Type					RW				RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	FC_RSV_GRP1_EN	0: Disable 1: Enable queue block reservation group 0
23:16	FC_RSV_GRP1_PMAP	**When FC_RSV_GRP1_EN=1,** Port map for queue block reservation group 1 Note: assume 8 port TBD (unit size? Mapping method?)
11:8	FC_RSV_GRP1_BLK_NUM	**When FC_RSV_GRP1_EN=1,** Block size for queue block reservation group 1 Unit: TBD
7:0	FC_RSV_GRP1_QMAP	**When FC_RSV_GRP1_EN=1,** Queue map for queue block reservation group 1 Unit: TBD

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00001FF0 GIRLCR Global Ingress Rate Limit Control Register 00110104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IGC_FC_OFF_THD				IGC_FC_DROP_THD			
Type									RW				RW			
Reset									0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IGC_MFRM_EX	IGC_IPG_OP	IGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
23:20	IGC_FC_OFF_THD	**Ingress Rate Limit Pause-Off Threshold** Pause-off frame is sent when the ingress token bucket is higher than pause-off threshold. Threshold = max_bucket_size >> igc_fc_off_thd
19:16	IGC_FC_DROP_THD	**Ingress Rate Limit Drop Threshold** If Port Flow Control and rate limit control is enabled, frame is drop when the ingress token bucket is less than drop threshold. Threshold = -(max_bucket_size >> igc_fc_drop_thd)
9	IGC_MFRM_EX	**Ingress Rate Excludes Management Frames** Management frames will be ignored by rate limit. (management frame type is set by ARL registers) 0: Include management frames 1: Exclude management frames
8	IGC_IPG_OP	**Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation.** 0: IPG byte is excluded 1: IPG byte is included
7:0	IGC_IPG_BYTE	**Ingress Rate IPG Byte Count** Byte count should be added while calculating the rate limit 8'h4: add 4 byte CRC (byte rate calculation) 8'h18: add 4 byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation)

00001FF4 GFCCR2 Global Flow_Control Control Register 2 0000120C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FC_PORT_BLK_HI_THD								FC_QUE_BLK_HI_THD							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
15:8	FC_PORT_BLK_HI_THD	**Number of port block high threshold (unit: 2 blocks) associated with packet discard mechanism**
7:0	FC_QUE_BLK_HI_THD	**Number of queue block high threshold (unit: 2 blocks) associated with packet discard mechanism**

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00002000 SSC STP State Control of P0 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**
11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

00002004 PCR Port Control of P0 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**
26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**

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12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Look up the ACL Table and take corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable** All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame is processed according to PORT_VLAN. 1'b1: VLAN mismatched frame is copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port do not belong to the VLAN member. Discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002008 PIC Port IGMP Control of P0 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

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Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed from the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed from the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).

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4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD-specific query message doe not refresh the IP multicast table. 1: This port is capable of recognizing the MLD-specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP-specific query message does not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP-specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000200C PSC Port Security Control of P0 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Set the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and is not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or the received frames that are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX).

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		2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002010 PVC Port VLAN Control of P0 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port

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5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002014 PPBV1 Port-and-Protocol Based VLAN I of P0 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)** The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002018 PPBV2 Port-and-Protocol Based VLAN II of P0 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

0000201C BSR Broadcast Storm Rate Control of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

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15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002020 STAG01 STAG Index 0/1 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002024 STAG23 STAG Index 2/3 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002028 STAG45 STAG Index 4/5 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

0000202C STAG67 STAG Index 6/7 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**
11:0	VID6	**VLAN Identifier for STAG index 6**

00002100 SSC STP State Control of P1 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**
11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

00002104 PCR Port Control of P1 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**
26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**
12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable** All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped

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3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame is processed according to PORT_VLAN. 1'b1: VLAN mismatched frame is copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. Discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002108 PIC Port IGMP Control of P1 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.

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		0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000210C PSC Port Security Control of P1 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW

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Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002110 PVC Port VLAN Control of P1 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.

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15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002114 PPBV1 Port-and-Protocol Based VLAN I of P1 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)** The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002118 PPBV2 Port-and-Protocol Based VLAN II of P1 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

0000211C BSR Broadcast Storm Rate Control of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002120 STAG01 STAG Index 0/1 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002124 STAG23 STAG Index 2/3 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002128 STAG45 STAG Index 4/5 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

0000212C STAG67 STAG Index 6/7 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**
11:0	VID6	**VLAN Identifier for STAG index 6**

00002200 SSC STP State Control of P2 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**
11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

00002204 PCR Port Control of P2 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**
26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**
12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority 0: Disable

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		1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable** All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002208 PIC Port IGMP Control of P2 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port.

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		[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the

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		specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000220C PSC Port Security Control of P2 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock.

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0: Receive authorized.
1: Disable frame receiving.

00002210 PVC Port VLAN Control of P2 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.

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3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002214 PPBV1 Port-and-Protocol Based VLAN I of P2 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)** The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002218 PPBV2 Port-and-Protocol Based VLAN II of P2 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**

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27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

0000221C BSR Broadcast Storm Rate Control of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps

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8'h1: (1* STORM_UNIT) packets or bps

00002220 STAG01 STAG Index 0/1 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002224 STAG23 STAG Index 2/3 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002228 STAG45 STAG Index 4/5 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

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0000222C STAG67 STAG Index 6/7 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**
11:0	VID6	**VLAN Identifier for STAG index 6**

00002300 SSC STP State Control of P3 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**
11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

00002304 PCR Port Control of P3 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding Enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**
26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**
12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable** All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member.

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2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table.
2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002308 PIC Port IGMP Control of P3 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.

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8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000230C PSC Port Security Control of P3 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table

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		12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002310 PVC Port VLAN Control of P3 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID

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		1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002314 PPBV1 Port-and-Protocol Based VLAN I of P3 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)**

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		The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002318 PPBV2 Port-and-Protocol Based VLAN II of P3 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

0000231C BSR Broadcast Storm Rate Control of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame

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		1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002320 STAG01 STAG Index 0/1 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002324 STAG23 STAG Index 2/3 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**

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23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002328 STAG45 STAG Index 4/5 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

0000232C STAG67 STAG Index 6/7 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**
11:0	VID6	**VLAN Identifier for STAG index 6**

00002400 SSC STP State Control of P4 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**

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11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

00002404 PCR Port Control of P4 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**
26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**
12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable**

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		All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002408 PIC Port IGMP Control of P4 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress

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		port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table.

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1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000240C PSC Port Security Control of P4 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002410 PVC Port VLAN Control of P4 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type**

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2'b00: Admit All frames
2'b01: Admit Only VLAN-tagged frames
2'b10: Admit only untagged or priority-tagged frames.
2'b11: Reserved

00002414 PPBV1 Port-and-Protocol Based VLAN I of P4 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)** The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002418 PPBV2 Port-and-Protocol Based VLAN II of P4 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

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0000241C BSR Broadcast Storm Rate Control of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002420 STAG01 STAG Index 0/1 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											

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Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002424 STAG23 STAG Index 2/3 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002428 STAG45 STAG Index 4/5 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

0000242C STAG67 STAG Index 6/7 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**
11:0	VID6	**VLAN Identifier for STAG index 6**

00002500 SSC STP State Control of P5 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**
11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

00002504 PCR Port Control of P5 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**

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26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**
12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable** All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames once if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002508 **PIC** **Port IGMP Control of P5** **00008000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_	IGMP_MIS		

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													MIR			
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR

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		Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000250C PSC Port Security Control of P5 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable

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		1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002510 PVC Port VLAN Control of P5 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged

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		3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002514 PPBV1 Port-and-Protocol Based VLAN I of P5 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)** The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

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00002518 PPBV2 Port-and-Protocol Based VLAN II of P5 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

0000251C BSR Broadcast Storm Rate Control of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us

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25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002520 STAG01 STAG Index 0/1 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002524 STAG23 STAG Index 2/3 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002528 STAG45 STAG Index 4/5 of P5 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

0000252C STAG67 STAG Index 6/7 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**
11:0	VID6	**VLAN Identifier for STAG index 6**

00002600 SSC STP State Control of P6 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	DC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15:14	FID7_PST	**(Rapid) Spanning Tree Protocol Port State**
13:12	FID6_PST	**(Rapid) Spanning Tree Protocol Port State**
11:10	FID5_PST	**(Rapid) Spanning Tree Protocol Port State**
9:8	FID4_PST	**(Rapid) Spanning Tree Protocol Port State**
7:6	FID3_PST	**(Rapid) Spanning Tree Protocol Port State**
5:4	FID2_PST	**(Rapid) Spanning Tree Protocol Port State**
3:2	FID1_PST	**(Rapid) Spanning Tree Protocol Port State**
1:0	FID0_PST	**(Rapid) Spanning Tree Protocol Port State**

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00002604 PCR Port Control of P6 00FF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	DC	RW	RW		DC	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	DC			RW	RW	RW	RW	RW	RW	RW			DC	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	**Reserved**
30	MLDv2_EN	**IPv6 MLDv2 source address multicast forwarding enable** 0: Disable 1: Enable
29:28	EG_TAG	**Port-Based Egress VLAN Tag Attribution** 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	**Reserved**
26:24	PORT_PRI	**Port-based User Priority** User priority for the ingress port
23:16	PORT_MATRIX	**Port Matrix Member** The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	**Reserved**
12	UP2DSCP_EN	**User Priority to DSCP Enable** Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	**User Priority to Tag Enable** Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	**Port-based ACL Enable** 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	**Port Tx Mirror Enable** All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	**Port Rx Mirror Enable** All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	**ACL Mismatch to Mirror Port** Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable

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		1: Enable
6:4	MIS_PORT_FW	**ACL Mismatch TO_CPU Forward** Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	**Reserved**
2	VLAN_MIS	**VLAN Mismatch to Mirror Port** 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	**Port-based VLAN Mechanism Select** 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002608 PIC Port IGMP Control of P6 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	DC												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	DC		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	IGMP_MIR	**IP Multicast IGMP Table Mismatch to Mirror Port** Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	**IP Multicast "TO_CPU" Forwarding** Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	**Robustness Variable** Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default)

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		3: Three times
13	MLD_HW_LEAVE	**MLD HW Leave Enable** Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	**IGMP HW Leave Enable** Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	**IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x** 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	**IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx** 1'b0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	**IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx** 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	**MLD v2 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	**IGMP v3 HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	**MLD Snooping HW Join Enable** 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	**IGMP Snooping HW Join Enable** Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	**MLD HW Specific Query Enable** 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	**IGMP HW Specific Query Enable** 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	**MLD HW General Query Enable** 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	**IGMP HW General Query Enable** 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

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0000260C PSC Port Security Control of P6 000FFF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN[11:8]			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_SA_LRN[7:0]								REV0		SA_CNT_EN	SA_DIS	SA_LOCK		TX_PORT_LOCK	RX_PORT_LOCK
Type	RW								DC		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	**Learned Source Address Number**
19:8	MAC_SA_LRN	**Rx SA Allowable Learning Number** Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	**Reserved**
5	SA_CNT_EN	**SA Counter Enable** Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	**SA Disable** Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	**SA Lock Select** [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frame whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	**Tx Port Lock Enable** [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	**Rx Port Lock Enable** [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002610 PVC Port VLAN Control of P6 000000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PVID	FORCE_PVID	REV0	PT_VPM	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	BC_LKYV_EN	MC_LKYV_EN	UC_LKYV_EN	ACC_FRM	
Type	RW	RW	DC	RW	RW	RW			RW		RW	RW	RW	RW	RW	

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Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	**Stack Tag VPID (VLAN Protocol ID) Value** The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	**PVID Disable** Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	**Force PVID on VLAN-tagged frames** 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID .
13	REV0	
12	PT_VPM	**Pass-through capability on TPID** 0: Disable pass-through on TPID 1: Enable pass-through on TPID
11	PT_OPTION	**Pass-through capability on TX special tag** 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	**Incoming Port Egress VLAN Tag Attribution** 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	**VLAN Port Attribute** 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	**Special Tag Enable** Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	BC_LKYV_EN	**Broadcast Leaky VLAN Enable** 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
3	MC_LKYV_EN	**Multicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	**Unicast Leaky VLAN Enable** [NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.) 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	**Acceptable Frame Type** 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

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00002614 PPBV1 Port-and-Protocol Based VLAN I of P6 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	**Group 1 Port Priority (optional)** The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G1_PORT_VID	**Group 1 Port VLAN ID (optional)** The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	**Group 0 Port Priority (Default Port Priority)** The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G0_PORT_VID	**Group 0 Port VLAN ID (Default Port VID)** The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002618 PPBV2 Port-and-Protocol Based VLAN II of P6 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G3_PORT_PRI			REV0	G3_PORT_VID											
Type	DC			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			DC	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G3_PORT_PRI	**Group 3 Port Priority (optional)** The Group 3 Priority for each port according to IEEE 802.1Q definition
28	REV0	**Reserved**
27:16	G3_PORT_VID	**Group 3 Port VLAN ID (optional)** The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	**Group 2 Port Priority (optional)** The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	**Reserved**
11:0	G2_PORT_VID	**Group 2 Port VLAN ID (optional)** The Group 2 VID for each port according to IEEE 802.1Q definition

0000261C BSR Broadcast Storm Rate Control of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MOD	STRM_BC_I	STRM_MC_I	STRM_UC_I	STRM_DRO	STRM_PER	STRM_UNIT		STORM_1G							

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	E	NC	NC	NC	P	D										
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	**Broadcast Storm Suppression** 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	**Broadcast Storm Included** 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	**Unknown Multicast Storm Included** 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	**Unknown Unicast Storm Included** 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	**Broadcast Storm Suppression enabled** 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	**Broadcast Strom Detection Signal Period** 0: One second 1: 125us
25:24	STRM_UNIT	**Broadcast Storm Suppression** 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	**1000 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	**100 Mbps Broadcast Storm Rate Limit Control** The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bp
7:0	STORM_10M	**10 MbpsBroadcast Storm Rate Limit Control** The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002620 STAG01 STAG Index 0/1 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1[3:0]				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:24	REV0	**Reserved**
23:12	VID1	**VLAN Identifier for STAG index 1**
11:0	VID0	**VLAN Identifier for STAG index 0**

00002624 STAG23 STAG Index 2/3 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3[3:0]				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID3	**VLAN Identifier for STAG index 3**
11:0	VID2	**VLAN Identifier for STAG index 2**

00002628 STAG45 STAG Index 4/5 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5[3:0]				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID5	**VLAN Identifier for STAG index 5**
11:0	VID4	**VLAN Identifier for STAG index 4**

0000262C STAG67 STAG Index 6/7 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7[11:4]							
Type	DC								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7[3:0]				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	**Reserved**
23:12	VID7	**VLAN Identifier for STAG index 7**

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11:0	VID6	**VLAN Identifier for STAG index 6**

00003000 PMCR_P0 PORT 0 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P0		EXT_PHY_P0	MAC_MODE_P0
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P0	MAC_TX_EN_P0	MAC_RX_EN_P0		MAC_PRE_P0	SFD_DET_MODE	BKOFF_EN_P0	BACKPR_EN_P0	FORCE_EEE1G_P0	FORCE_EEE100_P0	FORCE_RX_FC_P0	FORCE_TX_FC_P0	FORCE_SPD_P0		FORCE_DPX_P0	FORCE_LNK_P0
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0	0	1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P0	**PORT 0 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P0	**PORT 0 External PHY. Port 0 connects with external PHY.** 0: PORT 0 DOES NOT connect with external PHY 1: PORT 0 connects with external PHY
16	MAC_MODE_P0	**PORT 0 MAC Mode. PORT 0 operates in MAC mode** 0: PORT 0 operates in PHY mode. 1: PORT 0 operates in MAC mode.
15	FORCE_MODE_P0	**PORT 0 Force Mode. PORT 0 operates in force mode. It is used to control PORT 0 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g.** 0: Force mode is off.(Mac status is determined by phy auto-polling module) 1: Force mode is on. (Mac status is determined by force_xxx_P0 register)
14	MAC_TX_EN_P0	**Port 0 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P0	**PORT 0 RX MAC Enable. (Note: This bit only has impact on MAC function, it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P0	**TX short preamble mode** 0: TX short preamble length is disabled 1: TX short preamble is enabled.
10	SFD_DET_MODE	0: SFD is detected after RX buffer is ready. 1: SFD is detected whether RX buffer is ready or not.
9	BKOFF_EN_P0	**PORT 0 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 0 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P0	**PORT 0 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P0	**PORT 0 Force LPI Mode For 1000Mbps. When (force_mode_P0 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 0.** 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P0	**PORT 0 Force LPI Mode For 100Mbps. When (force_mode_P0 = 1), this bit is used**

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		to control the 100Base-TX EEE ability of PORT 0. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P0	**PORT 0 Force RX FC. When (force_mode_P0 = 1), this bit is used to control the RX FC ability of PORT 0.** 0: Disabled 1: Let the MAC of PORT 0 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P0	**PORT 0 Force TX FC. When (force_mode_P0 = 1), this bit is used to control the TX FC ability of PORT 0.** 0: Disabled 1: Let the MAC of PORT 0 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P0	**PORT 0 Force Speed [1:0]. When (force_mode_P0 = 1), these bits are used to control MAC speed of PORT 0.** 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P0	**PORT 0 Force duplex. When (force_mode_P0 = 1), this bit is used to control MAC duplex of PORT 0.** 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P0	**PORT 0 Force MAC Link Up. When (force_mode_P0 = 1), this bit is used to control link status of PORT 0.** 0: Link Down 1: Link Up

00003004 PMEEECR_P0 PORT 0 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P0								WAKEUP_TIME_100_P0							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P0															LPI_MODE_EN_P0
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P0	**PORT 0 Wake Up Time for 1000Mbps LPI Mode.** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P0	**PORT 0 Wake Up Time for 100Mbps LPI Mode.** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P0	**PORT 0 LPI Threshold.** When there is no packet to be transmitted, and the idle time is greater than P0_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P0	**PORT 0 Enter LPI Mode.** When there is no packet to be transmitted, and the idle time is greater than P0_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P0_LPI_THRESHOLD.

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1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003008 PMSR_P0 PORT 0 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P0	EEE100_STS_P0	RX_FC_STS_P0	TX_FC_STS_P0	MAC_SPD_STS_P0		MAC_DPX_STS_P0	MAC_LNK_STS_P0
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P0	**PORT 0 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P0	**PORT 0 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P0	**PORT 0 RX XFC Status. Port 0 Rx flow control status.** 0: Disabled 1: Let the MAC of PORT 0 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P0	**PORT 0 TX XFC Status. PORT 0 TX flow control status.** 0: Disabled 1: Let the MAC of PORT 0 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P0	**PORT 0 Speed [1:0] Status. Current speed of PORT 0 after PHY links up.** 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P0	**PORT 0 duplex Status. Current duplex mode of PORT 0 after PHY links up.** 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P0	**Port 6 Link Up Status. Link up status of PORT 0.** 0: Link Down 1: Link Up

00003010 PINT_EN_P0 PORT 0 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

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Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable** 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

00003014 PINT_STS_P0 PORT 0 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False

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		1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True
10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt** 0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True
0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003018 DBG_CNT PORT 0 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			
Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable of DA / SA comparison mode** 0: Disable 1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**
19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is**

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		increased.
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.**
2:0	RX_FIFO_OV	**Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.**

000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LPDET_EN6	LPDET_EN5	LPDET_EN4	LPDET_EN3	LPDET_EN2	LPDET_EN1	LPDET_EN0	LPDET_PERIOD_EN	LPDET_ALARM_EN	LPDET_PASS	LPDET_PERIOD	LPDET_LED_RATE	LPDET_THRESHOLD		
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_ST_LOOP	LPDET_ST_BCST	LPDET_TRAP_EN							LPDET_ALARM6	LPDET_ALARM5	LPDET_ALARM4	LPDET_ALARM3	LPDET_ALARM2	LPDET_ALARM1	LPDET_ALARM0
Type	RO	RO	RO							RO	RO	RO	RO	RO	RO	W1C
Reset	0	0	0							0	0	0	0	0	0	0

Bit(s)	Name	Description
30	LPDET_EN6	**Enable the loop detection ability of user port 6.** 0: Disable 1: Enable
29	LPDET_EN5	**Enable loop detection the ability of user port 5.** 0: Disable 1: Enable
28	LPDET_EN4	**Enable loop detection the ability of user port 4.** 0: Disable 1: Enable
27	LPDET_EN3	**Enable loop detection the ability of user port 3.** 0: Disable 1: Enable
26	LPDET_EN2	**Enable loop detection the ability of user port 2.** 0: Disable 1: Enable
25	LPDET_EN1	**Enable loop detection the ability of user port 1.** 0: Disable 1: Enable
24	LPDET_EN0	**Enable loop detection the ability of user port 0.** 0: Disable 1: Enable
23	LPDET_PERIOD_EN	**The loop detection frame is triggered by a periodical timer or by broadcast storm.** 0: Broadcast mode 1: Periodical mode
22	LPDET_ALARM_EN	**Enable 2 kHz alarm output and per-port LED when loop is detected.** 0: Disable 1: Enable
21	LPDET_PASS	**Loop detection frame is blocked or passed to packet memory.** 0: Blocked 1: Pass
20	LPDET_PERIOD	**Interval of transmitting loop detection frame in Periodical mode.** 0: 125 us

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		1: 1000 ms
19	LPDET_LED_RATE	**LED blinking rate of per port when loop is detected.** 0: LED blinking at 2 Hz 1: LED blinking at 4 Hz
18:16	LPDET_THRESHOLD	**Number of missed loop detection frame before 2 kHz alarm is reset**
15	LPDET_ST_LOOP	**The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.** 0: Not in Loop state 1: Loop state
14	LPDET_ST_BCST	**The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.** 0: Not in BCST state 1: BCST state
13	LPDET_TRAP_EN	**Status of strap pin for loop detection** 0: Disabled 1: Enabled
6	LPDET_ALARM6	**The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
5	LPDET_ALARM5	**The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
4	LPDET_ALARM4	**The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
3	LPDET_ALARM3	**The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
2	LPDET_ALARM2	**The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
1	LPDET_ALARM1	**The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.** 0: Not detected 1: Detected
0	LPDET_ALARM0	**The status of loop detected on port 0. This bit is cleared when it is written as 1.** 0: Not detected 1: Detected

000030C8 LPDET_SA_MSB LOOP DETECTION SA MSB 88740180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LPDET_TYPE															
Type	RW															
Reset	1	0	0	0	1	0	0	0	0	1	1	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_SA_MSB															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:16	LPDET_TYPE	**Loop detection frame type**
15:0	LPDET_SA_MSB	**Bits [47:32] of loop detection frame SA**

000030CC LPDET_SA_LSBLOOP DETECTION SA LSB C2000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LPDET_SA_LSB[31:16]															
Type	RW															
Reset	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_SA_LSB[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	LPDET_SA_LSB	**Bits [31:00] of loop detection frame SA**

000030D0 LPDET_RXSA_MSB LOOP DETECTION RX SA MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LPDET_RXPORT				LPDET_SRCPORT			
Type									RO				RO			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23:20	LPDET_RXPORT	**This is the 4-bit port number from which the loop detection frame was received.**
19:16	LPDET_SRCPORT	**This is the 4-bit source port number in the received loop detection frame.**

000030E0 GMACCR Global MAC Control Register 00003F25

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TXCRC_EN	RXCRC_EN	PRMBL_LMT_EN	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MTCC_LMT							MAX_RX_JUMBO				MAX_RX_PKT_LEN	
Type				RW							RW				RW	
Reset				1	1	1	1				1	0	0	1	0	1

Bit(s)	Name	Description
19	TXCRC_EN	**TX CRC Enable** 0: TX CRC insertion is enabled. 1: TX CRC insertion is disabled.
18	RXCRC_EN	**RX CRC Enable**

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		0: RX CRC removal is enabled. 1: RX CRC removal is disabled.
17	PRMBL_LMT_EN	**Preamble Limit Enable** 0: RXMAC can recognize SFD anytime. 1: RXMAC will recognize SFD within 7 Preamble bits, if SFD (0xd5) shows up after 7 bits preamble; RXMAC will not recognize it and treat it as no SFD case.
12:9	MTCC_LMT	**MTCC Limit.** Maximum transmitted collision count limitation 0: Disable TX collision abort function, send packet until the packet is sent successfully. 15: Maximum transmitted collision count is up to 15.
5:2	MAX_RX_JUMBO	**Maximum length of ingress jumbo frames** 0: Reserved. 1: Reserved. 2: 2K Bytes. 3: 3K Bytes. 4: 4K Bytes. 5: 5K Bytes. 6: 6K Bytes. 7: 7K Bytes. 8: 8K Bytes. 9: 9K Bytes. 10: 10K Bytes. 11: 11K Bytes. 12: 12K Bytes. 13: 13K Bytes. 14: 14K Bytes. 15: 15K Bytes.
1:0	MAX_RX_PKT_LEN	**Max Receive Packet Length.** Maximum length of ingress packet including CRC which can be received by MAC 0: 1518 bytes for untagged frames; 1522 bytes for tagged frames. 1: 1536bytes 2: 1552 bytes 3: MAX_RX_JUMBO

000030E4 SMACCR0 System MAC Control Register 0 0017A501

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SMACCR0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR0[15:0]															
Type	RW															
Reset	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	SMACCR0	**System MAC Address, sys_mac [31:0]. The first 32-bit of system MAC address. It is unique and is specified for pause frame.**

000030E8 SMACCR1 System MAC Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	SMACCR1	**System MAC Address, sys_mac [47:32]. The second 16-bit of system MAC address. It is unique and is specified for pause frame.**

000030F0 CKGCR Clock Gating Control Register 00001E33

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_TXIDLE_THD										CKG_TXIDLE	CKG_RXLPI			CKG_LNKDN_PORT	CKG_LNKDN_GLB
Type	RW										RW	RW			RW	RW
Reset	0	0	0	1	1	1	1	0			1	1			1	1

Bit(s)	Name	Description
15:8	LPI_TXIDLE_THD	**When there is no packet to be transmitted, and the idle time is greater than LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.** Default: 30ms (unit: 1ms)
5	CKG_TXIDLE	0: Keep the TX port clock ticking. 1: Stop the TX port clock ticking when the corresponding port has no traffic to send, and the idle time is greater than <LPI_TXIDLE_THD> ms.
4	CKG_RXLPI	0: Keep RX port clock ticking. 1: Stop the RX port clock ticking when the corresponding port enters the LPI mode, and the RX FIFO is empty.
1	CKG_LNKDN_PORT	**Port clock gating: Clock of gmac, port_ctrl, sch** 0: Keep the RX and TX port clock ticking. 1: Stop both RX and TX port clock ticking when the corresponding port enters the link-down status for 2 seconds.
0	CKG_LNKDN_GLB	**Global clock gating: Clock of bmu, pb_ctrl, arl** 0: Keep the global clock ticking. 1: Stop the global clock ticking when port0~port5 enter the link-down status for 2 seconds.

000030F4 GPINT_EN Global Port Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LPDET_INT_EN		PC6_INT_EN	PC5_INT_EN	PC4_INT_EN	PC3_INT_EN	PC2_INT_EN	PC1_INT_EN	PC0_INT_EN
Type								RW		RW	RW	RW	RW	RW	RW	RW
Reset								0		0	0	0	0	0	0	0

Bit(s)	Name	Description
8	LPDET_INT_EN	**Enable interrupt when the loop is detected.** 0: Disable

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		1: Enable
6	PC6_INT_EN	**Port Controller 6 Interrupt Enable** 0: Disable 1: Enable
5	PC5_INT_EN	**Port Controller 5 Interrupt Enable** 0: Disable 1: Enable
4	PC4_INT_EN	**Port Controller 4 Interrupt Enable** 0: Disable 1: Enable
3	PC3_INT_EN	**Port Controller 3 Interrupt Enable** 0: Disable 1: Enable
2	PC2_INT_EN	**Port Controller 2 Interrupt Enable** 0: Disable 1: Enable
1	PC1_INT_EN	**Port Controller 1 Interrupt Enable** 0: Disable 1: Enable
0	PC0_INT_EN	**Port Controller 0 Interrupt Enable** 0: Disable 1: Enable

000030F8 GPINT_STS Global Port Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								LPDET_INT		PC6_INT	PC5_INT	PC4_INT	PC3_INT	PC2_INT	PC1_INT	PC0_INT
Type								W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset								0		0	0	0	0	0	0	0

Bit(s)	Name	Description
8	LPDET_INT	**Loop detection interrupt status. This bit is cleared when it is written as 1.** 0: False 1: True
6	PC6_INT	**Port Controller 6 Interrupt. This bit is cleared when it is written as 1.** 0: False 1: True
5	PC5_INT	**Port Controller 5 Interrupt. This bit is cleared when it is written as 1.** 0: False 1: True
4	PC4_INT	**Port Controller 4 Interrupt. This bit is cleared when it is written as 1.** 0: False 1: True
3	PC3_INT	**Port Controller 3 Interrupt. This bit is cleared when it is written as 1.** 0: False 1: True
2	PC2_INT	**Port Controller 2 Interrupt. This bit is cleared when it is written as 1.** 0: False 1: True
1	PC1_INT	**Port Controller 1 Interrupt. This bit is cleared when it is written as 1.** 0: False

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		1: True
0	PC0_INT	**Port Controller 0 Interrupt. This bit is cleared when it is written as 1.** 0: False 1: True

00003100 PMCR_P1 PORT 1 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P1		EXT_PHY_P1	MAC_MODE_P1
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P1	MAC_TX_EN_P1	MAC_RX_EN_P1		MAC_PRE_P1		BKOFF_EN_P1	BACKPR_EN_P1	FORCE_EEE1G_P1	FORCE_EEE100_P1	FORCE_RX_FC_P1	FORCE_TX_FC_P1	FORCE_SPD_P1		FORCE_DPX_P1	FORCE_LNK_P1
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P1	**PORT 1 Inter-Frame+ Gap Shrink.** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P1	**PORT 1 External PHY. Port 1 connects with external PHY.** 0: PORT 1 DOES NOT connect with external PHY 1: PORT 1 connects with external PHY
16	MAC_MODE_P1	**PORT 1 MAC Mode. PORT 1 operates in MAC mode** 0: PORT 1 operates in PHY mode 1: PORT 1 operates in MAC mode
15	FORCE_MODE_P1	**PORT 1 Force Mode. PORT 1 operates in force mode. It is used to control PORT 1 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g.** 0: Force mode is off (The mac status is determined by phy auto-polling module). 1: Force mode is on (The mac status is determined by force_xxx_P1 register).
14	MAC_TX_EN_P1	**Port 1 TX MAC Enable (Note: This bit only has impacts on the MAC function, it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P1	**PORT 1 RX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P1	**TX short preamble mode** 0: The TX short preamble length is disabled. 1: The TX short preamble is enabled.
9	BKOFF_EN_P1	**PORT 1 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 1 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P1	**PORT 1 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P1	**PORT 1 Force LPI Mode For 1000Mbps. When (force_mode_P1 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 1.** 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.

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6	FORCE_EEE100_P1	**PORT 1 Force LPI Mode For 100Mbps. When (force_mode_P1 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 1.** 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P1	**PORT 1 Force RX FC. When (force_mode_P1 = 1), this bit is used to control the RX FC ability of PORT 1.** 0: Disabled 1: Let the MAC of PORT 1 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P1	**PORT 1 Force TX FC. When (force_mode_P1 = 1), this bit is used to control the TX FC ability of PORT 1.** 0: Disabled 1: Let the MAC of PORT 1 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P1	**PORT 1 Force Speed [1:0]. When (force_mode_P1 = 1), these bits are used to control MAC speed of PORT 1.** 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: reserved
1	FORCE_DPX_P1	**PORT 1 Force duplex. When (force_mode_P1 = 1), this bit is used to control MAC duplex of PORT 1.** 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P1	**PORT 1 Force MAC Link Up. When (force_mode_P1 = 1), this bit is used to control link status of PORT 1.** 0: Link Down 1: Link Up

00003104 PMEEECR_P1 PORT 1 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P1								WAKEUP_TIME_100_P1							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P1															LPI_MODE_EN_P1
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P1	**PORT 1 Wake Up Time for 1000Mbps LPI Mode.** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P1	**PORT 1 Wake Up Time for 100Mbps LPI Mode.** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P1	**PORT 1 LPI Threshold.** When there is no packet to be transmittedm, and the idle time is greater than P1_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P1	**PORT 1 Enter LPI Mode.** When there is no packet to be transmitted, and the idle time is greater than P1_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.

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0: LPI mode depends on the P1_LPI_THRESHOLD.
1: Let the system enter the LPI mode immediately and send EEE LPI frame to the link partner.

00003108 PMSR_P1 PORT 1 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P1	EEE100_STS_P1	RX_FC_STS_P1	TX_FC_STS_P1	MAC_SPD_STS_P1		MAC_DPX_STS_P1	MAC_LNK_STS_P1
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P1	**PORT 1 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P1	**PORT 1 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P1	**PORT 1 RX XFC Status. Port 1 Rx flow control status.** 0: Disabled 1: Let the MAC of PORT 1 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P1	**PORT 1 TX XFC Status. PORT 1 TX flow control status.** 0: Disabled 1: Let the MAC of PORT 1 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P1	**PORT 1 Speed [1:0] Status. Current speed of PORT 1 after PHY links up.** 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P1	**PORT 1 duplex Status. Current duplex mode of PORT 1 after PHY links up.** 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P1	**Port 1 Link Up Status. Link up status of PORT 1.** 0: Link Down 1: Link Up

00003110 PINT_EN_P1 PORT 1 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW

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Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable** 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

00003114 PINT_STS_P1 PORT 1 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description

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15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False 1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True
10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt** 0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True
0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003118 DBG_CNT PORT 1 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			
Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable DA / SA comparison mode.** 0: Disable 1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**

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19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is increased.**
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.**
2:0	RX_FIFO_OV	**Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.**

00003200 PMCR_P2 PORT 2 MAC Control Register 00056130

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P2		EXT_PHY_P2	MAC_MODE_P2
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P2	MAC_TX_EN_P2	MAC_RX_EN_P2		MAC_PRE_P2			BACKPR_EN_P2	FORCE_EEE1G_P2	FORCE_EEE100_P2	FORCE_RX_FC_P2	FORCE_TX_FC_P2	FORCE_SPD_P2		FORCE_DPX_P2	FORCE_LNK_P2
Type	RW	RW	RW		RW			RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0			1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P2	**PORT 2 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P2	**PORT 2 External PHY. Port 2 connects with external PHY.** 0: PORT 2 DOES NOT connect with external PHY 1: PORT 2 connects with external PHY
16	MAC_MODE_P2	**PORT 2 MAC Mode. PORT 2 operates in MAC mode** 0: PORT 2 operates in PHY mode 1: PORT 2 operates in MAC mode
15	FORCE_MODE_P2	**PORT 2 Force Mode. PORT 2 operates in force mode. It is used to control PORT 2 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g.** 0: Force mode is off (mac status is determined by phy auto-polling module). 1: Force mode is on (mac status is determined by force_xxx_P2 register).
14	MAC_TX_EN_P2	**Port 2 TX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P2	**PORT 2 RX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P2	**TX short preamble mode** 0: TX short preamble length is disabled 1: TX short preamble is enabled.
8	BACKPR_EN_P2	**PORT 2 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P2	**PORT 2 Force LPI Mode For 1000Mbps. When (force_mode_pn = 1), this bit is used to control the 1000Base-T EEE ability of PORT 2.** 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps.

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		1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P2	**PORT 2 Force LPI Mode For 100Mbps. When (force_mode_pn = 1), this bit is used to control the 100Base-TX EEE ability of PORT 2.** 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P2	**PORT 2 Force RX FC. When (force_mode_P2 = 1), this bit is used to control the RX FC ability of PORT 2.** 0: Disabled. 1: Let the MAC of PORT 2 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P2	**PORT 2 Force TX FC. When (force_mode_P2 = 1), this bit is used to control the TX FC ability of PORT 2.** 0: Disabled. 1: Let the MAC of PORT 2 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P2	**PORT 2 Force Speed [1:0]. When (force_mode_P2 = 1), these bits are used to control MAC speed of PORT 2.** 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P2	**PORT 2 Force duplex. When (force_mode_P2 = 1), this bit is used to control the MAC duplex of PORT 2.** 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P2	**PORT 2 Force MAC Link Up. When (force_mode_P2 = 1), this bit is used to control the link status of PORT 2.** 0: Link Down 1: Link Up

00003204 PMEEECR_P2 PORT 2 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P2								WAKEUP_TIME_100_P2							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P2															LPI_MODE_EN_P2
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P2	**PORT 2 Wake Up Time for 1000Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P2	**PORT 2 Wake Up Time for 100Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P2	**PORT 2 LPI Threshold.** When there is no packet to be transmitted, and the idle time is greater than P2_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P2	**PORT 2 Enter LPI Mode.** When there is no packet to be transmitted, and the idle time is greater than P2_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode

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and send EEE LPI frame to the link partner.
0: LPI mode depends on the P2_LPI_THRESHOLD.
1: Let the system enter the LPI mode immediately and send EEE LPI frame to the link partner.

00003208 PMSR_P2 PORT 2 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P2	EEE100_STS_P2	RX_FC_STS_P2	TX_FC_STS_P2	MAC_SPD_STS_P2		MAC_DPX_STS_P2	MAC_LNK_STS_P2
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P2	**PORT 2 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P2	**PORT 2 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P2	**PORT 2 RX XFC Status. Port 2 Rx flow control status** 0: Disabled. 1: Let the MAC of PORT 2 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P2	**PORT 2 TX XFC Status** PORT 2 TX flow control status 0: Disabled. 1: Let the MAC of PORT 2 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P2	**PORT 2 Speed [1:0] Status** Current speed of PORT 2 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P2	**PORT 2 duplex Status** Current duplex mode of PORT 2 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P2	**Port 2 Link Up Status** Link up status of PORT 2 0: Link Down 1: Link Up

00003210 PINT_EN_P2 PORT 2 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TF	TX_MI	TX_MI	TX_RP	TX_RP	TX_G	TX_R	TX_D					RX_A	RX_A	RX_W	RX_G

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	F_UNDR_INT_EN	SVLAN_ERR_INT_EN	SPAGE_ERR_INT_EN	AGE_ERR_INT_EN	AGE_TOUT_INT_EN	PAGE_TOUT_INT_EN	DPB_TOUT_INT_EN	EQ_TOUT_INT_EN					FF_FULL_INT_EN	RL_TOUT_INT_EN	RPB_TOUT_INT_EN	PAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable** 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

00003214 PINT_STS_P2 PORT 2 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO

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Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False 1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True
10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt** 0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True
0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003218 DBG_CNT PORT 2 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			
Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable DA / SA comparison mode** 0: Disable

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		1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**
19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is increased.**
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.**
2:0	RX_FIFO_OV	**Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.**

00003300 PMCR_P3 PORT 3 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P3		EXT_PHY_P3	MAC_MODE_P3
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P3	MAC_TX_EN_P3	MAC_RX_EN_P3		MAC_PRE_P3		BKOFF_EN_P3	BACKPR_EN_P3	FORCE_EEE1G_P3	FORCE_EEE100_P3	FORCE_RX_FC_P3	FORCE_TX_FC_P3	FORCE_SPD_P3		FORCE_DPX_P3	FORCE_LNK_P3
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P3	**PORT 3 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P3	**PORT 3 External PHY** Port 3 connects with external PHY. 0: PORT 3 DOES NOT connect with external PHY 1: PORT 3 connects with external PHY
16	MAC_MODE_P3	**PORT 3 MAC Mode** PORT 3 operates in MAC mode. 0: PORT 3 operates in PHY mode 1: PORT 3 operates in MAC mode
15	FORCE_MODE_P3	**PORT 3 Force Mode** PORT 3 operates in force mode. It is used to control PORT 3 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g. 0: Force mode is off (mac status is determined by phy auto-polling module). 1: Force mode is on (mac status is determined by force_xxx_P3 register).
14	MAC_TX_EN_P3	**Port 3 TX MAC Enable (Note: This bit only has impact on MAC function, it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P3	**PORT 3 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P3	**TX short preamble mode** 0: TX short preamble length is disabled 1: TX short preamble is enabled.
9	BKOFF_EN_P3	**PORT 3 Backoff Enable**

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		0: Disabled 1: Let the MAC of PORT 3 to follow the back-off mechanism when collision happens.
8	BACKPR_EN_P3	**PORT 3 Backpressure Enable** 0: Disabled 1: Enable the back pressure mechanism when operating in half-duplex mode with low internal free memory page count .
7	FORCE_EEE1G_P3	**PORT 3 Force LPI Mode For 1000Mbps** When (force_mode_P3 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 3. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P3	**PORT 3 Force LPI Mode For 100Mbps** When (force_mode_P3 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 3. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P3	**PORT 3 Force RX FC** When (force_mode_P3 = 1), this bit is used to control the RX FC ability of PORT 3. 0: Disabled. 1: Let the MAC of PORT 3 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P3	**PORT 3 Force TX FC** When (force_mode_P3 = 1), this bit is used to control the TX FC ability of PORT 3. 0: Disabled. 1: Let the MAC of PORT 3 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P3	**PORT 3 Force Speed [1:0]** When (force_mode_P3 = 1), these bits are used to control the MAC speed of PORT 3. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P3	**PORT 3 Force duplex.** When (force_mode_P3 = 1), this bit is used to control the MAC duplex of PORT 3. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P3	**PORT 3 Force MAC Link Up** When (force_mode_P3 = 1), this bit is used to control the link status of PORT 3. 0: Link Down 1: Link Up

00003304 PMEEECR_P3 PORT 3 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P3								WAKEUP_TIME_100_P3							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P3															LPI_MODE_EN_P3
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P3	**PORT 3 Wake Up Time for 1000Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second

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23:16	WAKEUP_TIME_100_P3	**PORT 3 Wake Up Time for 100Mbps LPI Mode.** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P3	**PORT 3 LPI Threshold** When there is no packet to be transmitted, and the idle time is greater than P3_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P3	**PORT 3 Enter LPI Mode.** When there is no packet to be transmitted, and the idle time is greater than P3_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P3_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003308 PMSR_P3 PORT 3 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P3	EEE100_STS_P3	RX_FC_STS_P3	TX_FC_STS_P3	MAC_SPD_STS_P3		MAC_DPX_STS_P3	MAC_LNK_STS_P3
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P3	**PORT 3 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P3	**PORT 3 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P3	**PORT 3 RX XFC Status** Port 3 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 3 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P3	**PORT 3 TX XFC Status** PORT 3 TX flow control status 0: Disabled. 1: Let the MAC of PORT 3 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P3	**PORT 3 Speed [1:0] Status** Current speed of PORT 3 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P3	**PORT 3 duplex Status** Current duplex mode of port 3 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P3	**Port 3 Link Up Status** Link up status of PORT 3 0: Link Down

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1: Link Up

00003310 PINT_EN_P3 PORT 3 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable** 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

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00003314 PINT_STS_P3 PORT 3 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False 1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True
10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt** 0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True
0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003318 DBG_CNT PORT 3 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			

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Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable DA / SA comparison mode.** 0: Disable 1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**
19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is increased.**
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo** The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	**Overflow count of RX fifo** The field is increased when RX fifo overflow occurs.

00003400 PMCR_P4 PORT 4 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P4		EXT_PHY_P4	MAC_MODE_P4
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P4	MAC_TX_EN_P4	MAC_RX_EN_P4		MAC_PRE_P4		BKOFF_EN_P4	BACKPR_EN_P4	FORCE_EEE1G_P4	FORCE_EEE100_P4	FORCE_RX_FC_P4	FORCE_TX_FC_P4	FORCE_SPD_P4		FORCE_DPX_P4	FORCE_LNK_P4
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P4	**PORT 4 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: shrink 64-bits IFG
17	EXT_PHY_P4	**PORT 4 External PHY** Port 4 connects with external PHY. 0: PORT 4 DOES NOT connect with external PHY 1: PORT 4 connects with external PHY
16	MAC_MODE_P4	**PORT 4 MAC Mode** PORT 4 operates in MAC mode. 0: PORT 4 operates in PHY mode 1: PORT 4 operates in MAC mode
15	FORCE_MODE_P4	**PORT 4 Force Mode** PORT 4 operates in force mode. It is used to control PORT 4 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g. 0: Force mode is off (mac status is determined by phy auto-polling module).

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		1: Force mode is on (mac status is determined by force_xxx_P4 register).
14	MAC_TX_EN_P4	**Port 4 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P4	**PORT 4 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P4	**TX short preamble mode** 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P4	**PORT 4 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 4 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P4	**PORT 4 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P4	**PORT 4 Force LPI Mode For 1000Mbps. When (force_mode_P4 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 4.** 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P4	**PORT 4 Force LPI Mode For 100Mbps. When (force_mode_P4 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 4.** 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P4	**PORT 4 Force RX FC** When (force_mode_P4 = 1), this bit is used to control the RX FC ability of PORT 4. 0: Disabled. 1: Let the MAC of PORT 4 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P4	**PORT 4 Force TX FC** When (force_mode_P4 = 1), this bit is used to control the TX FC ability of PORT 4. 0: Disabled. 1: Let the MAC of PORT 4 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P4	**PORT 4 Force Speed [1:0]** When (force_mode_P4 = 1), these bits are used to control MAC speed of PORT 4. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P4	**PORT 4 Force duplex** When (force_mode_P4 = 1), this bit is used to control MAC duplex of PORT 4. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P4	**PORT 4 Force MAC Link Up** When (force_mode_P4 = 1), this bit is used to control link status of PORT 4. 0: Link Down 1: Link Up

00003404 PMEEECR_P4 PORT 4 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P4								WAKEUP_TIME_100_P4							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P4															LPI_M

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																ODE_EN_P4
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P4	**PORT 4 Wake Up Time for 1000Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P4	**PORT 4 Wake Up Time for 100Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P4	**PORT 4 LPI Threshold** When there is no packet to be transmitted, and the idle time is greater than P4_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P4	**PORT 4 Enter LPI Mode.** When there is no packet to be transmitted, and the idle time is greater than P4_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P4_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003408 PMSR_P4 PORT 4 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P4	EEE100_STS_P4	RX_FC_STS_P4	TX_FC_STS_P4	MAC_SPD_STS_P4		MAC_DPX_STS_P4	MAC_LNK_STS_P4
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P4	**PORT 4 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P4	**PORT 4 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P4	**PORT 4 RX XFC Status** Port 4 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 4 accept a pause frame when operating in full-duplex mode
4	TX_FC_STS_P4	**PORT 4 TX XFC Status** PORT 4 TX flow control status 0: Disabled. 1: Let the MAC of PORT 4 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P4	**PORT 4 Speed [1:0] Status**

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		Current speed of PORT 4 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P4	**PORT 4 duplex Status** Current duplex mode of PORT 4 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P4	**Port 4 Link Up Status** Link up status of PORT 4 0: Link Down 1: Link Up

00003410 PINT_EN_P4 PORT 4 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable**

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		0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

00003414 PINT_STS_P4 PORT 4 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False 1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True
10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt** 0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True

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0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003418 DBG_CNT PORT 4 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			
Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable DA / SA comparison mode.** 0: Disable 1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**
19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is increased.**
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo** The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	**Overflow count of RX fifo** The field is increased when RX fifo overflow occurs.

00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P5		EXT_PHY_P5	MAC_MODE_P5
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P5	MAC_TX_EN_P5	MAC_RX_EN_P5		MAC_PRE_P5		BKOFF_EN_P5	BACKPR_EN_P5	FORCE_EEE1G_P5	FORCE_EEE100_P5	FORCE_RX_FC_P5	FORCE_TX_FC_P5	FORCE_SPD_P5		FORCE_DPX_P5	FORCE_LNK_P5
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P5	**PORT 5 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P5	**PORT 5 External PHY**

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		Port 5 connects with external PHY. 0: PORT 5 DOES NOT connect with external PHY. 1: PORT 5 connects with external PHY.
16	MAC_MODE_P5	**PORT 5 MAC Mode** PORT 5 operates in MAC mode. 0: PORT 5 operates in PHY mode. 1: PORT 5 operates in MAC mode.
15	FORCE_MODE_P5	**PORT 5 Force Mode** PORT 5 operates in force mode. It is used to control PORT 5 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g. 0: Force mode is off (mac status is determined by phy auto-polling module). 1: Force mode is on (mac status is determined by force_xxx_P5 register).
14	MAC_TX_EN_P5	**Port 5 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P5	**PORT 5 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P5	**TX short preamble mode** 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P5	**PORT 5 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 5 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P5	**PORT 5 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P5	**PORT 5 Force LPI Mode For 1000Mbps** When (force_mode_P5 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps
6	FORCE_EEE100_P5	**PORT 5 Force LPI Mode For 100Mbps** When (force_mode_P5 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps
5	FORCE_RX_FC_P5	**PORT 5 Force RX FC** When (force_mode_P5 = 1), this bit is used to control the RX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P5	**PORT 5 Force TX FC** When (force_mode_P5 = 1), this bit is used to control the TX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P5	**PORT 5 Force Speed [1:0]** When (force_mode_P5 = 1), these bits are used to control MAC speed of PORT 5. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P5	**PORT 5 Force duplex** When (force_mode_P5 = 1), this bit is used to control MAC duplex of PORT 5. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P5	**PORT 5 Force MAC Link Up** When (force_mode_P5 = 1), this bit is used to control link status of PORT 5.

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0: Link Down
1: Link Up

00003504 PMEEECR_P5 PORT 5 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P5								WAKEUP_TIME_100_P5							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P5															LPI_MODE_EN_P5
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P5	**PORT 5 Wake Up Time for 1000Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P5	**PORT 5 Wake Up Time for 100Mbps LPI Mode.** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P5	**PORT 5 LPI Threshold.** When there is no packet to be transmitted, and the idle time is greater than P5_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P5	**PORT 5 Enter LPI Mode** When there is no packet to be transmitted, and the idle time is greater than P5_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P5_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5		MAC_DPX_STS_P5	MAC_LNK_STS_P5
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P5	**PORT 5 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P5	**PORT 5 LPI Status Mode For 100Mbps**

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		0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P5	**PORT 5 RX XFC Status. Port 5 Rx flow control status** 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P5	**PORT 5 TX XFC Status** PORT 5 TX flow control status 0: Disabled. 1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P5	**PORT 5 Speed [1:0] Status** Current speed of PORT 5 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P5	**PORT 5 duplex Status** Current duplex mode of port 5 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P5	**Port 5 Link Up Status. Link up status of PORT 5.** 0: Link Down 1: Link Up

00003510 PINT_EN_P5 PORT 5 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

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9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable** 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

00003514 PINT_STS_P5 PORT 5 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False 1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True
10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt**

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		0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True
0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003518 DBG_CNT PORT 5 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			
Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable DA / SA comparison mode.** 0: Disable 1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**
19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is increased.**
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.**
2:0	RX_FIFO_OV	**Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.**

00003600 PMCR_P6 PORT 6 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P6		EXT_PHY_P6	MAC_MODE_P6
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P6	MAC_TX_EN_P6	MAC_RX_EN_P6		MAC_PRE_P6		BKOFF_EN_P6	BACKPR_EN_P6	FORCE_EEE1G_P6	FORCE_EEE100_P6	FORCE_RX_FC_P6	FORCE_TX_FC_P6	FORCE_SPD_P6		FORCE_DPX_P6	FORCE_LNK_P6
Type	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW

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Reset	0	1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
19:18	IPG_CFG_P6	**PORT 6 Inter-Frame+ Gap Shrink** 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P6	**PORT 6 External PHY. Port 6 connects with external PHY.** 0: PORT 6 DOES NOT connect with external PHY. 1: PORT 6 connects with external PHY.
16	MAC_MODE_P6	**PORT 6 MAC Mode. PORT 6 operates in MAC mode** 0: PORT 6 operates in PHY mode. 1: PORT 6 operates in MAC mode.
15	FORCE_MODE_P6	**PORT 6 Force Mode. PORT 6 operates in force mode. It is used to control PORT 6 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g.** 0: Force mode is off (mac status is determined by phy auto-polling module). 1: Force mode is on (mac status is determined by force_xxx_P6 register).
14	MAC_TX_EN_P6	**Port 6 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P6	**PORT 6 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P6	**TX short preamble mode** 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P6	**PORT 6 Backoff Enable** 0: Disabled 1: Let the MAC of PORT 6 to follow the back-off mechanism when collision happens.
8	BACKPR_EN_P6	**PORT 6 Backpressure Enable** 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex with low internal free memory page count.
7	FORCE_EEE1G_P6	**PORT 6 Force LPI Mode For 1000Mbps** When (force_mode_P6 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 6. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P6	**PORT 6 Force LPI Mode For 100Mbps** When (force_mode_P6 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 6. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P6	**PORT 6 Force RX FC. When (force_mode_P6 = 1), this bit is used to control the RX FC ability of PORT 6.** 0: Disabled. 1: Let the MAC of PORT 6 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P6	**PORT 6 Force TX FC** When (force_mode_P6 = 1), this bit is used to control the TX FC ability of PORT 6. 0: Disabled. 1: Let the MAC of PORT 6 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P6	**PORT 6 Force Speed [1:0]** When (force_mode_P6 = 1), these bits are used to control MAC speed of PORT 6. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved

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1	FORCE_DPX_P6	**PORT 6 Force duplex** When (force_mode_P6 = 1), this bit is used to control MAC duplex of PORT 6. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P6	**PORT 6 Force MAC Link Up** When (force_mode_P6 = 1), this bit is used to control link status of PORT 6. 0: Link Down 1: Link Up

00003604 PMEEECR_P6 PORT 6 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P6								WAKEUP_TIME_100_P6							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P6															LPI_MODE_EN_P6
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P6	**PORT 6 Wake Up Time for 1000Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P6	**PORT 6 Wake Up Time for 100Mbps LPI Mode** The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P6	**PORT 6 LPI Threshold** When there is no packet to be transmitted, and the idle time is greater than P6_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P6	**PORT 6 Enter LPI Mode** When there is no packet to be transmitted, and the idle time is greater than P6_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P6_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003608 PMSR_P6 PORT 6 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P6	EEE100_STS_P6	RX_FC_STS_P6	TX_FC_STS_P6	MAC_SPD_STS_P6		MAC_DPX_STS_P6	MAC_LNK_STS_P6
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7	EEE1G_STS_P6	**PORT 6 LPI Mode Status For 1000Mbps** 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P6	**PORT 6 LPI Status Mode For 100Mbps** 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P6	**PORT 6 RX XFC Status** Port 6 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 6 accept a pause frame when operating in full-duplex mode
4	TX_FC_STS_P6	**PORT 6 TX XFC Status** PORT 6 TX flow control status 0: Disabled. 1: Let the MAC of PORT 6 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P6	**PORT 6 Speed [1:0] Status** Current speed of PORT 6 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P6	**PORT 6 duplex Status** Current duplex mode of PORT 6 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P6	**Port 6 Link Up Status** Link up status of PORT 6 0: Link Down 1: Link Up

00003610 PINT_EN_P6 PORT 6 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	**TXMAC TXFIFO Under run Interrupt Enable** 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	**TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable** 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	**TX_CTRL Release Page Count Error Interrupt Enable** 0: Disabled

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		1: Enabled
11	TX_RPAGE_TOUT_INT_EN	**TX_CTRL Release Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	**TX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	**TX_CTRL RD_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	**TX_CTRL DEQ Timeout Interrupt Enable** 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	**RX_CTRL Agent FIFO Full Interrupt Enable** 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	**RX_CTRL ARL Timeout Interrupt Enable** 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	**RX_CTRL WR_PB Timeout Interrupt Enable** 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	**RX_CTRL Get Page Timeout Interrupt Enable** 0: Disabled 1: Enabled

00003614 PINT_STS_P6 PORT 6 Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	**TXMAC TXFIFO Under run Interrupt** 0: False 1: True
14	TX_MISVLAN_ERR_INT	**TX_CTRL PKT INFO VLAN Mismatch Error Interrupt** 0: False 1: True
13	TX_MISPAGE_ERR_INT	**TX_CTRL PKT INFO Page Mismatch Error Interrupt** 0: False 1: True
12	TX_RPAGE_ERR_INT	**TX_CTRL Release Page Count Error Interrupt** 0: False 1: True
11	TX_RPAGE_TOUT_INT	**TX_CTRL Release Page Timeout Interrupt** 0: False 1: True

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10	TX_GPAGE_TOUT_INT	**TX_CTRL Get Page Timeout Interrupt** 0: False 1: True
9	TX_RDPB_TOUT_INT	**TX_CTRL RD_PB Timeout Interrupt** 0: False 1: True
8	TX_DEQ_TOUT_INT	**TX_CTRL DEQ Timeout Interrupt** 0: False 1: True
3	RX_AFF_FULL_INT	**RX_CTRL Agent FIFO Full Interrupt** 0: False 1: True
2	RX_ARL_TOUT_INT	**RX_CTRL ARL Timeout Interrupt** 0: False 1: True
1	RX_WRPB_TOUT_INT	**RX_CTRL WR_PB Timeout Interrupt** 0: False 1: True
0	RX_GPAGE_TOUT_INT	**RX_CTRL Get Page Timeout Interrupt** 0: False 1: True

00003618 DBG_CNT PORT 6 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CMP								DA_CMP				SA_CMP			
Type	RW								RW				RW			
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_ERR				SA_ERR				TX_FIFO_URUN					RX_FIFO_OV		
Type	RW				RW				RO					RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
31	MODE_CMP	**Enable DA / SA comparison mode.** 0: Disable 1: Enable
23:20	DA_CMP	**In DA / SA comparison mode, the received DA[3:0] is compared to this field. If DA[47:4] is not zero, or DA[3:0] is not identical to this field, the DA_ERR is increased.**
19:16	SA_CMP	**In DA / SA comparison mode, the received SA[3:0] is compared to this field. If SA[47:4] is not zero, or SA[3:0] is not identical to this field, the SA_ERR is increased.**
15:12	DA_ERR	**The error count after DA comparison**
11:8	SA_ERR	**The error count after SA comparison**
7:4	TX_FIFO_URUN	**Underrun count of TX fifo.** The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	**Overflow count of RX fifo** The field is increased when RX fifo overflow occurs.

00004000 TDPC_P0 TX Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event when the frame output should be dropped due to the late collision or excessive collision**

00004004 TCRC_P0 TX CRC Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004008 TUPC_P0 TX Unicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.**

0000400C TMPC_P0 TX Multicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004010 TBPC_P0 TX Broadcast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004014 TCEC_P0 TX Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurrence during frame transmission**

00004018 TSCEC_P0 TX Single Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

0000401C TMCEC_P0 TX Multiple Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004020 TDEC_P0 TX Deferred Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted**

00004024 TLCEC_P0 TX Late Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004028 TXCEC_P0 TX excessive Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16)**

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consecutive collisions or more, not including late collisions

0000402C TPPC_P0 TX Pause Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correct transmitted MAC flow-control frame

00004030 TL64PC_P0 TX packet Length in 64-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004034 TL65PC_P0 TX packet Length in 65-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004038 TL128PC_P0 TX packet Length in 128-byte slot Packet Counter of 00000000

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Port 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000403C TL256PC_P0 TX packet Length in 256-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

00004040 TL512PC_P0 TX packet Length in 512-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

00004044 TL1024PC_P0 TX packet Length in 1024-byte slot Packet Counter of Port 0 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

00004048 TOCL_P0 TX Octet Counter Low double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000404C TOCH_P0 TX Octet Counter High double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004060 RDPC_P0 RX Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004064 RFPC_P0 RX Filtering Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero.**

00004068 RUPC_P0 RX Unicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000406C RMPC_P0 RX Multicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004070 RBPC_P0 RX Broadcast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004074 RAEPC_P0 RX Alignment Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted.**

00004078 RCEPC_P0 RX CRC(FCS) Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted.**

0000407C RUSPC_P0 RX Undersize Packet Counter of Port 0 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long excluding framing bits, but including FCS octets which are otherwise well formed.**

00004080 RFEPC_P0 RX Fragment Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).**

00004084 ROSPC_P0 RX Oversize Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error.**

00004088 RJEPC_P0 RX Jabber Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).**

0000408C RPPC_P0 RX Pause Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame.**

00004090 RL64PC_P0 RX packet Length in 64-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004094 RL65PC_P0 RX packet Length in 65-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004098 RL128PC_P0 RX packet Length in 128-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000409C RL256PC_P0 RX packet Length in 256-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000040A0 RL512PC_P0 RX packet Length in 512-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

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000040A4 RL1024PC_P0 RX packet Length in 1024-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

000040A8 ROCL_P0 RX Octet Counter Low double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000040AC ROCH_P0 Rx Octet Counter High double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above)**

000040B0 RDPC_CTRL_P RX CTRL Drop Packet Counter of Port 0 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000040B4 RDPC_ING_P0 RX Ingress Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped according to the ingress rate limit set by the Ingress rate limiter**

000040B8 RDPC_ARL_P0 RX ARL Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000040D0 TMIB_HF_STS_P0 TX Port MIB Counter Half Full Status of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status** 0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True
2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status**

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		0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000040D4 RMIB_HF_STS_P0 RX Port MIB Counter Half Full Status of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status** 0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status**

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		0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False 1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

00004100 TDPC_P1 TX Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event when the frame output should be dropped due to the late collision or excessive collision**

00004104 TCRC_P1 TX CRC Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004108 TUPC_P1 TX Unicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission**

0000410C TMPC_P1 TX Multicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004110 TBPC_P1 TX Broadcast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004114 TCEC_P1 TX Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurred during frame transmission**

00004118 TSCEC_P1 TX Single Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

0000411C TMCEC_P1 TX Multiple Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004120 TDEC_P1 TX Deferred Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode** Frame involved in collision is not counted.

00004124 TLCEC_P1 TX Late Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004128 TXCEC_P1 TX excessive Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions**

0000412C TPPC_P1 TX Pause Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	**The number of correctly transmitted MAC flow-control frame**

00004130 TL64PC_P1 TX packet Length in 64-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	**It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004134 TL65PC_P1 TX packet Length in 65-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004138 TL128PC_P1 TX packet Length in 128-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

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0000413C TL256PC_P1 TX packet Length in 256-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

00004140 TL512PC_P1 TX packet Length in 512-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

00004144 TL1024PC_P1 TX packet Length in 1024-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

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00004148 TOCL_P1 TX Octet Counter Low double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000414C TOCH_P1 TX Octet Counter High double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004160 RDPC_P1 RX Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit

00004164 RFPC_P1 RX Filtering Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or when the port map is equal to zero**

00004168 RUPC_P1 RX Unicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000416C RMPC_P1 RX Multicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004170 RBPC_P1 RX Broadcast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004174 RAEPC_P1 RX Alignment Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted**

00004178 RCEPC_P1 RX CRC(FCS) Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted**

0000417C RUSPC_P1 RX Undersize Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long excluding framing bits, but including FCS octets which are otherwise well formed**

00004180 RFEPC_P1 RX Fragment Error Packet Counter of Port 1 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).**

00004184 ROSPC_P1 RX Oversize Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error**

00004188 RJEPC_P1 RX Jabber Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

0000418C RPPC_P1 RX Pause Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame**

00004190 RL64PC_P1 RX packet Length in 64-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received and equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004194 RL65PC_P1 RX packet Length in 65-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004198 RL128PC_P1 RX packet Length in 128-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received and transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000419C RL256PC_P1 RX packet Length in 256-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000041A0 RL512PC_P1 RX packet Length in 512-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

000041A4 RL1024PC_P1 RX packet Length in 1024-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

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000041A8 ROCL_P1 RX Octet Counter Low double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000041AC ROCH_P1 Rx Octet Counter High double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above)**

000041B0 RDPC_CTRL_P1 RX CTRL Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000041B4 RDPC_ING_P1 RX Ingress Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter**

000041B8 RDPC_ARL_P1 RX ARL Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000041D0 TMIB_HF_STS_P1 TX Port MIB Counter Half Full Status of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False

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		1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status** 0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True
2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status** 0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000041D4 RMIB_HF_STS_P1 RX Port MIB Counter Half Full Status of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXINGHF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status** 0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status** 0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False

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		1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

00004200 TDPC_P2 TX Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event which the frame should be dropped on output due to the late collision or excessive collision**

00004204 TCRC_P2 TX CRC Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004208 TUPC_P2 TX Unicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error, which excludes Pause frame but includes MAC control and successful retransmission**

0000420C TMPC_P2 TX Multicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004210 TBPC_P2 TX Broadcast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004214 TCEC_P2 TX Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurrence during frame transmission**

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00004218 TSCEC_P2 TX Single Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

0000421C TMCEC_P2 TX Multiple Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004220 TDEC_P2 TX Deferred Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.**

00004224 TLCEC_P2 TX Late Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004228 TXCEC_P2 TX excessive Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions**

0000422C TPPC_P2 TX Pause Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	**The number of correctly transmitted MAC flow-control frame**

00004230 TL64PC_P2 TX packet Length in 64-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	**It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.**

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00004234 TL65PC_P2 TX packet Length in 65-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004238 TL128PC_P2 TX packet Length in 128-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000423C TL256PC_P2 TX packet Length in 256-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

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00004240 TL512PC_P2 TX packet Length in 512-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

00004244 TL1024PC_P2 TX packet Length in 1024-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

00004248 TOCL_P2 TX Octet Counter Low double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

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0000424C TOCH_P2 TX Octet Counter High double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004260 RDPC_P2 RX Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit

00004264 RFPC_P2 RX Filtering Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero**

00004268 RUPC_P2 RX Unicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000426C RMPC_P2 RX Multicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004270 RBPC_P2 RX Broadcast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004274 RAEPC_P2 RX Alignment Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted**

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00004278 RCEPC_P2 RX CRC(FCS) Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted**

0000427C RUSPC_P2 RX Undersize Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed**

00004280 RFEPC_P2 RX Fragment Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

00004284 ROSPC_P2 RX Oversize Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error**

00004288 RJEPC_P2 RX Jabber Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets, excluding framing bits but including FCS octets, and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

0000428C RPPC_P2 RX Pause Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame**

00004290 RL64PC_P2 RX packet Length in 64-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004294 RL65PC_P2 RX packet Length in 65-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004298 RL128PC_P2 RX packet Length in 128-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000429C RL256PC_P2 RX packet Length in 256-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000042A0 RL512PC_P2 RX packet Length in 512-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

000042A4 RL1024PC_P2 RX packet Length in 1024-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

000042A8 ROCL_P2 RX Octet Counter Low double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.

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RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000042AC ROCH_P2 Rx Octet Counter High double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above).**

000042B0 RDPC_CTRL_P2 RX CTRL Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000042B4 RDPC_ING_P2 RX Ingress Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter**

000042B8 RDPC_ARL_P2 RX ARL Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000042D0 TMIB_HF_STS_P2 TX Port MIB Counter Half Full Status of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status**

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		0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True
2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status** 0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000042D4 RMIB_HF_STS_P2 RX Port MIB Counter Half Full Status of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status**

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		0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status** 0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False 1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

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00004300 TDPC_P3 TX Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event which the frame should be dropped on output due to late collision or excessive collision**

00004304 TCRC_P3 TX CRC Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004308 TUPC_P3 TX Unicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.**

0000430C TMPC_P3 TX Multicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004310 TBPC_P3 TX Broadcast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004314 TCEC_P3 TX Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurrence during frame transmission**

00004318 TSCEC_P3 TX Single Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

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0000431C TMCEC_P3 TX Multiple Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004320 TDEC_P3 TX Deferred Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.**

00004324 TLCEC_P3 TX Late Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004328 TXCEC_P3 TX excessive Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions**

0000432C TPPC_P3 TX Pause Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	**The number of correct transmitted MAC flow-control frame**

00004330 TL64PC_P3 TX packet Length in 64-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	**It indicates the total number of packets, including bad packets transmitted and equal to 64 octets in length, and excluding framing bits but including FCS octets.**

00004334 TL65PC_P3 TX packet Length in 65-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, and excluding framing bits but including FCS octets.**

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00004338 TL128PC_P3 TX packet Length in 128-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, and excluding framing bits but including FCS octets.**

0000433C TL256PC_P3 TX packet Length in 256-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, and excluding framing bits but including FCS octets.**

00004340 TL512PC_P3 TX packet Length in 512-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, and excluding framing bits but including FCS octets.**

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00004344 TL1024PC_P3 TX packet Length in 1024-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, and excluding framing bits but including FCS octets.**

00004348 TOCL_P3 TX Octet Counter Low double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000434C TOCH_P3 TX Octet Counter High double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004360 RDPC_P3 RX Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004364 RFPC_P3 RX Filtering Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero**

00004368 RUPC_P3 RX Unicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000436C RMPC_P3 RX Multicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004370 RBPC_P3 RX Broadcast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004374 RAEPC_P3 RX Alignment Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted**

00004378 RCEPC_P3 RX CRC(FCS) Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted**

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0000437C RUSPC_P3 RX Undersize Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed**

00004380 RFEPC_P3 RX Fragment Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

00004384 ROSPC_P3 RX Oversize Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error**

00004388 RJEPC_P3 RX Jabber Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

0000438C RPPC_P3 RX Pause Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame**

00004390 RL64PC_P3 RX packet Length in 64-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004394 RL65PC_P3 RX packet Length in 65-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004398 RL128PC_P3 RX packet Length in 128-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000439C RL256PC_P3 RX packet Length in 256-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000043A0 RL512PC_P3 RX packet Length in 512-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_C	**It indicates the total number of packets, including bad packets received between**

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NT	**512 and 1023 octets in length, excluding framing bits but including FCS octets.**

000043A4 RL1024PC_P3 RX packet Length in 1024-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

000043A8 ROCL_P3 RX Octet Counter Low double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000043AC ROCH_P3 Rx Octet Counter High double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above).**

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000043B0 RDPC_CTRL_P3 RX CTRL Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000043B4 RDPC_ING_P3 RX Ingress Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter**

000043B8 RDPC_ARL_P3 RX ARL Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000043D0 TMIB_HF_STS_P3 TX Port MIB Counter Half Full Status of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS

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Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status** 0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True

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2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status** 0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000043D4 RMIB_HF_STS_P3 RX Port MIB Counter Half Full Status of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status** 0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True

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11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status** 0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False 1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

00004400 TDPC_P4 TX Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event which the frame should be dropped on output due to the late collision or excessive collision.**

00004404 TCRC_P4 TX CRC Packet Counter of Port 4 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004408 TUPC_P4 TX Unicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.**

0000440C TMPC_P4 TX Multicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004410 TBPC_P4 TX Broadcast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004414 TCEC_P4 TX Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurrence during frame transmission**

00004418 TSCEC_P4 TX Single Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

0000441C TMCEC_P4 TX Multiple Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004420 TDEC_P4 TX Deferred Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.**

00004424 TLCEC_P4 TX Late Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004428 TXCEC_P4 TX excessive Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions**

0000442C TPPC_P4 TX Pause Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:0	TX_PAUSE_CNT	**The number of correct transmitted MAC flow-control frame**

00004430 TL64PC_P4 TX packet Length in 64-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	**It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004434 TL65PC_P4 TX packet Length in 65-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004438 TL128PC_P4 TX packet Length in 128-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

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0000443C TL256PC_P4 TX packet Length in 256-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

00004440 TL512PC_P4 TX packet Length in 512-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

00004444 TL1024PC_P4 TX packet Length in 1024-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

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00004448 TOCL_P4 TX Octet Counter Low double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000444C TOCH_P4 TX Octet Counter High double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004460 RDPC_P4 RX Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004464 RFPC_P4 RX Filtering Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero**

00004468 RUPC_P4 RX Unicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000446C RMPC_P4 RX Multicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004470 RBPC_P4 RX Broadcast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004474 RAEPC_P4 RX Alignment Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted**

00004478 RCEPC_P4 RX CRC(FCS) Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted**

0000447C RUSPC_P4 RX Undersize Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed.**

00004480 RFEPC_P4 RX Fragment Error Packet Counter of Port 4 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

00004484 ROSPC_P4 RX Oversize Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error**

00004488 RJEPC_P4 RX Jabber Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

0000448C RPPC_P4 RX Pause Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame**

00004490 RL64PC_P4 RX packet Length in 64-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004494 RL65PC_P4 RX packet Length in 65-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004498 RL128PC_P4 RX packet Length in 128-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000449C RL256PC_P4 RX packet Length in 256-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000044A0 RL512PC_P4 RX packet Length in 512-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

000044A4 RL1024PC_P4 RX packet Length in 1024-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

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000044A8 ROCL_P4 RX Octet Counter Low double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000044AC ROCH_P4 Rx Octet Counter High double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above).**

000044B0 RDPC_CTRL_P4 RX CTRL Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000044B4 RDPC_ING_P4 RX Ingress Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter**

000044B8 RDPC_ARL_P4 RX ARL Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000044D0 TMIB_HF_STS_P4 TX Port MIB Counter Half Full Status of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False

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		1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status** 0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True
2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status** 0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000044D4 RMIB_HF_STS_P4 RX Port MIB Counter Half Full Status of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXINGHF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status** 0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status** 0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False

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		1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

00004500 TDPC_P5 TX Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event which the frame should be dropped on output due to the late collision or excessive collision**

00004504 TCRC_P5 TX CRC Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004508 TUPC_P5 TX Unicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.**

0000450C TMPC_P5 TX Multicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004510 TBPC_P5 TX Broadcast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004514 TCEC_P5 TX Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurrence during frame transmission**

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00004518 TSCEC_P5 TX Single Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

0000451C TMCEC_P5 TX Multiple Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004520 TDEC_P5 TX Deferred Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.**

00004524 TLCEC_P5 TX Late Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004528 TXCEC_P5 TX excessive Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions**

0000452C TPPC_P5 TX Pause Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	**The number of correct transmitted MAC flow-control frame**

00004530 TL64PC_P5 TX packet Length in 64-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	**It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.**

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00004534 TL65PC_P5 TX packet Length in 65-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004538 TL128PC_P5 TX packet Length in 128-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000453C TL256PC_P5 TX packet Length in 256-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

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00004540 TL512PC_P5 TX packet Length in 512-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

00004544 TL1024PC_P5 TX packet Length in 1024-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

00004548 TOCL_P5 TX Octet Counter Low double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

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0000454C TOCH_P5 TX Octet Counter High double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004560 RDPC_P5 RX Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004564 RFPC_P5 RX Filtering Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero**

00004568 RUPC_P5 RX Unicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000456C RMPC_P5 RX Multicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004570 RBPC_P5 RX Broadcast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004574 RAEPC_P5 RX Alignment Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted**

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00004578 RCEPC_P5 RX CRC(FCS) Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted**

0000457C RUSPC_P5 RX Undersize Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed**

00004580 RFEPC_P5 RX Fragment Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

00004584 ROSPC_P5 RX Oversize Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error**

00004588 RJEPC_P5 RX Jabber Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

0000458C RPPC_P5 RX Pause Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame**

00004590 RL64PC_P5 RX packet Length in 64-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004594 RL65PC_P5 RX packet Length in 65-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004598 RL128PC_P5 RX packet Length in 128-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000459C RL256PC_P5 RX packet Length in 256-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000045A0 RL512PC_P5 RX packet Length in 512-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

000045A4 RL1024PC_P5 RX packet Length in 1024-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

000045A8 ROCL_P5 RX Octet Counter Low double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.

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RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000045AC ROCH_P5 Rx Octet Counter High double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above).**

000045B0 RDPC_CTRL_P5 RX CTRL Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000045B4 RDPC_ING_P5 RX Ingress Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter**

000045B8 RDPC_ARL_P5 RX ARL Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000045D0 TMIB_HF_STS_P5 TX Port MIB Counter Half Full Status of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status**

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		0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True
2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status** 0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000045D4 RMIB_HF_STS_P5 RX Port MIB Counter Half Full Status of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status**

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		0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status** 0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False 1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

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00004600 TDPC_P6 TX Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	**The number of event which the frame should be dropped on output due to the late collision or excessive collision**

00004604 TCRC_P6 TX CRC Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	**The number of event which the frame will output a CRC packet due to TX FIFO underrun**

00004608 TUPC_P6 TX Unicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	**The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.**

0000460C TMPC_P6 TX Multicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TX_MCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	**The number of multicast frames transmitted without any error**

00004610 TBPC_P6 TX Broadcast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	**The number of broadcast frames transmitted without any error**

00004614 TCEC_P6 TX Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	**The total number of collision events occurrence during frame transmission**

00004618 TSCEC_P6 TX Single Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	**The number of frames transmitted without any error following a single collision**

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0000461C TMCEC_P6 TX Multiple Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	**The number of frames transmitted without any error following multiple collisions**

00004620 TDEC_P6 TX Deferred Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	**The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.**

00004624 TLCEC_P6 TX Late Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	**The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet**

00004628 TXCEC_P6 TX excessive Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	**The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions**

0000462C TPPC_P6 TX Pause Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	**The number of correct transmitted MAC flow-control frame**

00004630 TL64PC_P6 TX packet Length in 64-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	**It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004634 TL65PC_P6 TX packet Length in 65-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

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00004638 TL128PC_P6 TX packet Length in 128-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000463C TL256PC_P6 TX packet Length in 256-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

00004640 TL512PC_P6 TX packet Length in 512-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	**It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.**

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00004644 TL1024PC_P6 TX packet Length in 1024-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

00004648 TOCL_P6 TX Octet Counter Low double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	**{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.** **TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000464C TOCH_P6 TX Octet Counter High double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	**Refer to TX_OCT_CNT_L (above).**

00004660 RDPC_P6 RX Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	RX_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	**The number of event which the frame should be dropped due to** 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004664 RFPC_P6 RX Filtering Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	**The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero**

00004668 RUPC_P6 RX Unicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	**The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

0000466C RMPC_P6 RX Multicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	**The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004670 RBPC_P6 RX Broadcast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	**The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames**

00004674 RAEPC_P6 RX Alignment Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted**

00004678 RCEPC_P6 RX CRC(FCS) Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	**The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted**

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0000467C RUSPC_P6 RX Undersize Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	**The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed**

00004680 RFEPC_P6 RX Fragment Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	**The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

00004684 ROSPC_P6 RX Oversize Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	**The number of frames with length larger than the maximum frame size, received without any error**

00004688 RJEPC_P6 RX Jabber Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT[31:16]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	**The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)**

0000468C RPPC_P6 RX Pause Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	**The number of correctly received MAC flow-control frame**

00004690 RL64PC_P6 RX packet Length in 64-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	**It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.**

00004694 RL65PC_P6 RX packet Length in 65-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	**It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.**

00004698 RL128PC_P6 RX packet Length in 128-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	**It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.**

0000469C RL256PC_P6 RX packet Length in 256-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	**It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.**

000046A0 RL512PC_P6 RX packet Length in 512-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_C	**It indicates the total number of packets, including bad packets received between**

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NT	**512 and 1023 octets in length, excluding framing bits but including FCS octets.**

000046A4 RL1024PC_P6 RX packet Length in 1024-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	**It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.**

000046A8 ROCL_P6 RX Octet Counter Low double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	**{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.** **RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.** RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000046AC ROCH_P6 Rx Octet Counter High double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	**Refer to RX_OCT_CNT_L (above).**

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000046B0 RDPC_CTRL_P6 RX CTRL Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	**The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL**

000046B4 RDPC_ING_P6 RX Ingress Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	**The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter**

000046B8 RDPC_ARL_P6 RX ARL Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	**The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit**

000046D0 TMIB_HF_STS_P6 TX Port MIB Counter Half Full Status of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS

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Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCOL_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	**TX Octet Counter Half Full Status** 0: False 1: True
17	TXL1024_HF_STS	**TX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	TXL512_HF_STS	**TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	TXL256_HF_STS	**TX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	TXL128_HF_STS	**TX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	TXL65_HF_STS	**TX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	TXL64_HF_STS	**TX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True
11	TXPAU_HF_STS	**TX Pause Packet Counter Half Full Status** 0: False 1: True
10	TXECOL_HF_STS	**TX Excessive Collision Counter Half Full Status** 0: False 1: True
9	TXLCOL_HF_STS	**TX Late Collision Counter Half Full Status** 0: False 1: True
8	TXDFR_HF_STS	**TX Deferred Counter Half Full Status** 0: False 1: True
7	TXMCOL_HF_STS	**TX Multiple Collision Counter Half Full Status** 0: False 1: True
6	TXSCOL_HF_STS	**TX Single Collision Counter Half Full Status** 0: False 1: True
5	TXCOL_HF_STS	**TX Collision Event Counter Half Full Status** 0: False 1: True
4	TXBRD_HF_STS	**TX Broadcast Counter Half Full Status** 0: False 1: True
3	TXMUL_HF_STS	**TX Multicast Counter Half Full Status** 0: False 1: True

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2	TXUNI_HF_STS	**TX Unicast Counter Half Full Status** 0: False 1: True
1	TXCRC_HF_STS	**TX CRC Counter Half Full Status** 0: False 1: True
0	TXDROP_HF_STS	**TX DROP Counter Half Full Status** 0: False 1: True

000046D4 RMIB_HF_STS_P6 RX Port MIB Counter Half Full Status of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	**RX ARL Drop Counter Half Full Status** 0: False 1: True
20	RXING_HF_STS	**RX Ingress Drop Counter Half Full Status** 0: False 1: True
19	RXCTRL_HF_STS	**RX CTRL Drop Counter Half Full Status** 0: False 1: True
18	RXOCT_HF_STS	**RX Octet Counter Half Full Status** 0: False 1: True
17	RXL1024_HF_STS	**RX Packet Length above 1024 Bytes Counter Half Full Status** 0: False 1: True
16	RXL512_HF_STS	**RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status** 0: False 1: True
15	RXL256_HF_STS	**RX Packet Length 256 ~ 511 Bytes Counter Half Full Status** 0: False 1: True
14	RXL128_HF_STS	**RX Packet Length 128 ~ 255 Bytes Counter Half Full Status** 0: False 1: True
13	RXL65_HF_STS	**RX Packet Length 65 ~ 127 Bytes Counter Half Full Status** 0: False 1: True
12	RXL64_HF_STS	**RX Packet Length 64 Bytes Counter Half Full Status** 0: False 1: True

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11	RXPAU_HF_STS	**RX Pause Packet Counter Half Full Status** 0: False 1: True
10	RXJAB_HF_STS	**RX Jabber Error Counter Half Full Status** 0: False 1: True
9	RXOVR_HF_STS	**RX Oversize Packet Counter Half Full Status** 0: False 1: True
8	RXFRG_HF_STS	**RX Fragment Error Counter Half Full Status** 0: False 1: True
7	RXUND_HF_STS	**RX Undersize Packet Counter Half Full Status** 0: False 1: True
6	RXCRC_HF_STS	**RX CRC ERROR Counter Half Full Status** 0: False 1: True
5	RXALG_HF_STS	**RX Alignment Error Counter Half Full Status** 0: False 1: True
4	RXBRD_HF_STS	**RX Broadcast Counter Half Full Status** 0: False 1: True
3	RXMUL_HF_STS	**RX Multicast Counter Half Full Status** 0: False 1: True
2	RXUNI_HF_STS	**RX Unicast Counter Half Full Status** 0: False 1: True
1	RXFIL_HF_STS	**RX Filtering Counter Half Full Status** 0: False 1: True
0	RXDROP_HF_STS	**RX DROP Counter Half Full Status** 0: False 1: True

00004F00 AE0CNT ACL Event 0 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE0CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE0CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE0CNT	**Total number of ARL event 0 occurred**

00004F04 AE1CNT ACL Event 1 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	AE1CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE1CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE1CNT	**Total number of ARL event 1 occurred**

00004F08 AE2CNT ACL Event 2 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE2CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE2CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE2CNT	**Total number of ARL event 2 occurred**

00004F0C AE3CNT ACL Event 3 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE3CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE3CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE3CNT	**Total number of ARL event 3 occurred**

00004F10 AE4CNT ACL Event 4 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE4CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE4CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE4CNT	**Total number of ARL event 4 occurred**

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00004F14 AE5CNT ACL Event 5 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE5CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE5CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE5CNT	**Total number of ARL event 5 occurred**

00004F18 AE6CNT ACL Event 6 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE6CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE6CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE6CNT	**Total number of ARL event 6 occurred**

00004F1C AE7CNT ACL Event 7 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE7CNT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE7CNT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE7CNT	**Total number of ARL event 7 occurred**

00004FE0 MIBCCR MIB Counter Control 800000F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIB_ENABLE															
Type	RW															
Reset	1															

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_OCT_CNT_GOOD	RX_OCT_CNT_BAD	TX_OCT_CNT_GOOD	TX_OCT_CNT_BAD				
Type									RW	RW	RW	RW				
Reset									1	1	1	1				

Bit(s)	Name	Description
31	MIB_ENABLE	1'b0: Disable MIB counter and set all counter values to zero. 1'b1: Enable MIB counter.
7	RX_OCT_CNT_GOOD	1'b0: Octets of good received packets are not counted in RX_OCT_L_CNT and RX_OCT_H_CNT. 1'b1: Octets of good received packets are counted in RX_OCT_L_CNT and RX_OCT_H_CNT.
6	RX_OCT_CNT_BAD	1'b0: Octets of bad received packets are not counted in RX_OCT_L_CNT and RX_OCT_H_CNT. 1'b1: Octets of bad received packets are counted in RX_OCT_L_CNT and RX_OCT_H_CNT.
5	TX_OCT_CNT_GOOD	1'b0: Octets of good transmitted packets are not counted in TX_OCT_L_CNT and TX_OCT_H_CNT. 1'b1: Octets of good transmitted packets are counted in TX_OCT_L_CNT and TX_OCT_H_CNT. Good transmitted packets are frames transmitted successfully.
4	TX_OCT_CNT_BAD	1'b0: Octets of bad transmitted packets are not counted in TX_OCT_L_CNT and TX_OCT_H_CNT. 1'b1: Octets of bad transmitted packets are counted in TX_OCT_L_CNT and TX_OCT_H_CNT. Bad transmitted packets are frames transmitted in collision with deliberately destroyed CRC.

00004FE4 AECCR ARL Event Counter Control 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AEC_ENABLE															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	AEC_ENABLE	1'b0: Disable ARL event counter function and set all counter value to zero. 1'b1: Enable ARL event counter.

00004FE8 AEMIB_HF_STS ARL Event MIB Counter Half Full Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ARLEV7_HF_STS	ARLEV6_HF_STS	ARLEV5_HF_STS	ARLEV4_HF_STS	ARLEV3_HF_STS	ARLEV2_HF_STS	ARLEV1_HF_STS	ARLEV0_HF_STS
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

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Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	ARLEV7_HF_STS	**ARL Event 7 MIB Counter Half Full Status** 0: False 1: True
6	ARLEV6_HF_STS	**ARL Event 6 MIB Counter Half Full Status** 0: False 1: True
5	ARLEV5_HF_STS	**ARL Event 5 MIB Counter Half Full Status** 0: False 1: True
4	ARLEV4_HF_STS	**ARL Event 4 MIB Counter Half Full Status** 0: False 1: True
3	ARLEV3_HF_STS	**ARL Event 3 MIB Counter Half Full Status** 0: False 1: True
2	ARLEV2_HF_STS	**ARL Event 2 MIB Counter Half Full Status** 0: False 1: True
1	ARLEV1_HF_STS	**ARL Event 1 MIB Counter Half Full Status** 0: False 1: True
0	ARLEV0_HF_STS	**ARL Event 0 MIB Counter Half Full Status** 0: False 1: True

00004FF0 MIBHF_INT_EN Port/ARL MIB Counter Half Full Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HFSTS_ARL_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										HFSTS_P6_EN	HFSTS_P5_EN	HFSTS_P4_EN	HFSTS_P3_EN	HFSTS_P2_EN	HFSTS_P1_EN	HFSTS_P0_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HFSTS_ARL_EN	**ARL MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable
6	HFSTS_P6_EN	**Port 6 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable
5	HFSTS_P5_EN	**Port 5 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.**

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		0: Disable 1: Enable
4	HFSTS_P4_EN	**Port 4 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable
3	HFSTS_P3_EN	**Port 3 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable
2	HFSTS_P2_EN	**Port 2 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable
1	HFSTS_P1_EN	**Port 1 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable
0	HFSTS_P0_EN	**Port 0 MIB Half Full Interrupt Enable.** **When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.** 0: Disable 1: Enable

00004FF4 MIBHF_INT_STS Port/ARL MIB Counter Half Full Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HFSTS_ARL															
Type	W1C															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										HFSTS_P6	HFSTS_P5	HFSTS_P4	HFSTS_P3	HFSTS_P2	HFSTS_P1	HFSTS_P0
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HFSTS_ARL	**ARL MIB Half Full Interrupt Status** 0: False 1: True
6	HFSTS_P6	**Port 6 MIB Half Full Interrupt Status** 0: False 1: True
5	HFSTS_P5	**Port 5 MIB Half Full Interrupt Status** 0: False 1: True
4	HFSTS_P4	**Port 4 MIB Half Full Interrupt Status** 0: False 1: True
3	HFSTS_P3	**Port 3 MIB Half Full Interrupt Status** 0: False

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		1: True
2	HFSTS_P2	**Port 2 MIB Half Full Interrupt Status** 0: False 1: True
1	HFSTS_P1	**Port 1 MIB Half Full Interrupt Status** 0: False 1: True
0	HFSTS_P0	**Port 0 MIB Half Full Interrupt Status** 0: False 1: True

00007000 SYS_CTRL System Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ACL_TAB_INIT	MAC_TAB_INIT	VLAN_TAB_INIT				BMU_MEM_INIT
Type										RO	RO	RO				RO
Reset										0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TRTCM_BIST_STS	MASK_BIST_STS	CTRL_BIST_STS	ADDR_BIST_STS	VLN_BIST_STS	MIB_BIST_STS	PB_BIST_STS	PL_BIST_STS	FL_BIST_STS	MBIST_CMP	MBIST_EN		SW_PHY_RST	SW_SYS_RST	SW_REG_RST
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW		R/W/SC	R/W/SC	R/W/SC
Reset		0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
22	ACL_TAB_INIT	**ACL Table Initialization Complete** 1: Complete 0: Not Ready
21	MAC_TAB_INIT	**MAC Table Initialization Complete** 1: Complete 0: Not Ready
20	VLAN_TAB_INIT	**VLAN Table Initialization Complete** 1: Complete 0: Not Ready
16	BMU_MEM_INIT	**BMU Memory Initialization Complete** 1: Complete 0: Not Ready
14	TRTCM_BIST_STS	**TRTCM BIST Status** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
13	MASK_BIST_STS	**Mask Memory BIST Status** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
12	CTRL_BIST_STS	**CTRL Memory BIST Status** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
11	ADDR_BIST_STS	**Address Memory BIST Status** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
10	VLN_BIST_STS	**VLAN Memory BIST Status** This bit is valid only when MBIST_CMP is true.

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		1: OK 0: Failed
9	MIB_BIST_STS	**MIB Memory BIST Status (Port0~Port6)** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
8	PB_BIST_STS	**Pack Buffer Memory BIST Status** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
7	PL_BIST_STS	**Page Link Memory BIST Status** This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
6	FL_BIST_STS	**Frame Link Memory BIST Status** This bit is valid only when MBIST_CMP is true 1: OK 0: Failed
5	MBIST_CMP	**Memory BIST Complete** 1: Complete 0: Idle or not finish yet
4	MBIST_EN	**Memory BIST Enable** 1: Enable 0: Disable or test complete
2	SW_PHY_RST	**Software PHY Reset** 1: Write 1 to reset PHY's states to default. 0: Reset done/reset inactive.
1	SW_SYS_RST	**Software System Reset** 1: Write 1 to reset switch's states to default (excluding PHY and registers). Please note that all MACs must be forced to link-down before setting this bit. 0: Reset done/reset is inactive.
0	SW_REG_RST	**Software Register Reset** 1: Write 1 to reset pbus and MDIO registers to default values. Please note that all MACs must be forced to link-down before setting this bit. 0: Reset done/reset is inactive.

00007004 PM_CTRL Power Management Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PM_STS														PME
Type		RO														RW
Reset		0	0	0	0	0	0	0								0

Bit(s)	Name	Description
14:8	PM_STS	**Power Management Status** It indicates current power management status per port bit 8 => port 0 bit 9 => port 1 bit 14 => port 6 1: In low power mode 0: In normal mode
0	PME	**Power Management Enable** It indicates Switch can enter power saving mode 1: Enable

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0: Disable

00007008 SYS_INT_EN System Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_INT_EN	ARL_SEC_TAG_INT_EN	ARL_SEC_VLAN_INT_EN	ARL_SEC_IG1X_INT_EN	ARL_PKT_BC_INT_EN	ARL_EQ_ERR_INT_EN	ARL_PKT_QERR_INT_EN	ARL_TBL_ERR_INT_EN					PTP_INT_EN	MIB_INT_EN	BMU_INT_EN	MAC_PC_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PHY6_INT_EN	PHY5_INT_EN	PHY4_INT_EN	PHY3_INT_EN	PHY2_INT_EN	PHY1_INT_EN	PHY0_INT_EN		PHY6_LC_INTE	PHY5_LC_INTE	PHY4_LC_INTE	PHY3_LC_INTE	PHY2_LC_INTE	PHY1_LC_INTE	PHY0_LC_INTE
Type		RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ACL_INT_EN	**ACL Interrupt Enable** 1: Enable 0: Disable
30	ARL_SEC_TAG_INT_EN	**ARL Security Tag Interrupt Enable** 1: Enable 0: Disable
29	ARL_SEC_VLAN_INT_EN	**ARL Security VLAN Interrupt Enable** 1: Enable 0: Disable
28	ARL_SEC_IG1X_INT_EN	**ARL Security 1G Interrupt Enable** 1: Enable 0: Disable
27	ARL_PKT_BC_INT_EN	**ARL Broadcast Packet Drop Interrupt Enable** 1: Enable 0: Disable
26	ARL_EQ_ERR_INT_EN	**ARL Enqueue Error Interrupt Enable** 1: Enable 0: Disable
25	ARL_PKT_QERR_INT_EN	**ARL Packet Queue Error Interrupt Enable** 1: Enable 0: Disable
24	ARL_TBL_ERR_INT_EN	**ARL Table Error Interrupt Enable** 1: Enable 0: Disable
19	PTP_INT_EN	**PTP Interrupt Enable** 1: Enable 0: Disable
18	MIB_INT_EN	**MIB Interrupt Enable** 1: Enable 0: Disable
17	BMU_INT_EN	**BMU Interrupt Enable** 1: Enable 0: Disable
16	MAC_PC_INT_EN	**MAC/Port Controller Interrupt Enable** 1: Enable 0: Disable
14	PHY6_INT_EN	**PHY 6 Interrupt Enable**

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		1: Enable 0: Disable
13	PHY5_INT_EN	**PHY 5 Interrupt Enable** 1: Enable 0: Disable
12	PHY4_INT_EN	**PHY 4 Interrupt Enable** 1: Enable 0: Disable
11	PHY3_INT_EN	**PHY 3 Interrupt Enable** 1: Enable 0: Disable
10	PHY2_INT_EN	**PHY 2 Interrupt Enable** 1: Enable 0: Disable
9	PHY1_INT_EN	**PHY 1 Interrupt Enable** 1: Enable 0: Disable
8	PHY0_INT_EN	**PHY 0 Interrupt Enable** 1: Enable 0: Disable
6	PHY6_LC_INTE	**PHY 6 Link-up Change Interrupt Enable** 1: Enable 0: Disable
5	PHY5_LC_INTE	**PHY 5 Link-up Change Interrupt Enable** 1: Enable 0: Disable
4	PHY4_LC_INTE	**PHY 4 Link-up Change Interrupt Enable** 1: Enable 0: Disable
3	PHY3_LC_INTE	**PHY 3 Link-up Change Interrupt Enable** 1: Enable 0: Disable
2	PHY2_LC_INTE	**PHY 2 Link-up Change Interrupt Enable** 1: Enable 0: Disable
1	PHY1_LC_INTE	**PHY 1 Link-up Change Interrupt Enable** 1: Enable 0: Disable
0	PHY0_LC_INTE	**PHY 0 Link-up Change Interrupt Enable** 1: Enable 0: Disable

0000700C SYS_INT_STS System Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_INT	ARL_SEC_TAG_INT	ARL_SEC_VLAN_INT	ARL_SEC_IG1X_INT	ARL_PKT_BC_INT	ARL_EQ_ERR_INT	ARL_PKT_QERR_INT	ARL_TBL_ERR_INT					PTP_INT	MIB_INT	BMU_INT	MAC_PC_INT
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PHY6_INT	PHY5_INT	PHY4_INT	PHY3_INT	PHY2_INT	PHY1_INT	PHY0_INT		PHY6_LC_INT	PHY5_LC_INT	PHY4_LC_INT	PHY3_LC_INT	PHY2_LC_INT	PHY1_LC_INT	PHY0_LC_INT
Type		W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	ACL_INT	**ACL Interrupt Status** 1: True 0: False
30	ARL_SEC_TAG_INT	**ARL Security Tag Interrupt Status** 1: True 0: False
29	ARL_SEC_VLAN_INT	**ARL Security VLAN Interrupt Status** 1: True 0: False
28	ARL_SEC_IG1X_INT	**ARL Security 1G Interrupt Status** 1: True 0: False
27	ARL_PKT_BC_INT	**ARL Broadcast Packet Drop Interrupt Status** 1: True 0: False
26	ARL_EQ_ERR_INT	**ARL Enqueue Error Status** 1: True 0: False
25	ARL_PKT_QERR_INT	**ARL Packet Queue Error Status** 1: True 0: False
24	ARL_TBL_ERR_INT	**ARL Table Error Interrupt Status** 1: True 0: False
19	PTP_INT	**PTP Interrupt Status** 1: True 0: False
18	MIB_INT	**MIB Interrupt Status** 1: True 0: False
17	BMU_INT	**BMU Interrupt Status** 1: True 0: False
16	MAC_PC_INT	**MAC/Port Controller Interrupt Status** 1: True 0: False
14	PHY6_INT	**PHY 6 Interrupt Status** 1: True 0: False
13	PHY5_INT	**PHY 5 Interrupt Status** 1: True 0: False
12	PHY4_INT	**PHY 4 Interrupt Status** 1: True 0: False
11	PHY3_INT	**PHY 3 Interrupt Status** 1: True 0: False
10	PHY2_INT	**PHY 2 Interrupt Status** 1: True 0: False
9	PHY1_INT	**PHY 1 Interrupt Status** 1: True 0: False
8	PHY0_INT	**PHY 0 Interrupt Status** 1: True

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		0: False
6	PHY6_LC_INT	**PHY 6 Link-up Change Interrupt Status** 1: True 0: False
5	PHY5_LC_INT	**PHY 5 Link-up Change Interrupt Status** 1: True 0: False
4	PHY4_LC_INT	**PHY 4 Link-up Change Interrupt Status** 1: True 0: False
3	PHY3_LC_INT	**PHY 3 Link-up Change Interrupt Status** 1: True 0: False
2	PHY2_LC_INT	**PHY 2 Link-up Change Interrupt Status** 1: True 0: False
1	PHY1_LC_INT	**PHY 1 Link-up Change Interrupt Status** 1: True 0: False
0	PHY0_LC_INT	**PHY 0 Link-up Change Interrupt Status** 1: True 0: False

00007018 PHY_POLL PHY Polling and SMI Master Control Register 007F8600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PHY_AP_EN								EEE_POLL_EN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PHY_PRE_EN	RX_TA1_CHK_OFF		PHY_END_ADDR					PMDC_CFG			PHY_ST_ADDR				
Type	RW	RW		RW					RW			RW				
Reset	1	0		0	0	1	1	0	0	0		0	0	0	0	0

Bit(s)	Name	Description
30:24	PHY_AP_EN	**PHY Auto-Polling Enable** It indicates the updating PHY status by auto-polling or side-band signals. bit 24 => port 0 bit 25 => port 1 bit 30 => port 6 1: PHY status obtained by Auto-polling 0: PHY status obtained by side-band signals
22:16	EEE_POLL_EN	**PHY EEE Polling Enable** It indicates polling the EEE capability of each PHY. bit 16 => port 0 bit 17 => port 1 bit 22 => port 6 1: Enable 0: Disable
15	PHY_PRE_EN	**PHY Preamble Enable** It indicates that the SMI master will send preamble bits (32 bits) at each MDIO read/write transaction. 1: Enable 0: Disable Note: This bit will affect both PHY auto-polling mode and PHY indirect access mode.

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14	RX_TA1_CHK_OFF	**Disable the checking of RX_TA1 value.** 1: Do not check the value of RX_TA1 state 0: Check the value of RX_TA1. If this value is not 0, it means that there is no response from PHYs, and all rx_data are invalid.
12:8	PHY_END_ADDR	**PHY Polling End Address** It indicates the end address of PHY auto-polling process.
7:6	PMDC_CFG	**PHY MDC Clock Configuration** It is used to configure the divider N for MDC clock frequency. The MDC clock is from the system clock (500MHz) and is divided by N. 2'b00: N=256 2'b01: N=64 2'b10: N=32 2'b11: N=16 Note: MDC clock should not be over the MDC clock maximum value of PHY.
4:0	PHY_ST_ADDR	**PHY Polling Start Address** It indicates the start address of PHY auto-polling process.

0000701C PHY_IAC PHY Indirect Access Control 00090000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_ACS_ST		MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		MDIO_ST	
Type	R/W/SC		RW					RW					RW		RW	
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDIO_RW_DATA															
Type	R/W/RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PHY_ACS_ST	**PHY Access Start** Start the indirect accessing of PHY's register. When the accessing is completed, this bit will be self-cleared to 0. 1: Start 0: Idle or indirect accessing is completed
29:25	MDIO_REG_ADDR	**MDIO Register Address Fields** Configure the Register Address Field.
24:20	MDIO_PHY_ADDR	**MDIO PHY Address Field** Configure the PHY address field.
19:18	MDIO_CMD	**MDIO Command Field** Configure the MDIO command field. 2'b01: MDIO Write 2'b10: MDIO Read
17:16	MDIO_ST	**MDIO Start Field** Configure the MDIO start field. 2'b01: Start Others: Reserved
15:0	MDIO_RW_DATA	**MDIO Read/Write Data Field** It indicates the MDIO data field for Read/Write accessing. When READ, this is used as MDIO read data (Read Only). When Write, this is used as MDIO write data (R/W).

00007020 PSR_P3_P0 PHY Status Register for Port 3 ~ Port 0 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LP_AN_CAP_P3	PHY_EEE1000_P3	PHY_EEE100_P3	PHY_XFC_P3	PHY_DUPLEX_P3	PHY_SPEED_P3		PHY_LINKUP_P3	LP_AN_CAP_P2	PHY_EEE1000_P2	PHY_EEE100_P2	PHY_XFC_P2	PHY_DUPLEX_P2	PHY_SPEED_P2		PHY_LINKUP_P2
Type	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO		RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LP_AN_CAP_P1	PHY_EEE1000_P1	PHY_EEE100_P1	PHY_XFC_P1	PHY_DUPLEX_P1	PHY_SPEED_P1		PHY_LINKUP_P1	LP_AN_CAP_P0	PHY_EEE1000_P0	PHY_EEE100_P0	PHY_XFC_P0	PHY_DUPLEX_P0	PHY_SPEED_P0		PHY_LINKUP_P0
Type	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO		RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	LP_AN_CAP_P3	**Port 3 Link Partner Auto-Negotiation Capability** 1: Link Partner supports AN 0: Link Partner does not support AN
30	PHY_EEE1000_P3	**Port 3 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 3000Base-T EEE
29	PHY_EEE100_P3	**Port 3 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 300Base-Tx EEE
28	PHY_XFC_P3	**Port 3 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
27	PHY_DUPLEX_P3	**Port 3 PHY Duplex status** 1: Full-duplex 0: Half-duplex
26:25	PHY_SPEED_P3	**Port 3 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
24	PHY_LINKUP_P3	**Port 3 PHY Link Status** 1: Link-up 0: Link-down
23	LP_AN_CAP_P2	**Port 2 Link Partner Auto-Negotiation Capability** 1: Link Partner supports AN 0: Link Partner does not support AN
22	PHY_EEE1000_P2	**Port 2 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 2000Base-T EEE
21	PHY_EEE100_P2	**Port 2 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 200Base-Tx EEE
20	PHY_XFC_P2	**Port 2 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
19	PHY_DUPLEX_P2	**Port 2 PHY Duplex status** 1: Full-duplex 0: Half-duplex
18	PHY_SPEED_P2	**Port 2 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved

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16	PHY_LINKUP_P2	**Port 2 PHY Link Status** 1: Link-up 0: Link-down
15	LP_AN_CAP_P1	**Port 1 Link Partner Auto-Negotiation Capability** 1: Link Partner supports AN 0: Link Partner does not support AN
14	PHY_EEE1000_P1	**Port 1 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 1000Base-T EEE
13	PHY_EEE100_P1	**Port 1 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 100Base-Tx EEE
12	PHY_XFC_P1	**Port 1 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
11	PHY_DUPLEX_P1	**Port 1 PHY Duplex status** 1: Full-duplex 0: Half-duplex
10:9	PHY_SPEED_P1	**Port 1 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
8	PHY_LINKUP_P1	**Port 1 PHY Link Status** 1: Link-up 0: Link-down
7	LP_AN_CAP_P0	**Port 0 Link Partner Auto-Negotiation Capability** 1: Link Partner is Auto-negotiable 0: Link Partner is not Auto-negotiable Note: While PHY is link-up but LP_AN_CAP is false, it means that the current link-up state is generated by Parallel Detection. So the current phy_speed and phy_duplex bits are updated from PHY's Link Partner advertisement register (REG 05). No speed or duplex validity is guaranteed.
6	PHY_EEE1000_P0	**Port 0 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 1000Base-T EEE
5	PHY_EEE100_P0	**Port 0 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 100Base-Tx EEE
4	PHY_XFC_P0	**Port 0 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
3	PHY_DUPLEX_P0	**Port 0 PHY Duplex status** 1: Full-duplex 0: Half-duplex
2:1	PHY_SPEED_P0	**Port 0 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
0	PHY_LINKUP_P0	**Port 0 PHY Link Status** 1: Link-up 0: Link-down

00007024 PSR_P6_P4 PHY Status Register for Port 6 ~ Port 4 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LP_AN_CAP_P6	PHY_EEE1000_P6	PHY_EEE100_P6	PHY_XFC_P6	PHY_DUPLEX_P6	PHY_SPEED_P6		PHY_LINKUP_P6
Type									RO	RO	RO	RO	RO	RO		RO
Reset									0	0	0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LP_AN_CAP_P5	PHY_EEE1000_P5	PHY_EEE100_P5	PHY_XFC_P5	PHY_DUPLEX_P5	PHY_SPEED_P5		PHY_LINKUP_P5	LP_AN_CAP_P4	PHY_EEE1000_P4	PHY_EEE100_P4	PHY_XFC_P4	PHY_DUPLEX_P4	PHY_SPEED_P4		PHY_LINKUP_P4
Type	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO		RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	LP_AN_CAP_P6	**Port 6 Link Partner Auto-Negotiation Capability** 1: Link Partner supports AN 0: Link Partner does not support AN
22	PHY_EEE1000_P6	**Port 6 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 6000Base-T EEE
21	PHY_EEE100_P6	**Port 6 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 600Base-Tx EEE
20	PHY_XFC_P6	**Port 6 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
19	PHY_DUPLEX_P6	**Port 6 PHY Duplex status** 1: Full-duplex 0: Half-duplex
18	PHY_SPEED_P6	**Port 6 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
16	PHY_LINKUP_P6	**Port 6 PHY Link Status** 1: Link-up 0: Link-down
15	LP_AN_CAP_P5	**Port 5 Link Partner Auto-Negotiation Capability** 1: Link Partner supports AN 0: Link Partner does not support AN
14	PHY_EEE1000_P5	**Port 5 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 5000Base-T EEE
13	PHY_EEE100_P5	**Port 5 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 500Base-Tx EEE
12	PHY_XFC_P5	**Port 5 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
11	PHY_DUPLEX_P5	**Port 5 PHY Duplex status** 1: Full-duplex 0: Half-duplex
10:9	PHY_SPEED_P5	**Port 5 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved

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8	PHY_LINKUP_P5	**Port 5 PHY Link Status** 1: Link-up 0: Link-down
7	LP_AN_CAP_P4	**Port 4 Link Partner Auto-Negotiation Capability** 1: Link Partner is Auto-negotiable 0: Link Partner is not Auto-negotiable Note: While PHY is link-up but LP_AN_CAP is false, it means that the current link-up state is generated by Parallel Detection. So the current phy_speed and phy_duplex bits are updated from PHY's Link Partner advertisement register (REG 05). No speed or duplex validity is guaranteed.
6	PHY_EEE1000_P4	**Port 4 EEE ability at 1000Base-T** 1: Support EEE at 1000Base-T 0: Do not support 5000Base-T EEE
5	PHY_EEE100_P4	**Port 4 EEE ability at 100Base-Tx** 1: Support EEE at 100Base-Tx 0: Do not support 500Base-Tx EEE
4	PHY_XFC_P4	**Port 4 MAC Flow Control Status** 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
3	PHY_DUPLEX_P4	**Port 4 PHY Duplex status** 1: Full-duplex 0: Half-duplex
2:1	PHY_SPEED_P4	**Port 4 PHY Speed Status** 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
0	PHY_LINKUP_P4	**Port 4 PHY Link Status** 1: Link-up 0: Link-down

00007028 PAUSE_CAP_P6_P0 MAC Pause TX/RX Capability Register for Port 6 ~ Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MAC_RXFC_P6	MAC_TXFC_P6	MAC_RXFC_P5	MAC_TXFC_P5	MAC_RXFC_P4	MAC_TXFC_P4	MAC_RXFC_P3	MAC_TXFC_P3	MAC_RXFC_P2	MAC_TXFC_P2	MAC_RXFC_P1	MAC_TXFC_P1	MAC_RXFC_P0	MAC_TXFC_P0
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	MAC_RXFC_P6	**Port 6 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
12	MAC_TXFC_P6	**Port 6 MAC Tx Pause Capability** 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
11	MAC_RXFC_P5	**Port 5 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
10	MAC_TXFC_P5	**Port 5 MAC Tx Pause Capability**

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		1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
9	MAC_RXFC_P4	**Port 4 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
8	MAC_TXFC_P4	**Port 4 MAC Tx Pause Capability** 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
7	MAC_RXFC_P3	**Port 3 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
6	MAC_TXFC_P3	**Port 3 MAC Tx Pause Capability** 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
5	MAC_RXFC_P2	**Port 2 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
4	MAC_TXFC_P2	**Port 2 MAC Tx Pause Capability** 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
3	MAC_RXFC_P1	**Port 1 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
2	MAC_TXFC_P1	**Port 1 MAC Tx Pause Capability** 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
1	MAC_RXFC_P0	**Port 0 MAC Rx Pause Capability** 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
0	MAC_TXFC_P0	**Port 0 MAC Tx Pause Capability** 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability

00007034 DBG_SIG Debug Signals 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DBG_SIG_OUT[16:16]
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SIG_OUT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	DBG_SIG_OUT	**Debug Signals** It is used to read debug output signals from internal modules, while probe_en bit is true and DBG_SIG_SEL filed is programmed.

00007038 DBGSEL0 Debug Signals Selection Group 000003FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DBG_SEL_GRP										
Type						RW										
Reset						0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
10:0	DBG_SEL_GRP	**Debug Signal Group Selection** Use it to select LED debug output signal groups of gsw_top and its sub-modules.

00007120 EEPR_IND EEPROM INDIRECT ACCESS CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EP_IND_ACT	EP_IND_WR							EP_IND_ADDR							
Type	RW	RW							RW							
Reset	0	0							0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP_IND_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	EP_IND_ACT	**EEPROM indirect access indicator** 1: EEPROM indirect access is active, and this bit is cleared by hardware after accessing is completed. 0: Not active
30	EP_IND_WR	**EEPROM indirect writing operation** 1: WRITE 0: READ
23:16	EP_IND_ADDR	**EEPROM indirect accessing address**
15:0	EP_IND_DATA	**EEPROM indirect read/write data** EP_IND_DATA[7:0] is the content of EP_IND_ADDR, while EP_IND_DATA[15:8] is for EP_IND_DATA[7:0].

00007124 EEPR_STS EEPROM STATUS REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EP_AL_DONE
Type																RO
Reset																0

Bit(s)	Name	Description
0	EP_AL_DONE	**EEPROM auto-load status indicator** 1: DONE 0: Not yet

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00007200 TICKER_CR TICKER CONFIGURATION REGISTER 0001C8FA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GSW_2X_CK_SEL
Type																RO
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TICKER800NS_CNT								TICKER1US_CNT							
Type	RW								RW							
Reset	1	1	0	0	1	0	0	0	1	1	1	1	1	0	1	0

Bit(s)	Name	Description
16	GSW_2X_CK_SEL	**gsw_2x_ck selector** 1'b1: when gsw_2x_ck = 200MHz 1'b0: otherwise
15:8	TICKER800NS_CNT	**Count to generate 800ns ticker when gsw_2x_ck_sel = 1'b0** 8'd200: gsw_2x_ck = 500MHZ 8'd160: gsw_2x_ck = 400MHZ 8'd120: gsw_2x_ck = 300MHZ 8'd80: gsw_2x_ck = 200MHZ
7:0	TICKER1US_CNT	**Count to generate 1us ticker when gsw_2x_ck_sel = 1'b0** 8'd250: when gsw_2x_ck = 500MHZ 8'd200: when gsw_2x_ck = 400MHZ 8'd150: when gsw_2x_ck = 300MHZ 8'd100: when gsw_2x_ck = 200MHZ

00007204 DELSEL_CTRL DELSEL OF SRAM CONFIGURATION REGISTER 00005555

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FL_MEM_DELSEL		PL_MEM_DELSEL		PB_MEM_DELSEL		MIB_MEM_DELSEL		VLAN_MEM_DELSEL		ADDR_MEM_DELSEL		ACL_MEM_DELSEL		TRTCM_MEM_DELSEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15:14	FL_MEM_DELSEL	**DELSEL of SRAM for Frame Link**
13:12	PL_MEM_DELSEL	**DELSEL of SRAM for Page Link**
11:10	PB_MEM_DELSEL	**DELSEL of SRAM for Packet Buffer**
9:8	MIB_MEM_DELSEL	**DELSEL of SRAM for MIB Counter**
7:6	VLAN_MEM_DELSEL	**DELSEL of SRAM for VLAN table**
5:4	ADDR_MEM_DELSEL	**DELSEL of SRAM for MAC Address table**
3:2	ACL_MEM_DELSEL	**DELSEL of SRAM for ACL table**
1:0	TRTCM_MEM_DELSEL	**DELSEL of SRAM for TRTCM table**

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00007800 HWTRAP Hardware Trap Status Register 01007FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								bond_option								
Type								RO								
Reset								1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ht_loopdet_dis	ht_p5_intf_sel	ht_smi_addr		ht_xtal_fsel		ht_p6_intf_dis	ht_p5_intf_mode	ht_p5_intf_dis	ht_c_mdio_bps_n	ht_eeprom_en	ht_chip_mode			
Type		RO	RO	RO		RO		RO	RO	RO	RO	RO	RO			
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24	bond_option	**Bonding Option** 1: Single switch mode 0: MCM mode
14	ht_loopdet_dis	**From hw_trap[14]** Hardware Loop Detection Disable 1'b0: Enable 1'b1: Disable
13	ht_p5_intf_sel	**From hw_trap[13]** Port 5 Interface Selection 1'b1: P5 Interface connects to GMAC5 1'b0: P5 Interface connects to GePHY4 or GePHY0 (depends on csr_p5_phy0_sel)
12:11	ht_smi_addr	**From hw_trap[11:10]** Chip SMI address bit 4 ~ bit 3 Note: chip_smi_addr[2:0] = 3'b111
10:9	ht_xtal_fsel	**From {hw_trap[12],hw_trap[9]}** External Crystal Frequency Selection 2'b00: 40MHz 2'b01: 20MHz 2'b11: 25MHz
8	ht_p6_intf_dis	**From hw_trap[8]** Port 6 Interface Disable 1'b0: Enable 1'b1: Disable
7	ht_p5_intf_mode	**From hw_trap[7]** Port 5 Interface Mode 1'b0: GMII/MII 1'b1: RGMII
6	ht_p5_intf_dis	**From hw_trap[5]** Port 5 Interface Disable 1'b1: Disable 1'b0: Enable
5	ht_c_mdio_bps_n	**From hw_trap[4]** 0: Directly access PHY registers via C_MDC/C_MDIO 1: Indirectly access PHY registers
4	ht_eeprom_en	**From hw_trap[2]** External EEPROM Enable 1: Enable 0: Disable
3:0	ht_chip_mode	**From {hw_trap[1],hw_trap[6],hw_trap[3],hw_trap[0]}** Chip Operation Mode[3:0] 4'b0000: IDDQ mode 4'b0001: IO TEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST mode 4'b0101: SCAN mode

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4'b0110: SCAN-COMP mode (compression)
4'b0111: SCAN-MBIST-OLT mode
4'b1000: AFE-OLT mode
4'b1001: GPHY ATE mode
4'b1010: GPHY ADUMP mode
4'b1011: GPHY ADUMP probe mode
4'b1100: Reserved
4'b1101: Reserved
4'b1110: Bootup probe mode
4'b1111: Normal mode

00007804 MHWTRAP Modified Hardware Trap Status Register 0100000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								bond_option				csr_p5_phy0_sel				csr_chg_trap
Type								RO				RW				RW
Reset								1				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_gsw_ck_sel	csr_loopdet_dis	csr_p5_intf_sel	csr_smi_addr		csr_xtal_fsel		csr_p6_intf_dis	csr_p5_intf_mode	csr_p5_intf_dis	csr_cmdio_bps_n	csr_eeprom_en	csr_chip_mode			
Type	RW	RW	RW	RO		RO		RW	RW	RW	RW	RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
24	bond_option	**Bonding Option** 1: Single switch mode 0: MCM mode
20	csr_p5_phy0_sel	**When p5_intf_sel == 1'b0, the external device will be connected to** 1'b0: GPHY4 1'b1: GPHY0
16	csr_chg_trap	**Change HW-TRAP setting** 1'b1: Change 1'b0: Use default HW-TRAP setting
15	csr_gsw_ck_sel	**Control GSW_CK (if csr_chg_trap == 1)** 1'b0: 500MHz 1'b1: 200MHz
14	csr_loopdet_dis	**Hardware Loop Detection Disable (if csr_chg_trap == 1)** 1'b0: Enable 1'b1: Disable
13	csr_p5_intf_sel	**Port 5 Interface Selection (if csr_chg_trap == 1)** 1'b1: P5 Interface connects to GMAC5 1'b0: P5 Interface connects to GePHY4 or GePHY0 (depends on csr_p5_phy0_sel)
12:11	csr_smi_addr	**csr_smi_addr is equal to ht_smi_addr[1:0] (offset: 0x7800, bit 12~11) since this hardware trap cannot be modified by software.**
10:9	csr_xtal_fsel	**csr_xtal_fsel is equal to ht_xtal_fsel[1:0](offset: 0x7800, bit 10~9)since this hardware trap cannot be modified by software.**
8	csr_p6_intf_dis	**From hw_trap[8]** Port 6 Interface Disable (if csr_chg_trap == 1) 1'b0: Enable 1'b1: Disable
7	csr_p5_intf_mode	**Port 5 Interface Mode (if csr_chg_trap == 1)** 1'b0: GMII/MII 1'b1: RGMII
6	csr_p5_intf_dis	**Port 5 Interface Disable (if csr_chg_trap == 1)** 1'b1: Disable

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		1'b0: Enable
5	csr_c_mdio_bps_n	**Directly access phy mdc (if csr_chg_trap==1)** 0: Directly access PHY registers via C_MDC/C_MDIO 1: Indirectly access PHY registers
4	csr_eeprom_en	**csr_eeprom_en is equal to ht_eeprom_en (offset: 0x7800, bit 4) since this hardware trap cannot be modified by software.**
3:0	csr_chip_mode	**csr_chip_mode is equal to ht_chip_mode[3:0] (offset: 0x7800, bit 3~0) since this hardware trap cannot be modified by software.**

00007808 TOP_SIG_CTRL_CR TOP Signals Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															csr_p5_txd7_o_sel	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								csr_intr_sig_sel								csr_ebd_phy_mdc_cken
Type								RW								RW
Reset								0								1

Bit(s)	Name	Description
17:16	csr_p5_txd7_o_sel	**2'b11 : Output INTR/LOOPDET** Otherwise : Output normal signals
8	csr_intr_sig_sel	**Output INTR or LOOPDET_ALARM** 1'b1 : Output LOOPDET_ALARM 1'b0 : Output INTR
0	csr_ebd_phy_mdc_cken	**Gating phy_mdc**

00007810 IO_DRV_CR IO Driving Strength Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							csr_normal_drv				csr_mdc_drv				csr_led_mdio_drv	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			csr_p6_data_io_drv				csr_p6_clk_io_drv				csr_p5_io_data_drv				csr_p5_io_clk_drv	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
25:24	csr_normal_drv	**For other normal PAD driving strength**
21:20	csr_mdc_drv	**P_MDC (clock probing) driving strength**
17:16	csr_led_mdio_drv	**LED and MDIO I/O driving strength**
13:12	csr_p6_data_io_drv	**P6 TXD/TXEN I/O driving strength**
9:8	csr_p6_clk_io_drv	**P6 TXC I/O driving strength**
5:4	csr_p5_io_data_drv	**P5 TXD/TXEN I/O driving strength**

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1:0	csr_p5_io_clk_drv	**P5 TXC I/O driving strength** 2'b00: 4mA 2'b10: 8mA 2'b01: 12mA 2'b11: 16mA

00007814 P5_TX_IO_DUTY_CR P5 TX IO Duty Cycle Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					csr_p5_txen_duty				csr_p5_txd3_duty				csr_p5_txd2_duty			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_p5_txd1_duty				csr_p5_txd0_duty				csr_p5_txc_duty				csr_p5_gtxc_duty			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:24	csr_p5_txen_duty	**P5 TXEN Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
23:20	csr_p5_txd3_duty	**P5 TXD[3] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
19:16	csr_p5_txd2_duty	**P5 TXD[2] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
15:12	csr_p5_txd1_duty	**P5 TXD[1] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
11:8	csr_p5_txd0_duty	**P5 TXD[0] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
7:4	csr_p5_txc_duty	**P5 TXC Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
3:0	csr_p5_gtxc_duty	**P5 GTXC Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)

00007818 P5_RX_IO_DUT P5 RX IO Duty Cycle Control Register 00000000

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Y_CR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									csr_p5_rxdv_duty				csr_p5_rxd3_duty			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_p5_rxd2_duty				csr_p5_rxd1_duty				csr_p5_rxd0_duty				csr_p5_rxc_duty			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:20	csr_p5_rxdv_duty	**P5 RXDV Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
19:16	csr_p5_rxd3_duty	**P5 RXD[3] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
15:12	csr_p5_rxd2_duty	**P5 RXD[2] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
11:8	csr_p5_rxd1_duty	**P5 RXD[1] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
7:4	csr_p5_rxd0_duty	**P5 RXD[0] Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)
3:0	csr_p5_rxc_duty	**P5 RXC Duty Cycle Adjustment** [3]: Duty L (For Output mode) [2]: Duty H (For Output mode) [1]: Duty L (For Input mode) [0]: Duty H (For Input mode)

00007820 IOTEST_Output_0 IOTEST Output Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								csr_iotest_oe	csr_iotest_out_23_0[23:16]							
Type								RW	RW							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_iotest_out_23_0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	csr_iotest_oe	**Make IOTEST mode operate in output/input mode**

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		1: Output mode 0: Input mode
23:0	csr_iotest_out_23_0	**Make IOTEST[23:0] send 1/0**

00007824 IOTEST_Output_1 IOTEST Output Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			csr_mcm_iotest_tx											csr_iotest_out_44_24[18:16]		
Type			RW											RW		
Reset			0	0	0	0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_iotest_out_44_24[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:24	csr_mcm_iotest_tx	**Make TRGMII IOTEST[5:0] send 1/0**
18:0	csr_iotest_out_44_24	**Make IOTEST[44:24] send 1/0**

00007828 IOTEST_Intput_0 IOTEST Input Record Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									csr_iotest_in_23_0[23:16]							
Type									RO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_iotest_in_23_0[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	csr_iotest_in_23_0	**Record the input of IOTEST[23:0]**

0000782C IOTEST_Intput_1 IOTEST Input Record Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			csr_mcm_iotest_rx											csr_iotest_in_44_24[18:16]		
Type			RO											RO		
Reset			0	0	0	0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_iotest_in_44_24[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:24	csr_mcm_iotest_rx	**Record the TRGMII input of IOTEST[5:0]**
18:0	csr_iotest_in_44_24	**Record the input of IOTEST[44:24]**

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00007830 P6ECR P6 Extend Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															P6_INTF_MODE	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	P6_INTF_MODE	**P6 Interface Mode** 00: RGMII mode with edge -align 01: TRGMII mode 10: RGMII mode with center-align

00007A00 TRGMII_RCK_CTRL TRGMII RXC CONTROL REGISTER 00020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_RST	RXC_DQSISEL		BSLIP_SHIFT_RXDV	BSLIP_SHIFT_RXD				PDOWN	IE_N				RXCTL_DMWTLAT		
Type	RW	RW		RW	RW				RW	RW				RW		
Reset	0	0		0	0	0	0	0	0	0				0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DQSI1_TAP								DQSI0_TAP						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_RST	**Reset of RX** 0: Reset is released. 1: Reset is asserted.
30	RXC_DQSISEL	**DQS selection for receiving RXD and RXDV** 0: DQS0 1: DQS1
28	BSLIP_SHIFT_RXDV	**Edge selection for receiving LSB of RXDV** 0: LSB is received at the rising edge. 1: LSB is received at the falling edge.
27:24	BSLIP_SHIFT_RXD	**Edge selection for receiving LSB of RXD** 0: LSB is received at the rising edge. 1: LSB is received at the falling edge.
23	PDOWN	**Power-down mode** 0: Power-down is enabled 1: Power-down is disabled
22	IE_N	**Input Enable for RXDV and RXD** 0: Input is enabled. 1: Input is disabled
18:16	RXCTL_DMWTLAT	
14:8	DQSI1_TAP	**This is the delay tap of DQSI1. To modify the delay tap, it should be increased or**

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		decreased by 1.
6:0	DQSI0_TAP	**This is the delay tap of DQSI0. To modify the delay tap, it should be increased or decreased by 1.**

00007A04 TRGMII_RCK_RTT TRGMII RXC ODT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DQS1_GATE	DQS0_GATE	RCK_RDSEL						RCK_EXIST			RCK_RTTBNJ	RCK_RTTBPJ	RCK_RTT		
Type	RW	RW	RW						RO			RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RCK_ODTN				RCK_ODTP			RCK_DRVN				RCK_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	DQS1_GATE	**Clock gating of DQS1** 0: DQS1 is disabled. 1: DQS1 is enabled.
30	DQS0_GATE	**Clock gating of DQS0** 0: DQS0 is disabled. 1: DQS0 is enabled.
29:24	RCK_RDSEL	**RX duty selection**
23	RCK_EXIST	**Clock detection of RXCLK** 0: RXCLK does not exist. 1: RXCLK exists.
20	RCK_RTTBNJ	**Termination Pull-down Base Resistor (Base NMOS) OFF control.**
19	RCK_RTTBPJ	**Termination Pull-up Base Resistor (Base PMOS) OFF control.**
18:16	RCK_RTT	**On-Die-Termination** 000: Disabled
14:12	RCK_ODTN	**Programmable termination control for linear pull-down resistor**
10:8	RCK_ODTP	**Programmable termination control for linear pull-up resistor**
7:4	RCK_DRVN	**Pull-Down Driving Strength Control**
3:0	RCK_DRVP	**Pull-Up Driving Strength Control**

00007A10 TRGMII_RD0 TRGMII RD0 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD0_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD0_ERRCNT					RD0_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To trigger a bitslip operation, this bit should be written as 1. This bit is toggled**

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		after it is written as 1. 1: Bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks, this bit should be written as 1. The comparison error is stored in ERRCNT. This bit is toggled after it is written as 1.** 1: Training comparison is performed for 16 clocks.
28	EDGE_CHK_PAT	**Training pattern selection for comparison** 0: The training pattern is the toggling pattern. 1: The training pattern is all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when the bitslip is enabled. The suggested value is 15, 0, or 1.** 0: Normal operation
23:16	RD0_WD	**This register holds the received word for RD0.**
11:8	RD0_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of the training phase, the data received are compared to the data received at the previous clock. This register holds the mismatch counter of RD0.**
6:0	RD0_TAP	**This is the delay tap of RD0. To modify the delay tap, it should be increased or decreased by 1.**

00007A14 TRGMII_RD0_RTT TRGMII RD0 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD0_DMPEDRV		RD0_DM_RDSEL						RD0_DMERODT	RD0_DMOECTL	RD0_ODTEN	RD0_DM_RTTBPJ	RD0_DM_RTTBNJ	RD0_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD0_DM_ODTN				RD0_DM_ODTP			RD0_DM_DRVN				RD0_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD0_DMPEDRV	
29:24	RD0_DM_RDSEL	**RX duty selection**
23	RD0_DMERODT	**This is the ODT setting.**
22	RD0_DMOECTL	**OE edge selection**
21	RD0_ODTEN	**When this field is enabled, the DM_RTT setting is passed to the IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD0_DM_RTTBPJ	**This is the RTT setting.**
19	RD0_DM_RTTBNJ	**This is the RTT setting.**
18:16	RD0_DM_RTT	**This is the RTT setting.**
14:12	RD0_DM_ODTN	**Programmable termination control for linear pull-down resistor**
10:8	RD0_DM_ODTP	**Programmable termination control for linear pull-up resistor**
7:4	RD0_DM_DRVN	**Pull-Down Driving Strength Control**
3:0	RD0_DM_DRVP	**Pull-Up Driving Strength Control**

00007A18 TRGMII_RD1 TRGMII RD1 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD1_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD1_ERRCNT					RD1_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To trigger a bitslip operation, this bit should be written as 1. This bit is toggled after it is written as 1.** 1: Bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks, this bit should be written as 1. The comparison error is stored in ERRCNT. This bit is toggled after it is written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: The training pattern is a toggling pattern. 1: The training pattern is an all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.** 0: Normal operation
23:16	RD1_WD	**This register holds the received word for RD1.**
11:8	RD1_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received are compared to the data received at previous clock. This register holds the mismatch counter of RD1.**
6:0	RD1_TAP	**This is the delay tap of RD1. To modify the delay tap, it should be increased or decreased by 1.**

00007A1C TRGMII_RD1_RTT TRGMII RD1 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD1_DMPEDRV		RD1_DM_RDSEL						RD1_DMERODT	RD1_DMOECTL	RD1_ODTEN	RD1_DM_RTTBPJ	RD1_DM_RTTBNJ	RD1_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD1_DM_ODTN				RD1_DM_ODTP			RD1_DM_DRVN				RD1_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD1_DMPEDRV	
29:24	RD1_DM_RDSEL	**RX duty selection**
23	RD1_DMERODT	**This is the ODT setting.**
22	RD1_DMOECTL	**OE edge selection**
21	RD1_ODTEN	**When this field is enabled, the DM_RTT setting is passed to the IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD1_DM_RTTBPJ	**This is the RTT setting.**
19	RD1_DM_RTTBNJ	**This is the RTT setting.**

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18:16	RD1_DM_RTT	**This is the RTT setting.**
14:12	RD1_DM_ODTN	**Programmable termination control for linear pull-down resistor**
10:8	RD1_DM_ODTP	**Programmable termination control for linear pull-up resistor**
7:4	RD1_DM_DRVN	**Pull-Down Driving Strength Control**
3:0	RD1_DM_DRVP	**Pull-Up Driving Strength Control**

00007A20 TRGMII_RD2 TRGMII RD2 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD2_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD2_ERRCNT					RD2_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To trigger a bitslip operation, this bit should be written as 1. This bit is toggled after written as 1.** 1: Bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks, this bit should be written as 1. The comparison error is stored in ERRCNT. This bit is toggled after it is written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: The training pattern is a toggling pattern. 1: The training pattern is an all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.** 0: Normal operation
23:16	RD2_WD	**This register holds the received word for RD2.**
11:8	RD2_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received are compared to the data received at the previous clock. This register holds the mismatch counter of RD2.**
6:0	RD2_TAP	**This is the delay tap of RD2. To modify the delay tap, it should be increased or decreased by 1.**

00007A24 TRGMII_RD2_RTT TRGMII RD2 RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD2_DMPEDRV		RD2_DM_RDSEL						RD2_DMERODT	RD2_DMOECTL	RD2_ODTEN	RD2_DM_RTTBPJ	RD2_DM_RTTBNJ	RD2_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD2_DM_ODTN				RD2_DM_ODTP			RD2_DM_DRVN				RD2_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31	RD2_DMPEDRV	
29:24	RD2_DM_RDSEL	**RX duty selection**
23	RD2_DMERODT	**This is the ODT setting.**
22	RD2_DMOECTL	**OE edge selection**
21	RD2_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD2_DM_RTTBPJ	**This is the RTT setting.**
19	RD2_DM_RTTBNJ	**This is the RTT setting.**
18:16	RD2_DM_RTT	**This is the RTT setting.**
14:12	RD2_DM_ODTN	**Programmable termination control for linear pull-down resistor**
10:8	RD2_DM_ODTP	**Programmable termination control for linear pull-up resistor**
7:4	RD2_DM_DRVN	**Pull-Down Driving Strength Control**
3:0	RD2_DM_DRVP	**Pull-Up Driving Strength Control**

00007A28 TRGMII_RD3 TRGMII RD3 CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RD3_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RD3_ERRCNT					RD3_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To trigger a bitslip operation, this bit should be written as 1. This bit is toggled after it is written as 1.** 1: Bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks, this bit should be written as 1. The comparison error is stored in ERRCNT. This bit is toggled after it is written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: The training pattern is a toggling pattern. 1: The training pattern is an all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.** 0: Normal operation
23:16	RD3_WD	**This register holds the received word for RD3.**
11:8	RD3_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received are compared to the data received at the previous clock. This register holds the mismatch counter of RD3.**
6:0	RD3_TAP	**This is the delay tap of RD3. To modify the delay tap, it should be increased or decreased by 1.**

00007A2C TRGMII_RD3_R TRGMII RD3 RTT REGISTER 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RD3_DMPEDRV		RD3_DM_RDSEL						RD3_DMERODT	RD3_DMOECTL	RD3_ODTEN	RD3_DM_RTTBPJ	RD3_DM_RTTBNJ	RD3_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD3_DM_ODTN				RD3_DM_ODTP			RD3_DM_DRVN				RD3_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RD3_DMPEDRV	
29:24	RD3_DM_RDSEL	**RX duty selection**
23	RD3_DMERODT	**This is the ODT setting.**
22	RD3_DMOECTL	**OE edge selection**
21	RD3_ODTEN	**When this field is enabled, the DM_RTT setting is passed to IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RD3_DM_RTTBPJ	**This is the RTT setting.**
19	RD3_DM_RTTBNJ	**This is the RTT setting.**
18:16	RD3_DM_RTT	**This is the RTT setting.**
14:12	RD3_DM_ODTN	**Programmable termination control for linear pull-down resistor**
10:8	RD3_DM_ODTP	**Programmable termination control for linear pull-up resistor**
7:4	RD3_DM_DRVN	**Pull-Down Driving Strength Control**
3:0	RD3_DM_DRVP	**Pull-Up Driving Strength Control**

00007A30 TRGMII_RXCTL TRGMII RXCTL CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BSLIP_EN	EDGE_CHK		EDGE_CHK_PAT	BSLIP_INIT				RXCTL_WD							
Type	RW	RW		RW	RW				RO							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RXCTL_ERRCNT					RXCTL_TAP						
Type					RO					RW						
Reset					0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BSLIP_EN	**To trigger a bitslip operation, this bit should be written as 1. This bit is toggled after it is written as 1.** 1: Bitslip is performed. The initial value is loaded.
30	EDGE_CHK	**To trigger a comparison of received data for 16 clocks, this bit should be written as 1. The comparison error is stored in ERRCNT. This bit is toggled after it is written as 1.** 1: Training comparison is performed for 16 clocks
28	EDGE_CHK_PAT	**Training pattern selection** 0: The training pattern is a toggling pattern. 1: The training pattern is an all-zero or all-one pattern.
27:24	BSLIP_INIT	**This field is the bitslip initial value loaded when bitslip is enabled. The suggested value is 15, 0, or 1.**

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		0: Normal operation
23:16	RXCTL_WD	**This register holds the received word for RXCTL.**
11:8	RXCTL_ERRCNT	**This field is cleared when EDGE_CHK is written as 1. At each clock of training phase, the data received are compared to the data received at the previous clock. This register holds the mismatch counter of RXCTL.**
6:0	RXCTL_TAP	**This is the delay tap of RXCTL. To modify the delay tap, it should be increased or decreased by 1.**

00007A34 TRGMII_RXCTL_RTT TRGMII RXCTL RTT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RXCTL_DMPEDRV		RXCTL_DM_RDSEL						RXCTL_DMERODT	RXCTL_DMOECTL	RXCTL_ODTEN	RXCTL_DM_RTTBPJ	RXCTL_DM_RTTBNJ	RXCTL_DM_RTT		
Type	RW		RW						RW	RW	RW	RW	RW	RW		
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RXCTL_DM_ODTN				RXCTL_DM_ODTP			RXCTL_DM_DRVN				RXCTL_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RXCTL_DMPEDRV	
29:24	RXCTL_DM_RDSEL	**RX duty selection**
23	RXCTL_DMERODT	**This is the ODT setting.**
22	RXCTL_DMOECTL	**OE edge selection**
21	RXCTL_ODTEN	**When this field is enabled, the DM_RTT setting is passed to the IO block.** 0: ODT is disabled. 1: ODT is enabled.
20	RXCTL_DM_RTTBPJ	**This is the RTT setting.**
19	RXCTL_DM_RTTBNJ	**This is the RTT setting.**
18:16	RXCTL_DM_RTT	**This is the RTT setting.**
14:12	RXCTL_DM_ODTN	**Programmable termination control for linear pull-down resistor**
10:8	RXCTL_DM_ODTP	**Programmable termination control for linear pull-up resistor**
7:4	RXCTL_DM_DRVN	**Pull-Down Driving Strength Control**
3:0	RXCTL_DM_DRVP	**Pull-Up Driving Strength Control**

00007A40 TRGMII_TXCTRL TRGMII TX CONTROL REGISTER 40020000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRAIN_TXEN	TXC_INV	TX_DOEO	TX_RST	TX_DOEO_Z	TX_IE_N								TX_DMWTLAT		
Type	RW	RW	RW	RW	RO	RW								RW		
Reset	0	1	0	0	0	0								0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_IO_TEST	TX_IES						
Type									RW	RW						
Reset									0	0						

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Bit(s)	Name	Description
31	TRAIN_TXEN	**In training mode, the training patterns are transmitted.** 0: The training pattern is disabled. 1: The training is enabled.
30	TXC_INV	**TXC can be generated in normal phase or inverted phase.** 0: TXC is not inverted. 1: TXC is inverted.
29	TX_DOEO	**TX can be disabled for testing purpose.** 0: TX is transmitted. 1: TX is disabled.
28	TX_RST	**Reset of TX** 0: Reset is released. 1: Reset is asserted.
27	TX_DOEO_Z	**Status of TX output Enable** 0: TX is transmitted. 1: TX is disabled.
26	TX_IE_N	**Input Enable for TXEN and TXD** 0: Input is enabled. 1: Input is disabled
18:16	TX_DMWTLAT	
7	TX_IO_TEST	**TX IO test mode** 0: TX IO test mode is enabled. 1: TX IO test mode is disabled.
6	TX_IES	**O1 Input Enable for TXEN and TXD** 0: O1 Input is enabled. 1: O1 Input is disabled

00007A50 TRGMII_TD0_CTRL TRGMII TD0 CTRL REGISTER 00000455

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DMPEDRV					TD0_DM_RTT										
Type	RW					RW										
Reset	0					0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD0_DM_SR	TD0_DMERODT	TD0_DMOECTL		TD0_TAP				TD0_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	1	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TD0_DMPEDRV	
26:24	TD0_DM_RTT	**This is the RTT setting.**
15	TD0_DM_SR	
14	TD0_DMERODT	**This is the ODT setting.**
13	TD0_DMOECTL	**OE edge selection**
11:8	TD0_TAP	**This is the delay tap of TD0. The delay tap is encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD0_TRAIN_WD	**This is the training word in training mode.**

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00007A54 TRGMII_TD0_ODT TRGMII TD0 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DM_DRVN_PRE		TD0_DM_DRVP_PRE		TD0_DM_TDSEL				TD0_ODTEN			TD0_DME_PRE	TD0_DM_DRVNT0	TD0_DM_DRVPT0	TD0_DM_DRVNTE	TD0_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD0_DM_ODTN				TD0_DM_ODTP			TD0_DM_DRVN				TD0_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD0_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD0_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD0_DM_TDSEL	
23	TD0_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TD0_DME_PRE	**This is the pre-emphasis setting.**
19	TD0_DM_DRVNT0	
18	TD0_DM_DRVPT0	
17	TD0_DM_DRVNTE	
16	TD0_DM_DRVPTE	
14:12	TD0_DM_ODTN	**This is the ODT setting.**
10:8	TD0_DM_ODTP	**This is the ODT setting.**
7:4	TD0_DM_DRVN	**This is the driving current.**
3:0	TD0_DM_DRVP	**This is the driving current.**

00007A58 TRGMII_TD1_CTRL TRGMII TD1 CTRL REGISTER 00008055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD1_DMPEDRV					TD1_DM_RTT										
Type	RW					RW										
Reset	0					0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD1_DM_SR	TD1_DMERODT	TD1_DMOECTL		TD1_TAP				TD1_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TD1_DMPEDRV	
26:24	TD1_DM_RTT	**This is the RTT setting.**
15	TD1_DM_SR	
14	TD1_DMERODT	**This is the ODT setting.**
13	TD1_DMOECTL	**OE edge selection**
11:8	TD1_TAP	**This is the delay tap of TD1. The delay tap was encoded as gray code (0, 1, 3, 2, 6,**

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		7, 5, 4, C, D, F, E, A, B, 9, 8)
7:0	TD1_TRAIN_WD	**This is the training word in training mode.**

00007A5C TRGMII_TD1_ODT TRGMII TD1 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD1_DM_DRVN_PRE		TD1_DM_DRVP_PRE		TD1_DM_TDSEL				TD1_ODTEN			TD1_DME_PRE	TD1_DM_DRVNT0	TD1_DM_DRVPT0	TD1_DM_DRVNTE	TD1_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD1_DM_ODTN				TD1_DM_ODTP			TD1_DM_DRVN				TD1_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD1_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD1_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD1_DM_TDSEL	
23	TD1_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TD1_DME_PRE	**This is the pre-emphasis setting.**
19	TD1_DM_DRVNT0	
18	TD1_DM_DRVPT0	
17	TD1_DM_DRVNTE	
16	TD1_DM_DRVPTE	
14:12	TD1_DM_ODTN	**This is the ODT setting.**
10:8	TD1_DM_ODTP	**This is the ODT setting.**
7:4	TD1_DM_DRVN	**This is the driving current.**
3:0	TD1_DM_DRVP	**This is the driving current.**

00007A60 TRGMII_TD2_CTRL TRGMII TD2 CTRL REGISTER 00008055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD2_DMPEDRV					TD2_DM_RTT										
Type	RW					RW										
Reset	0					0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TD2_DM_SR	TD2_DMERODT	TD2_DMOECTL		TD2_TAP				TD2_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TD2_DMPEDRV	
26:24	TD2_DM_RTT	**This is the RTT setting.**

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15	TD2_DM_SR	
14	TD2_DMERODT	**This is the ODT setting.**
13	TD2_DMOECTL	**OE edge select**
11:8	TD2_TAP	**This is the delay tap of TD2. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD2_TRAIN_WD	**This is the training word in training mode.**

00007A64 TRGMII_TD2_ODT TRGMII TD2 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD2_DM_DRVN_PRE		TD2_DM_DRVP_PRE		TD2_DM_TDSEL				TD2_ODTEN			TD2_DME_PRE	TD2_DM_DRVNT0	TD2_DM_DRVPT0	TD2_DM_DRVNTE	TD2_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD2_DM_ODTN				TD2_DM_ODTP			TD2_DM_DRVN				TD2_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD2_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD2_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD2_DM_TDSEL	
23	TD2_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TD2_DME_PRE	**This is the pre-emphasis setting.**
19	TD2_DM_DRVNT0	
18	TD2_DM_DRVPT0	
17	TD2_DM_DRVNTE	
16	TD2_DM_DRVPTE	
14:12	TD2_DM_ODTN	**This is the ODT setting.**
10:8	TD2_DM_ODTP	**This is the ODT setting.**
7:4	TD2_DM_DRVN	**This is the driving current.**
3:0	TD2_DM_DRVP	**This is the driving current.**

00007A68 TRGMII_TD3_CTRL TRGMII TD3 CTRL REGISTER 00008055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD3_DMPEDRV					TD3_DM_RTT										
Type	RW					RW										
Reset	0					0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD3_DMERODT	TD3_DMOECTL		TD3_TAP				TD3_TRAIN_WD							
Type		RW	RW		RW				RW							
Reset		0	0		0	0	0	0	0	1	0	1	0	1	0	1

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Bit(s)	Name	Description
31	TD3_DMPEDRV	
26:24	TD3_DM_RTT	**This is the RTT setting.**
14	TD3_DMERODT	**This is the ODT setting.**
13	TD3_DMOECTL	**OE edge selection**
11:8	TD3_TAP	**This is the delay tap of TD3. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TD3_TRAIN_WD	**This is the training word in training mode.**

00007A6C TRGMII_TD3_ODT TRGMII TD3 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD3_DM_DRVN_PRE		TD3_DM_DRVP_PRE		TD3_DM_TDSEL				TD3_ODTEN			TD3_DME_PRE	TD3_DM_DRVNT0	TD3_DM_DRVPT0	TD3_DM_DRVNTE	TD3_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD3_DM_ODTN				TD3_DM_ODTP			TD3_DM_DRVN				TD3_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TD3_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TD3_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TD3_DM_TDSEL	
23	TD3_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TD3_DME_PRE	**This is the pre-emphasis setting.**
19	TD3_DM_DRVNT0	
18	TD3_DM_DRVPT0	
17	TD3_DM_DRVNTE	
16	TD3_DM_DRVPTE	
14:12	TD3_DM_ODTN	**This is the ODT setting.**
10:8	TD3_DM_ODTP	**This is the ODT setting.**
7:4	TD3_DM_DRVN	**This is the driving current.**
3:0	TD3_DM_DRVP	**This is the driving current.**

00007A70 TRGMII_TXCTL_CTRL TRGMII TXCTL CTRL REGISTER 00008055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXCTL_DMPEDRV					TXCTL_DM_RTT										
Type	RW					RW										
Reset	0					0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TXCTL_DM_SR	TXCTL_DMERODT	TXCTL_DMOECTL		TXCTL_TAP				TXCTL_TRAIN_WD							
Type	RW	RW	RW		RW				RW							
Reset	0	0	0		0	0	0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
31	TXCTL_DMPEDRV	
26:24	TXCTL_DM_RTT	**This is the RTT setting.**
15	TXCTL_DM_SR	
14	TXCTL_DMERODT	**This is the ODT setting.**
13	TXCTL_DMOECTL	**OE edge selection**
11:8	TXCTL_TAP	**This is the delay tap of TXCTL. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**
7:0	TXCTL_TRAIN_WD	**This is the training word in training mode.**

00007A74 TRGMII_TXCTL_ODT TRGMII TXCTL ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXCTL_DM_DRVN_PRE		TXCTL_DM_DRVP_PRE		TXCTL_DM_TDSEL				TXCTL_ODTEN			TXCTL_DME_PRE	TXCTL_DM_DRVNT0	TXCTL_DM_DRVPT0	TXCTL_DM_DRVNTE	TXCTL_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TXCTL_DM_ODTN				TXCTL_DM_ODTP			TXCTL_DM_DRVN				TXCTL_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TXCTL_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TXCTL_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TXCTL_DM_TDSEL	
23	TXCTL_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TXCTL_DME_PRE	**This is the pre-emphasis setting.**
19	TXCTL_DM_DRVNT0	
18	TXCTL_DM_DRVPT0	
17	TXCTL_DM_DRVNTE	
16	TXCTL_DM_DRVPTE	
14:12	TXCTL_DM_ODTN	**This is the ODT setting.**
10:8	TXCTL_DM_ODTP	**This is the ODT setting.**
7:4	TXCTL_DM_DRVN	**This is the driving current.**
3:0	TXCTL_DM_DRVP	**This is the driving current.**

00007A78 TRGMII_TCK_CTRL TRGMII TCK CTRL REGISTER 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCK_DMPEDRV															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TCK_DM_SR	TCK_DMERODT	TCK_DMOECTL		TCK_TAP											
Type	RW	RW	RW		RW											
Reset	0	0	0		0	0	0	0								

Bit(s)	Name	Description
31	TCK_DMPEDRV	
15	TCK_DM_SR	
14	TCK_DMERODT	**This is the ODT setting.**
13	TCK_DMOECTL	**OE edge selection**
11:8	TCK_TAP	**This is the delay tap of TCK. The delay tap was encoded as gray code (0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, 8)**

00007A7C TRGMII_TCK_ODT TRGMII TCK ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCK_DM_DRVN_PRE		TCK_DM_DRVP_PRE		TCK_DM_TDSEL				TCK_ODTEN			TCK_DME_PRE	TCK_DM_DRVNT0	TCK_DM_DRVPT0	TCK_DM_DRVNTE	TCK_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TCK_DM_ODTN				TCK_DM_ODTP			TCK_DM_DRVN				TCK_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:30	TCK_DM_DRVN_PRE	**This is the pre-emphasis setting.**
29:28	TCK_DM_DRVP_PRE	**This is the pre-emphasis setting.**
27:24	TCK_DM_TDSEL	
23	TCK_ODTEN	0: ODT is disabled. 1: ODT is enabled.
20	TCK_DME_PRE	**This is the pre-emphasis setting.**
19	TCK_DM_DRVNT0	
18	TCK_DM_DRVPT0	
17	TCK_DM_DRVNTE	
16	TCK_DM_DRVPTE	
14:12	TCK_DM_ODTN	**This is the ODT setting.**
10:8	TCK_DM_ODTP	**This is the ODT setting.**
7:4	TCK_DM_DRVN	**This is the driving current.**
3:0	TCK_DM_DRVP	**This is the driving current.**

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00007B00 P5RGMIIRXCR P5 RGMII Wrapper RX Clock Control Register 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						csr_rgmii_rctl_cfg								csr_rgmii_rxd_cfg		
Type						RW								RW		
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								csr_rgmii_central_align					csr_rgmii_rxc_0deg_cfg			
Type								RW					RW			
Reset								1					0	1	0	0

Bit(s)	Name	Description
26:24	csr_rgmii_rctl_cfg	**Port 5 RGMII RX_CTRL Delay Setting** [2:0] - Delay chain setting 3'b000: No delay applied 3'b001: 1-step buffer chain applied 3'b010: 2-step buffer chain applied 3'b011: 3-step buffer chain applied 3'b100: 4-step buffer chain applied 3'b101: 5-step buffer chain applied 3'b110: 6-step buffer chain applied 3'b111: 7-step buffer chain applied
18:16	csr_rgmii_rxd_cfg	**Port 5 RGMII RXD Delay Setting** [2:0] - Delay chain setting 3'b000: No delay applied 3'b001: 1-step buffer chain applied 3'b010: 2-step buffer chain applied 3'b011: 3-step buffer chain applied 3'b100: 4-step buffer chain applied 3'b101: 5-step buffer chain applied 3'b110: 6-step buffer chain applied 3'b111: 7-step buffer chain applied
8	csr_rgmii_central_align	**1: RXC/RXD is central-aligned; RXC does not pass through the delay chain.** 0: RXC/RXD is not central-aligned (edge-aligned); RXC passes through the delay chain.
3:0	csr_rgmii_rxc_0deg_cfg	**Port 5 RGMII RXC Delay Setting for 0-degree case** [3] - Inverted RXC [2:0] - Delay chain setting 3'b000: No delay applied 3'b001: 1-step buffer chain applied 3'b010: 2-step buffer chain applied 3'b011: 3-step buffer chain applied 3'b100: 4-step buffer chain applied 3'b101: 5-step buffer chain applied 3'b110: 6-step buffer chain applied 3'b111: 7-step buffer chain applied

00007B04 P5RGMIITXCR P5 RGMII Wrapper TX Clock Control Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														csr_rgmii_txen_cfg		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_rgmii_txd_cfg						csr_rgmii_txc_cfg				
Type						RW						RW				
Reset						0	0	0				1	0	0	0	0

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Bit(s)	Name	Description
18:16	csr_rgmii_txen_cfg	**Port 5 RGMII TXD Delay Setting** [2:0] - Delay chain setting 3'b000: No delay applied 3'b001: 1-step buffer chain applied 3'b010: 2-step buffer chain applied 3'b011: 3-step buffer chain applied 3'b100: 4-step buffer chain applied 3'b101: 5-step buffer chain applied 3'b110: 6-step buffer chain applied 3'b111: 7-step buffer chain applied
10:8	csr_rgmii_txd_cfg	**Port 5 RGMII TXD Delay Setting** [2:0] - Delay chain setting 3'b000: No delay applied 3'b001: 1-step buffer chain applied 3'b010: 2-step buffer chain applied 3'b011: 3-step buffer chain applied 3'b100: 4-step buffer chain applied 3'b101: 5-step buffer chain applied 3'b110: 6-step buffer chain applied 3'b111: 7-step buffer chain applied
4:0	csr_rgmii_txc_cfg	**Port 5 RGMII TXC Delay Setting** [4] - Using 90-degree TXC (central align) [3] - Inverted RXC [2:0] - Delay chain setting 3'b000: No delay applied 3'b001: 1-step buffer chain applied 3'b010: 2-step buffer chain applied 3'b011: 3-step buffer chain applied 3'b100: 4-step buffer chain applied 3'b101: 5-step buffer chain applied 3'b110: 6-step buffer chain applied 3'b111: 7-step buffer chain applied

00007B08 P5RGMIICKCR P5 RGMII Wrapper Clock Enable Control Register 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								csr_rgmii_rxc_ckeen								csr_rgmii_txc_ckeen
Type								RW								RW
Reset								1								1

Bit(s)	Name	Description
8	csr_rgmii_rxc_cken	**Port 5 RGMII RXC Clock Enable** 1'b1: Clock Enable; 1'b0: clock Disable
0	csr_rgmii_txc_cken	**Port 5 RGMII TXC Clock Enable** 1'b1: Clock Enable; 1'b0: clock Disable

00007D00 LED_EN LED I/O function enable 00077777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_EN		

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Type														RW		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_EN				P2_LED_EN				P1_LED_EN				P0_LED_EN		
Type		RW				RW				RW				RW		
Reset		1	1	1		1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
18:16	P4_LED_EN	**P4 LED I/O Enable** P4_LED_EN[2] for P4 LED #2 P4_LED_EN[1] for P4 LED #1 P4_LED_EN[0] for P4 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
14:12	P3_LED_EN	**P3 LED I/O Enable** P3_LED_EN[2] for P3 LED #2 P3_LED_EN[1] for P3 LED #1 P3_LED_EN[0] for P3 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
10:8	P2_LED_EN	**P2 LED I/O Enable** P2_LED_EN[2] for P2 LED #2 P2_LED_EN[1] for P2 LED #1 P2_LED_EN[0] for P2 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
6:4	P1_LED_EN	**P1 LED I/O Enable** P1_LED_EN[2] for P1 LED #2 P1_LED_EN[1] for P1 LED #1 P1_LED_EN[0] for P1 LED #0 For individual LED 1'b0: Disable 1'b1: Enable
2:0	P0_LED_EN	**P0 LED I/O Enable** P0_LED_EN[2] for P0 LED #2 P0_LED_EN[1] for P0 LED #1 P0_LED_EN[0] for P0 LED #0 For individual LED 1'b0: Disable 1'b1: Enable

00007D04 LED_IO_MODE LED I/O Mode 00077777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_MODE		
Type														RW		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_MODE				P2_LED_MODE				P1_LED_MODE				P0_LED_MODE		
Type		RW				RW				RW				RW		
Reset		1	1	1		1	1	1		1	1	1		1	1	1

Bit(s)	Name	Description
18:16	P4_LED_MODE	**P4 LED I/O Mode** P4_LED_MODE[2] for P4 LED #2 P4_LED_MODE[1] for P4 LED #1 P4_LED_MODE[0] for P4 LED #0

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		For individual LED Mode 1'b0: GPIO 1'b1: LED
14:12	P3_LED_MODE	**P3 LED I/O Mode** P3_LED_MODE[2] for P3 LED #2 P3_LED_MODE[1] for P3 LED #1 P3_LED_MODE[0] for P3 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
10:8	P2_LED_MODE	**P2 LED I/O Mode** P2_LED_MODE[2] for P2 LED #2 P2_LED_MODE[1] for P2 LED #1 P2_LED_MODE[0] for P2 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
6:4	P1_LED_MODE	**P1 LED I/O Mode** P1_LED_MODE[2] for P1 LED #2 P1_LED_MODE[1] for P1 LED #1 P1_LED_MODE[0] for P1 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED
2:0	P0_LED_MODE	**P0 LED I/O Mode** P0_LED_MODE[2] for P0 LED #2 P0_LED_MODE[1] for P0 LED #1 P0_LED_MODE[0] for P0 LED #0 For individual LED Mode 1'b0: GPIO 1'b1: LED

00007D08 LED_HW_MODE LED Hardware Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_HW_MODE		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_HW_MODE				P2_LED_HW_MODE				P1_LED_HW_MODE				P0_LED_HW_MODE		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
18:16	P4_LED_HW_MODE	**P4 LED Hardware Mode** For individual LED 1'b0: Open-Drain 1'b1: Push-Pull
14:12	P3_LED_HW_MODE	**P3 LED Hardware Mode** For individual LED 1'b0: Open-Drain 1'b1: Push-Pull
10:8	P2_LED_HW_MODE	**P2 LED Hardware Mode** For individual LED 1'b0: Open-Drain 1'b1: Push-Pull
6:4	P1_LED_HW_MODE	**P1 LED Hardware Mode** For individual LED 1'b0: Open-Drain 1'b1: Push-Pull

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2:0	P0_LED_HW_MODE	**P0 LED Hardware Mode** For individual LED 1'b0: Open-Drain 1'b1: Push-Pull

00007D0C LED_SRC LED Source Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														P4_LED_SRC_SEL		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		P3_LED_SRC_SEL				P2_LED_SRC_SEL				P1_LED_SRC_SEL				P0_LED_SRC_SEL		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
18:16	P4_LED_SRC_SEL	**P4 LED Source Selection** For individual LED 1'b0: P4 PHY 1'b1: Hardware Loop Detect Alarm of P4. When P4 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P4 PHY.
14:12	P3_LED_SRC_SEL	**P3 LED Source Selection** For individual LED 1'b0: P3 PHY 1'b1: Hardware Loop Detect Alarm of P3. When P3 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P3 PHY.
10:8	P2_LED_SRC_SEL	**P2 LED Source Selection** For individual LED 1'b0: P2 PHY 1'b1: Hardware Loop Detect Alarm of P2. When P2 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P2 PHY.
6:4	P1_LED_SRC_SEL	**P1 LED Source Selection** For individual LED 1'b0: P1 PHY 1'b1: Hardware Loop Detect Alarm of P1. When P1 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P1 PHY.
2:0	P0_LED_SRC_SEL	**P0 LED Source Selection** For individual LED 1'b0: P0 PHY 1'b1: Hardware Loop Detect Alarm of P0. When P0 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P0 PHY.

00007E00 GLB_PRB_CR Global Probing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PRB_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														GLB_PRB_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
16	PRB_MODE	**Probe Mode Enable** 1'b0: Probe Mode Disable; Normal Mode

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		1'b1: Probe Mode Enable
2:0	GLB_PRB_SEL	**Global Signal Probing Selector** 3'b000: Top Layer 3'b001: Switch IP 3'b010: GePHY IP 3'b011: FePHY IP 3'b100: TRGMII MACRO 3'b101: RGMII Wrapper

00007E04 GLB_PRB_SR Global Probing Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GLB_PRB_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GLB_PRB_STS	**Global Probing Status Register** This register shows the results of global probing

00007E10 TOP_PRB_CR TOP Probing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TOP_PRB_SEL				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TOP_PRB_SEL	**TOP Signal Probing Selector**

00007E14 TOP_PRB_SR TOP Probing Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_PRB_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_PRB_STS	**TOP Probing Status Register** This register shows the results of top (circuits outside switch and phy IPs) probing

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00007E20 TRGMII_PRB_CR TRGMII Probing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												TRGMII_PRB_SEL				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TRGMII_PRB_SEL	**TRGMII MACRO Signal Probing Selector**

00007E24 TRGMII_PRB_SR TRGMII Probing Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	TRGMII_PRB_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRGMII_PRB_STS	**TRGMII MACRO Probing Status Register** This register shows the results of TRGMII MACRO probing

00007E30 RGMII_PRB_CR RGMII Probing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												RGMII_PRB_SEL				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RGMII_PRB_SEL	**RGMII Wrapper Signal Probing Selector**

00007E34 RGMII_PRB_SR RGMII Probing Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGMII_PRB_STS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RGMII_PRB_STS	**RGMII Wrapper Probing Status Register** This register shows the results of RGMII Wrapper probing

00007FFC CREV Chip Revision 75300001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHIP_NAME															
Type	RO															
Reset	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CHIP_REV			
Type													RO			
Reset													0	0	0	1

Bit(s)	Name	Description
31:16	CHIP_NAME	**Chip Name**
3:0	CHIP_REV	**Chip Revision**

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