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5 **Characterization of a high bandwidth readout chain for the**  
6 **CMS Phase-2 pixel upgrade**

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11 **ABSTRACT:** The CMS collaboration is building a new inner tracking pixel detector for the High-  
12 Luminosity LHC. Each pixel readout chip will be controlled with a single serial input stream at  
13 160 **Mb/s** and will send out data via four current mode logic (CML) 1.28 **Gb/s** outputs. The readout  
14 chips will be grouped in modules and connected with up to 1.6 **meters** long low-mass electrical  
15 links to Low-Power Gigabit Transceivers (IpGBT) and Versatile Link PLUS Transceiver (VTRx+)  
16 modules that send the data optically to off-detector electronics at 10 **Gb/s**. **The characterization of**  
17 **these components and system tests of the readout chain are presented.**

18 **KEYWORDS:** Front-end electronics for detector readout, optical detector readout concepts, radiation-  
19 hard electronics

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## 27 **1 Introduction**

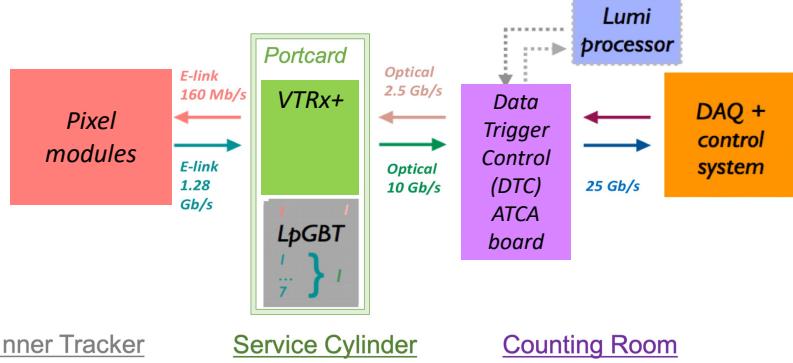
28 In preparation for the High-Luminosity LHC (HL-LHC) [1], the CMS Tracker will be fully replaced  
29 in the Phase-2 upgrade [2–4]. The new inner tracker will have about two billion silicon pixels  
30 installed, and hybrid pixel modules will process sensor data using a custom readout chip initially  
31 developed by the RD53 collaboration [5]. Each readout chip on the detector needs a control link to  
32 receive trigger, clock, commands, and settings from off-detector electronics as well as data links to  
33 send pixel data to off-detector electronics. The high bandwidth control and data links are split into  
34 two stages: electrical links and optical links. System tests of these electrical and optical links are  
35 presented.

## 36 **2 Data Readout Chain**

37 An overview of the data readout chain for the inner tracker is shown in Figure 1. High bandwidth  
38 electrical and optical links are used to establish control and data links between pixel modules on the  
39 CMS detector and Data Trigger Control (DTC) boards in the counting room. Low-mass electronic  
40 links (e-links) up to 1.6 meters long provide 160 Mb/s control links (downlinks) and 1.28 Gb/s  
41 data links (uplinks) between pixel modules and portcards. Optical fibers connect portcards, which  
42 are mounted on the support structure inside the detector, to DTC boards in the counting room to  
43 establish 2.5 Gb/s control links (downlinks) and 10 Gb/s data links (uplinks). The portcards each  
44 carry three Low-Power Gigabit Transceivers (lpGBT) [6] and three Versatile Link PLUS Transceiver  
45 (VTRx+) modules [7]. The lpGBTs communicate with the pixel modules via electrical links, and  
46 the VTRx+ modules establish optical links with the DTC boards.

## 47 **3 Electrical Links**

48 The electrical link (e-link) bundles are created using low mass, small diameter twisted pair cables.  
49 One end of a twisted pair electrical link bundle is shown in Figure 2. E-link bundles are made to



**Figure 1.** System readout architecture for the inner tracker [4]. Pixel modules communicate with portcards through e-links. Portcards communicate with Data Trigger Control (DTC) boards through optical links.

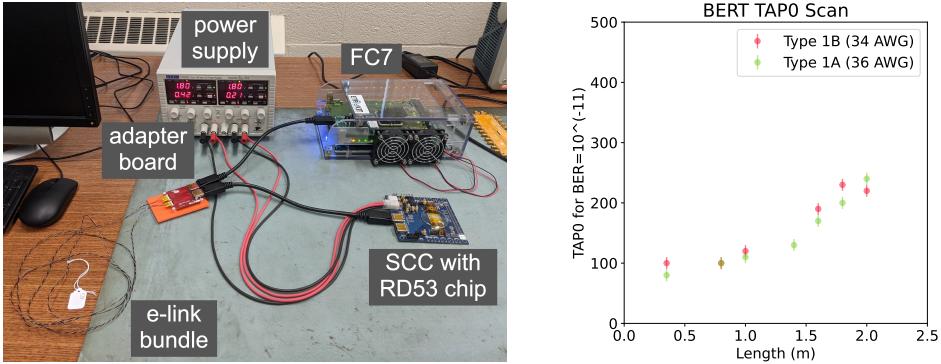
50 connect to modules and provide each module with one control link twisted pair and multiple data  
 51 link twisted pairs. Each twisted pair is produced using two 36 American Wire Gauge (AWG) copper  
 52 core ( $127 \mu\text{m}$  in diameter) wires surrounded by polyimide insulation ( $45 \mu\text{m}$  thick) that are twisted  
 53 together with 4 twists per inch. The pairs are soldered to small,  $20 \mu\text{m}$  thick PCBs that can plug into  
 54 Molex connectors with  $300 \mu\text{m}$  pitch [8]. To improve durability and handling, the soldered wires  
 55 are secured with a non-conductive epoxy, and then the bundle is lashed together using polyimide  
 56 braiding.



**Figure 2.** One end of an electrical link (e-link) bundle that has five twisted pair channels: one channel for a control link and four channels for data readout.

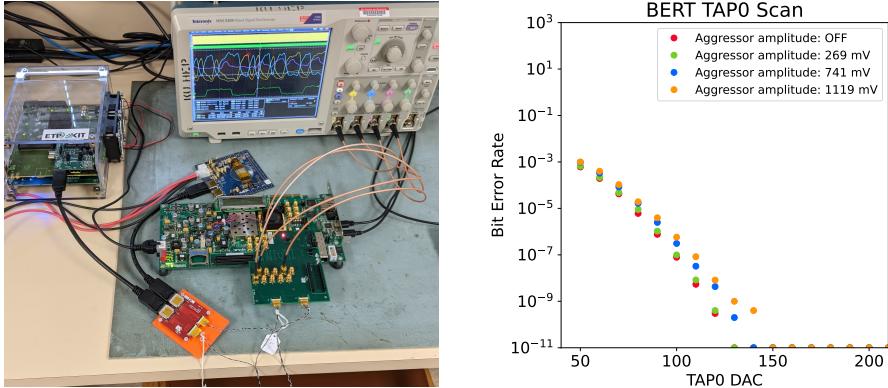
57 Prototype low-mass electrical links are characterized using a series of measurements. The  
 58 signal quality is assessed using eye diagrams, which overlay transitions between binary states from  
 59 repeated measurements of the signal over a time interval. Bit error rate scans are used to characterize  
 60 signal integrity across e-links. Cross talk effects from channels within an e-link bundle (internal)  
 61 and from multiple bundles (external) are studied.

62 In one system test of the e-links, an RD53 chip on a Single Chip Card (SCC) is read out over  
 63 e-links using an FC7 mezzanine card [9], as shown in Figure 3. E-links of two gauges (34 and  
 64 36 AWG) and different lengths (from 0.35 to 2.0 meters) are used in the readout chain. Bit error  
 65 rates are determined using a pseudorandom binary sequence (PRBS) that is sent at  $1.28 \text{ Gb/s}$  from  
 66 the RD53 chip to the FC7 mezzanine card. The amplitude of the PRBS signal is varied using the  
 67 “TAP0” pre-emphasis digital-to-analog converter (DAC) setting, which controls the amplitude of  
 68 the signal output by the current mode logic (CML) driver on the RD53 chip. For this test, the  
 69 amplitude is increased until the bit error rate of  $10^{-11}$  is reached. Longer e-links require a larger  
 70 signal amplitude to maintain a given bit error rate. Good performance is seen for e-links up to  
 71 2.0 meters.



**Figure 3.** Measurement of signal amplitudes (set by TAP0) on e-links for a fixed bit error rate. In the hardware setup (left), an FC7 mezzanine card is connected to an SCC through two commercial display port cables, an adapter board, and an e-link **bundle** for control and readout of an RD53 chip. The measurements (right) show the TAP0 setting to achieve a bit error rate of  $10^{-11}$  for e-links of different lengths and gauges.

Furthermore, an external crosstalk measurement for **e-link bundles** was performed, and the results are shown in Figure 4. To mitigate the effect of external crosstalk from a large aggressor amplitude, the victim amplitude set by TAP0 only requires a small increase. Thus, external crosstalk from the single aggressor e-link **bundle** has a small effect on readout over the victim e-link **bundle**.

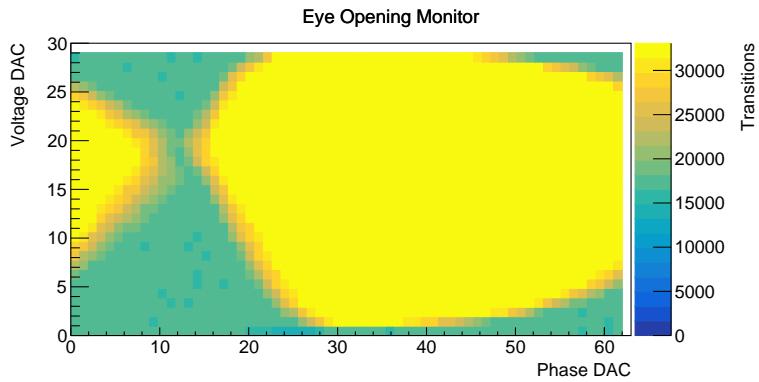


**Figure 4.** Measurement of the effect of external crosstalk on data transmission across e-link **bundles**. Two e-link **bundles** (1.4 meters, 36 AWG) are twisted together (left), with a victim e-link **bundle** connected between an FC7 mezzanine card and SCC to read from an RD53 chip, and an aggressor e-link **bundle** connected to a KC705. The KC705 sends PRBS signals on four e-link channels on the aggressor at different amplitudes.

Radiation testing was performed to determine if e-links can maintain performance after receiving up to 1500 Mrad. Two different epoxies, Araldite 2011 (Ref. [10]) and UR6060 (Ref. [11]), were used for e-links that underwent radiation testing. For doses up to 1300 Mrad, the Araldite 2011 epoxy showed significant darkening, while the UR6060 epoxy remained transparent. The signal integrity on e-links remained good after radiation doses. The polyimide braiding used for lashing becomes brittle after 1900 Mrad, but this should not affect the electrical readout.

82 **4 Portcards**

83 The portcards convert electrical signals from on-detector readout chips to optical signals for off-  
84 detector DTC boards (see Figure 1). Dedicated setups with the portcards reading out SCCs with  
85 short coaxial cables have been used to test the prototype portcards and validate the optical part of  
86 the readout chain. In one measurement of the optical links, the high-speed input to the lpGBT is  
87 compared to a 5-bit adjustable constant voltage by a comparator sampled with a phase interpolated  
88 clock. Transitions of the comparator are counted; within the eye the output should toggle, but  
89 above or below the eye, no transitions are expected. The data from this measurement are shown in  
90 Figure 5. The high toggle count region is large, corresponding to a large eye diagram and a strong  
91 optical signal.

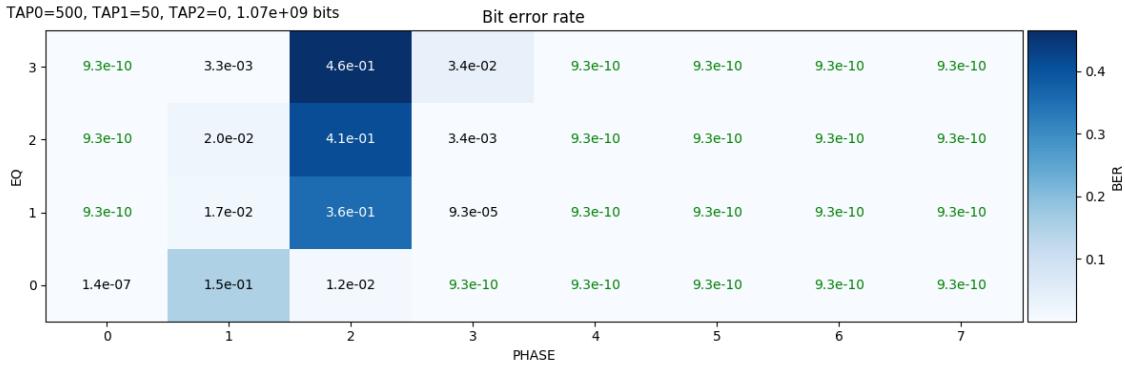


**Figure 5.** Eye opening monitor from an lpGBT for the 2.56 Gb/s optical down link with equalization parameters at default settings. The vertical axis is a 5-bit encoded voltage threshold, and the horizontal axis is a 6-bit encoded sampling phase. The color scale shows the number of transitions (toggle count). Regions with high toggle count correspond to the eye opening.

92 In addition, the electrical link receivers on the lpGBT are being studied. In one measurement,  
93 the signal source is a PRBS7 generator in the RD53 readout chip. This signal is sent over a  
94 commercial display port cable, an adapter board, and a [commercial](#) Molex FPC cable (Ref. [12]) to  
95 be received by an lpGBT. The signal is compared to an internal error checker on the lpGBT. The  
96 [bit error](#) rate is measured as a function of clock sampling phase and equalization setting, and the  
97 results are provided in Figure 6. The region with a bit error rate of  $9.3 * 10^{-10}$  corresponds to zero  
98 errors for the total number of bits checked ( $1.07 * 10^9$ ). Low error rates on the lpGBT electrical  
99 link receivers are achieved by tuning the sampling phase, and changing the equalization setting has  
100 only a small effect on the timing.

101 **5 Conclusion**

102 Various system tests have been performed to characterize the electrical and optical links forming the  
103 readout chain for the CMS Phase-2 pixel upgrade. Electrical links can provide stable connectivity  
104 at the required lengths, and crosstalk has a small effect on signal quality. Conversion from electrical  
105 to optical links is working well, and the optical links have good performance. These results form



**Figure 6.** Scan of bit error rate vs. clock sampling phase and equalization setting for electrical port receivers on the lpGBT driven by the RD53 pixel readout chip. The number of bits checked at each setting is  $1.07 * 10^9$ . Points in green have zero observed errors and report  $9.3 * 10^{-10}$ , which is the reciprocal of the number of bits checked.

106 an important input to the final design, production, and testing of components for the pixel detector  
107 readout chain.

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