TITLE: Digital Circuit of 2-bit two binary adder

Introduction:

The objective of this exercise is to design, simulate and document a digital circuit that implements the functionality of a 2-bit binary adder basic digital logic gates.

Abstract:

The digital circuit adds two 2-bit binary numbers and produces a 3-bit output (including the carry-out bit). It consists of two half-adders and one OR gate to handle the carry bits. It examines the performance of a 2-bit binary adder using a digital logic simulator. The simulation tested various input combinations to analyze the output and carry out bit. The results show that the circuit has been well constructed due to the results corresponding to the truth table.

Truth Table:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 |

Output Equations:

S0 = A0’B0A1’B1’ + A0’B0A1’B1 + A0’B0A1B1’ + A0’B0A1B1 + A0B0’A1’B1’ + A0B0’A1’B1 +AOB0’A1B1’ + A0B0’A1B1

S0 = A0’B0 (A1’B1’ + A1’B1 + A1B1’ + A1B1) + A0B0’ (A1’B1’ + A1’B1 + A1B1’ + A1B1)

S0 = A0’B0(A1’ (B1’ + B1) + A1(B1’ + B1)) + A0B0’ (A1’ (B1’ + B1) + A1 (A1 + B1))

S0 = A0’B0 + A0B0’

S0 = A0 XOR B0

S1 =A0’ B0’ A1’B1 + A0’ B0’ A1 B1’ + A0’ B0 A1’ B1 + A0’ B0A1 B1’ + A0B0’ A1’B1 + A0 B0’ A1 B1’ + A0 B0 A1’B1’ + A0 B0 A1B1

= (B0’ A1 B1’ + B0’ A1’ B1) (A0 + A0’) + B0(A0’ (A1’ B1 + A1 B1’) + A0 (A1’B1’ + A1B1)

= (B0’ A1 B1’ + B0’ A1’ B1) (A0 + A0’) + B0(A0’ ((A1 XOR B1))) + A0(A1’ B1’ + A1B1)

= B0’ A1 B1’ + B0’ A1’ B1 + B0(A0’ ((A1 XOR B1))) + A0 (A1 XOR B1)’

= B0’ A1 B1’ + B0’ A1’ B1 + B0 (A0 XOR A1 XOR B1)

= B0’(A1 XOR B1 ) + B0 ( A0 XOR A1 XOR B1)

COUT = A0’ B0’ A1B1 + A0’ B0 A1B1 + A0B0’ A1B1 + A0 B0 A1’ B1 + A0 B0 A1 B1’ + A0 B0 A1B1

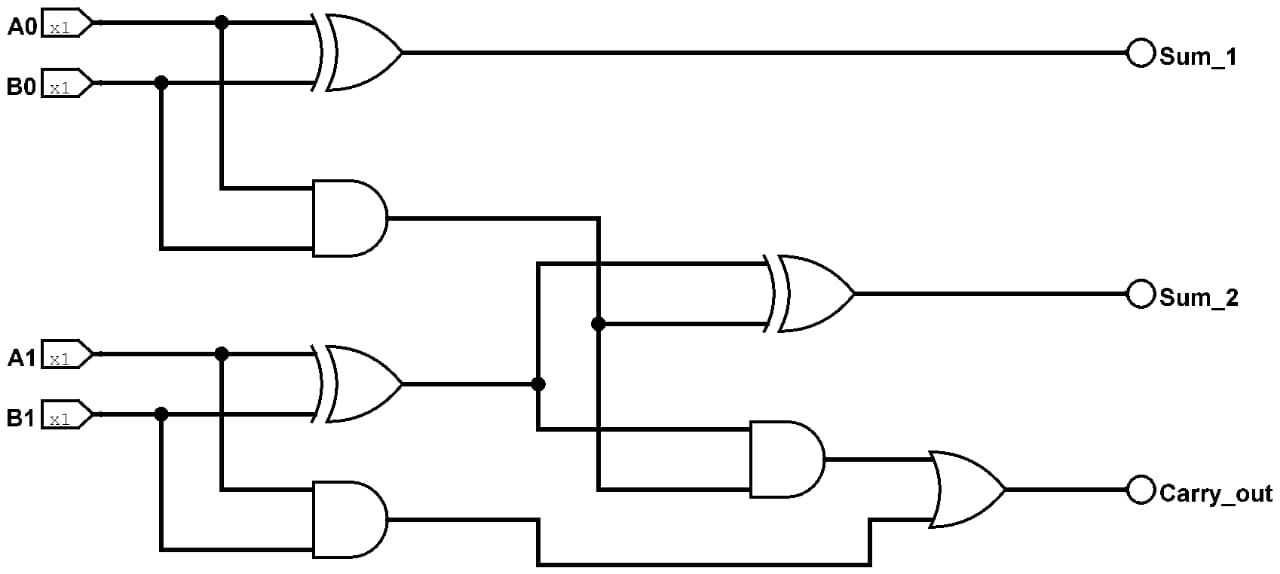
=(B0’ A1B1 + B0 A1B1) (A0’ + A0) + A0 B0 A1’ B1 + A0 B0 A1 B1’

= B0’ A1B1 + B0 A1B1 + A0 B0 (A1’ B1 + A1 B1’)

= A1B1(B0’ + B0) + A0 B0 (A1 XOR B1)

= A1B1 + A0 B0 (A1 XOR B1)

CIRCUIT SCHEMA:



Conclusion:

Logism software tool was used to verify the correctness of the circuit via simulation. All possible inputs were implemented to verify whether the combination gives theoretical output. And this was achieved through the use of LEDs. The sums and carry-output turned LED on for a 1 and off for a 0 bit which made it easier the spot whether the output corresponds to the input. Being familiar with the logism software was a bit demanding especially on the decision of which correct components to use, being components that display the output, but fortunately a similar problem was encountered throughout our research and that eventually made it easier to figure out the solution.

Group Members

1. Mathetsa , Toka: 202201083
2. Ralekoata, Hlompho Edwn: 202201073
3. Aarone, Mamello Emmanuel : 202004556
4. Chefa, Tsepiso Joseph: 202100088
5. Seala, Mamoitheri M : 202201078
6. Mohapi, Hlalefang : 201700822