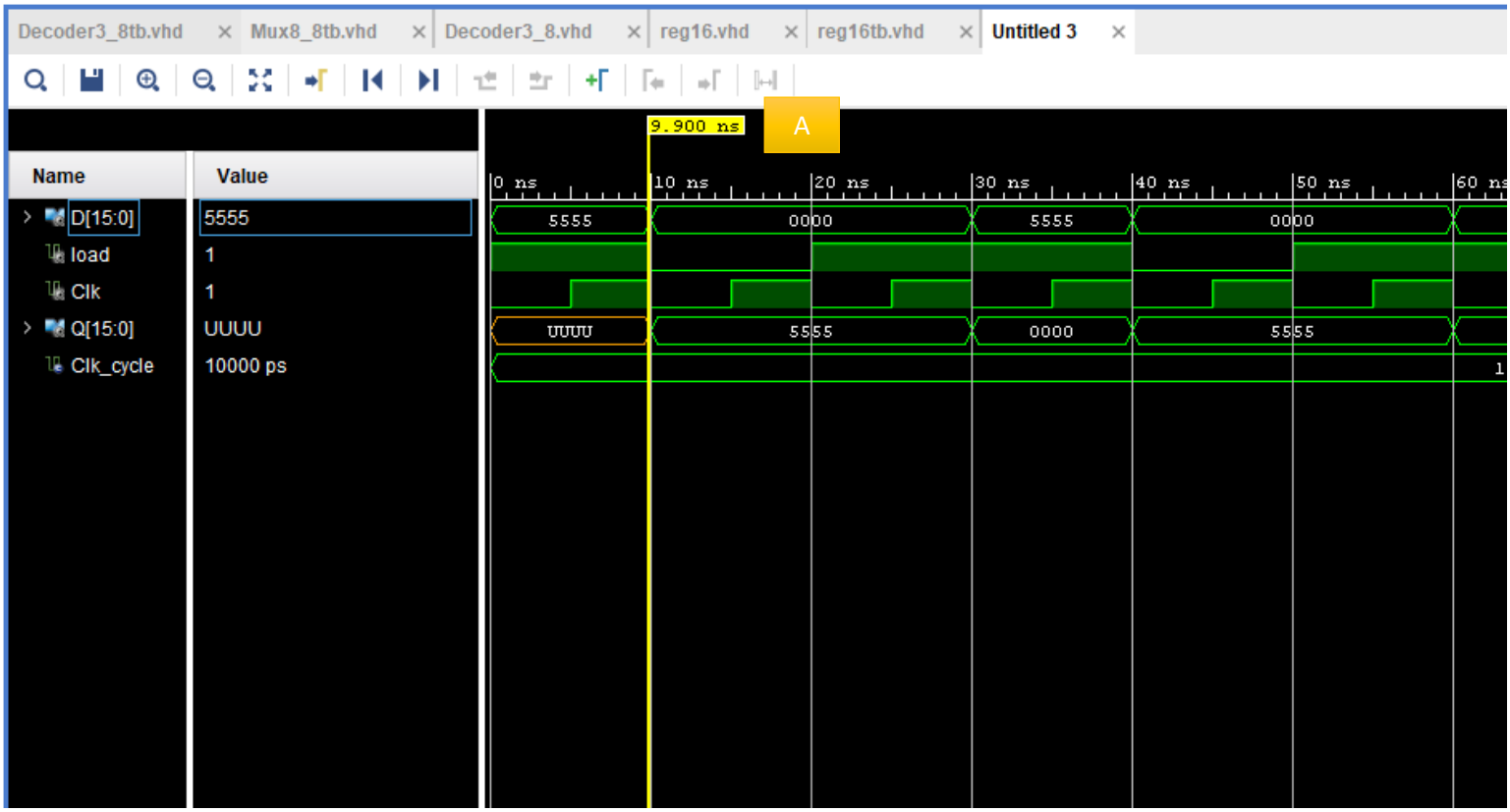
CS2022 Computer Architecture

Project 1 – Datapath Design Part A

Name: Caleb Teo
Student Number: 15324741

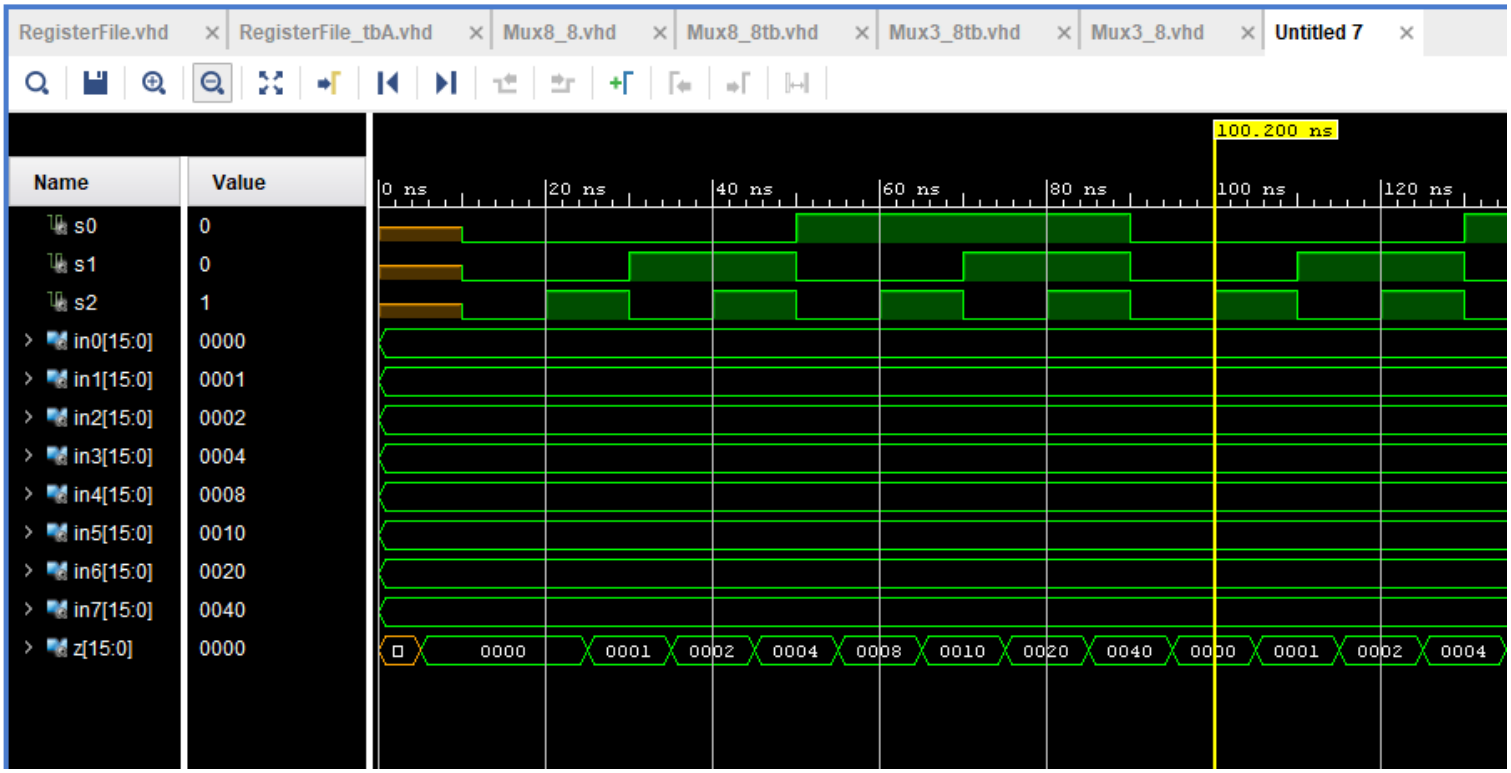
1 SINGLE REGISTER – REG16.VHD



A

At A we can see that the output ‘Q’ remains the “5555” even though the input ‘D’ is “0000”. This is because load is ‘0’ which means that the register output does not change to “0000”. Only at 30ns does the output ‘Q’ change to “0000” when load is ‘1’.

2 MULTIPLEXER – MUX_8_8.VDH



We can see that for the Multiplexer 8 register and 16 bits, which the output ‘z’ changes from the input ‘in0’ – ‘in7’. We know that it is correct from the example at 100,200ns. At 100,200ns we can see that ‘s0’ = 0, ‘s1’ = 0, ‘s2’ = 1, which will give us the output ‘z’ will be ‘in1’ and that can be confirmed after 5ns ‘z’ changes from 0000 to 0001. This is correct as 001 maps to in1.

3 MULTIPLEXER – MUX3_8.VDH

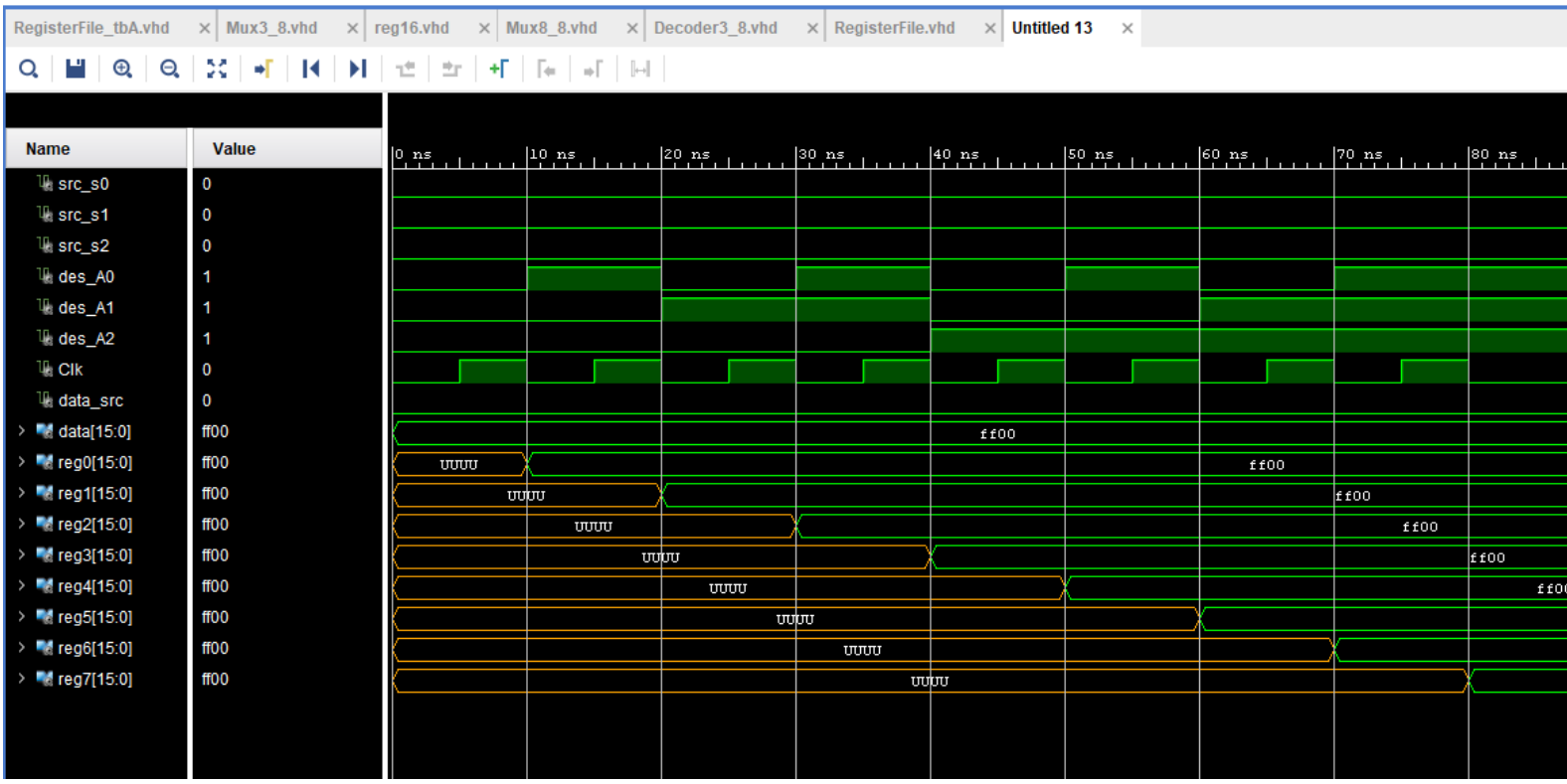
From the Mu3_8 at 30ns we can see that the output ‘z’ = “ff00”. This changes as the select, ‘s’ = 0 and after 5ns (at 35.20ns) that the output ‘z’ = “00ff” which is ‘In0’. We can see that it changes back to “ff00” as the ‘s’ changes to 1. This is correct as s = 0 maps to In0 and s = 1 maps to In1.

4 DECODER – DECODER3_8.VDH

We can see that the Decoder is selecting the output ‘D0’ – ‘D7’ to be either 0 or 1 depending on ‘A0’ – ‘A2’. For example at 60.10ns, we can see that the value of ‘A0’ = 0, ‘A1’ = 1 and ‘A2’ = 1. After 5ns the output ‘D5’ changes to 0 and ‘D6’ changes to 1. This is correct as 110 maps to D6.

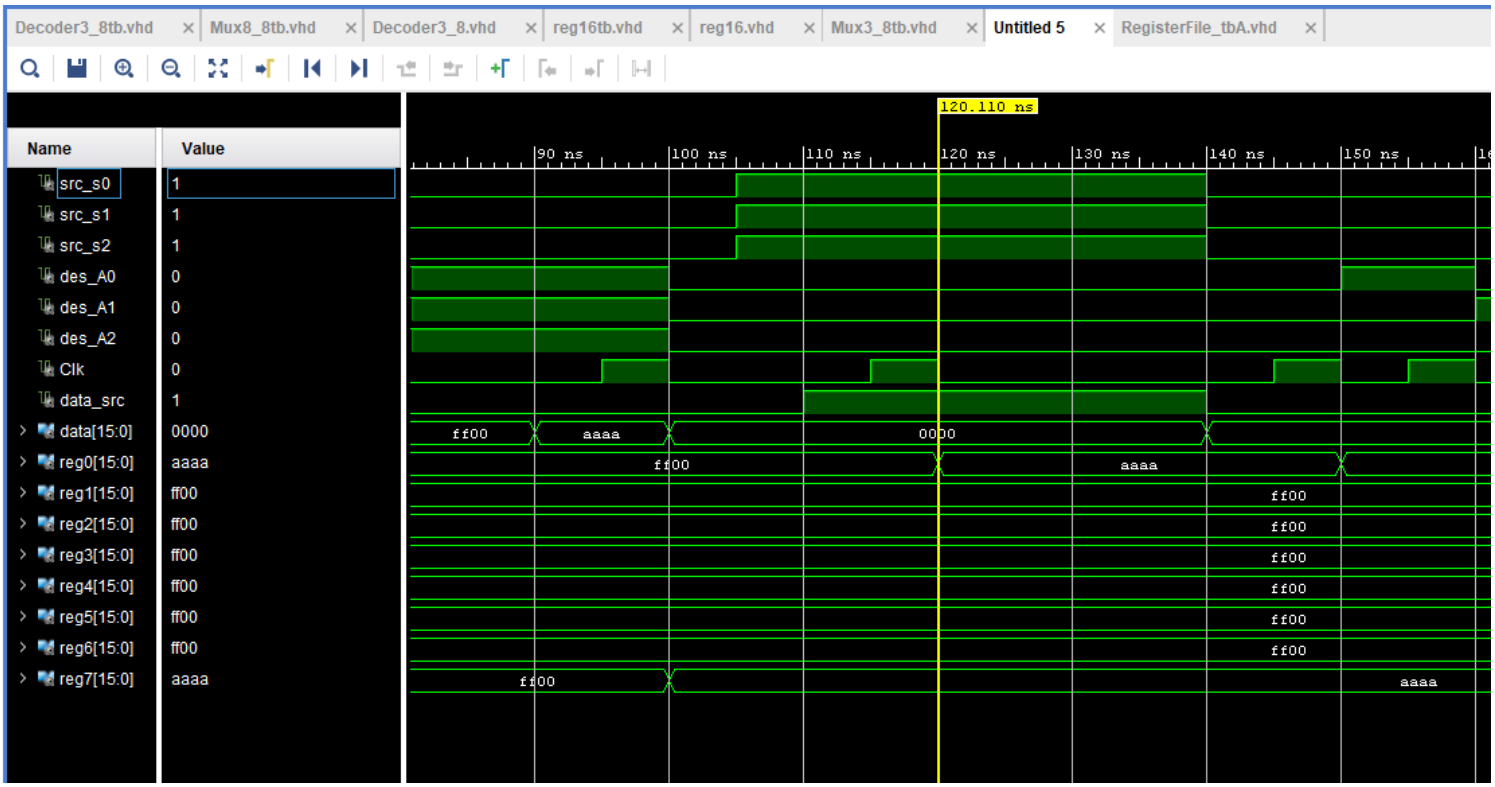
5 REGISTER FILE – REGISTERFILE.VDH

5.1 LOADING AN ARBITRARY HEX VALUE TO ALL REGISTER.



From the above test bench, we can see that each register is loaded with the data from the Mux3_8 which is “ff00”. We can see this is being done with the ‘des_A0’, ‘des_A1’ and ‘des_A2’ as they change to enable the load for each register.

5.2 REGISTER FILE TRANSFER FROM REG7 TO REG0



In the test bench image above, we can see that the value of reg7 = “aaaa” and the data = “0000” after 100ns. We can then see the register transfer from reg7 to reg0 at 120ns. We can see that using the ‘data_src’ = 1 means that reg7 transfer its output to reg0.