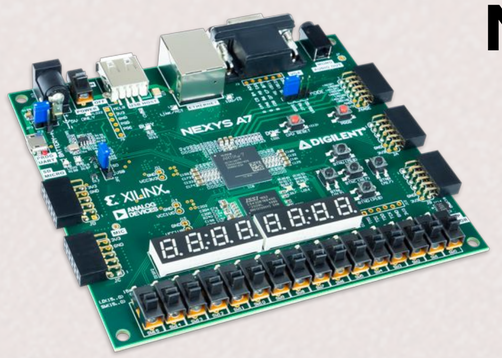
# FPGA ALARM CLOCK IMPLEMENTED USING VERILOG

**By: Kyle Acosta, Jimmy Luu, Rob Ranit, Jeff Tang**

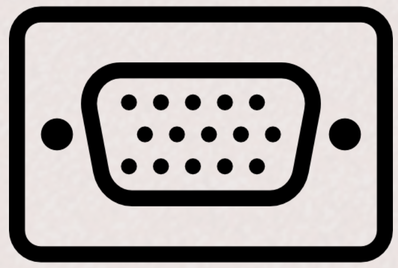
# Significance:

This FPGA-based Smart Alarm Clock project not only showcases the seamless integration of advanced features using Xilinx Vivado and Nexys A7-100T but also underscores the significance of precise version control and hardware programming methodologies. The alarm clocks incorporates innovative features, including LEDs and a switch for dynamic input control. These features provide users with a holistic wake-up solution, emphasizing user customization with load number LEDs and up counter indicators.




**Made on a Nexys A7-100t FPGA**

**24-hour alarm clock with loading**



**VGA display on an analog monitor**

**PWM implementation through RGB LEDs**