FPGA-Based Smart Alarm Clock: ECE 3300 Final Project

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Title: FPGA-Based Smart Alarm Clock: Innovations in Embedded Systems for Enhanced Wake-Up Experiences

Abstract:

This project showcases the successful development of an advanced FPGA-based smart alarm clock, representing the culmination of collaborative efforts within the ECE 3300 course. Leveraging the capabilities of Xilinx Vivado ML Edition (2023.1) software and implemented on the Nexys A7-100T FPGA board, our project introduces significant advancements in hardware integration, coding proficiency, and user-centric design.

The Clock module, a pivotal component, showcases refined features including a 24-hour display with precise timekeeping capabilities. Iterative enhancements, such as a revamped minute counter, expanded hour display (00-23), and an optimized loading mechanism, contribute to the project's commitment to achieving precision and functionality.

Simultaneously, the completed Alarm module incorporates innovative features, including LEDs and a switch for dynamic input control. Integrated into the comprehensive AlarmClock module, these features provide users with a holistic wake-up solution, emphasizing user customization with load number LEDs and up counter indicators.

Our version-controlled repository ensures efficient tracking of changes across three distinct components: Alarm, Clock, and the Combined AlarmClock. The adoption of Verilog as the coding language underscores our commitment to meticulous hardware-level programming, establishing a versatile foundation for future FPGA applications.

In summary, this FPGA-based Smart Alarm Clock project not only showcases the seamless integration of advanced features using Xilinx Vivado and Nexys A7-100T but also underscores the significance of precise version control and hardware programming methodologies. Our submission contributes to the discourse on embedded systems, highlighting successful innovations in FPGA technology for a more personalized and intelligent wake-up experience.