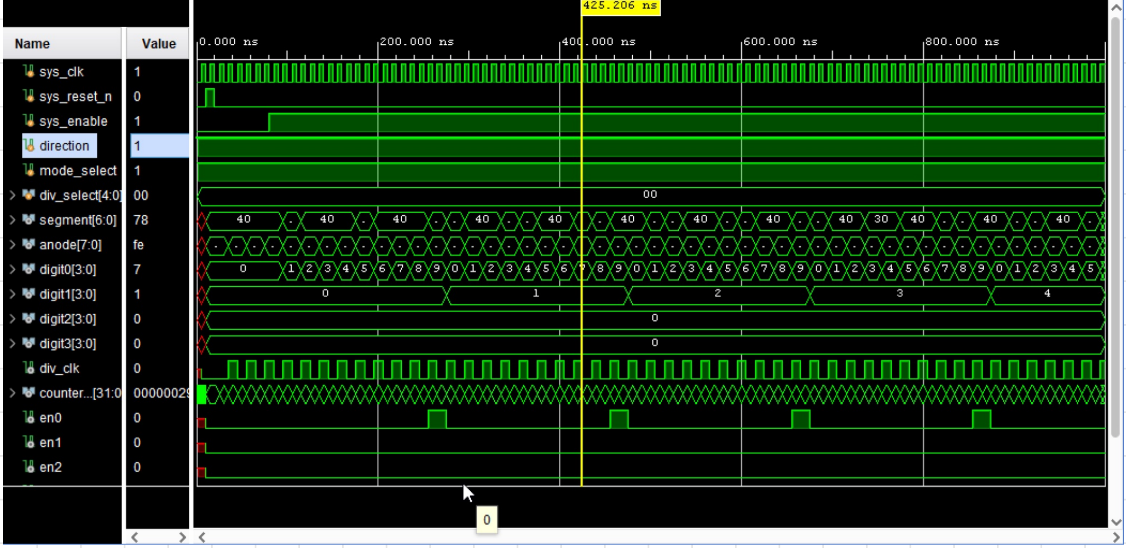
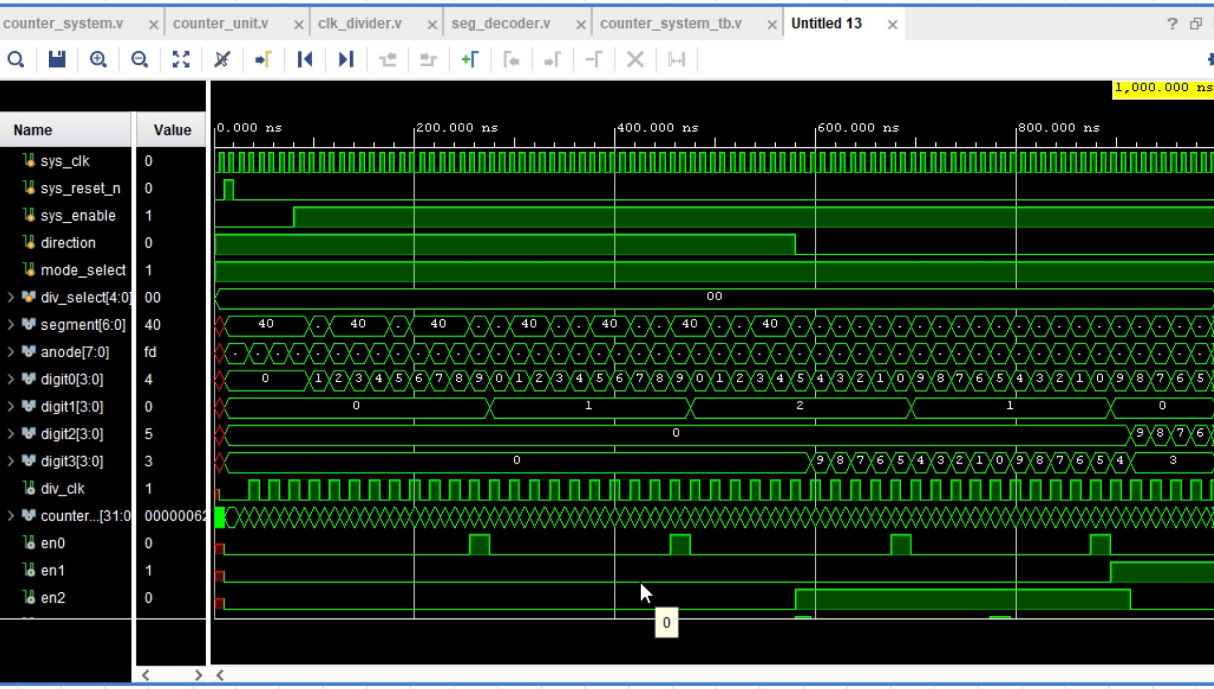
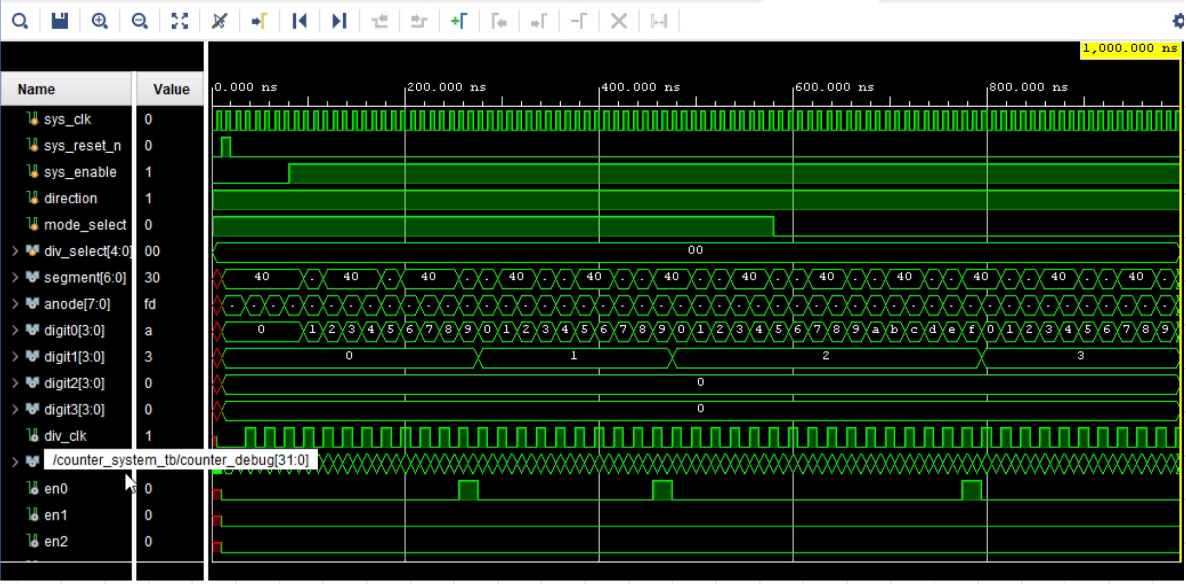
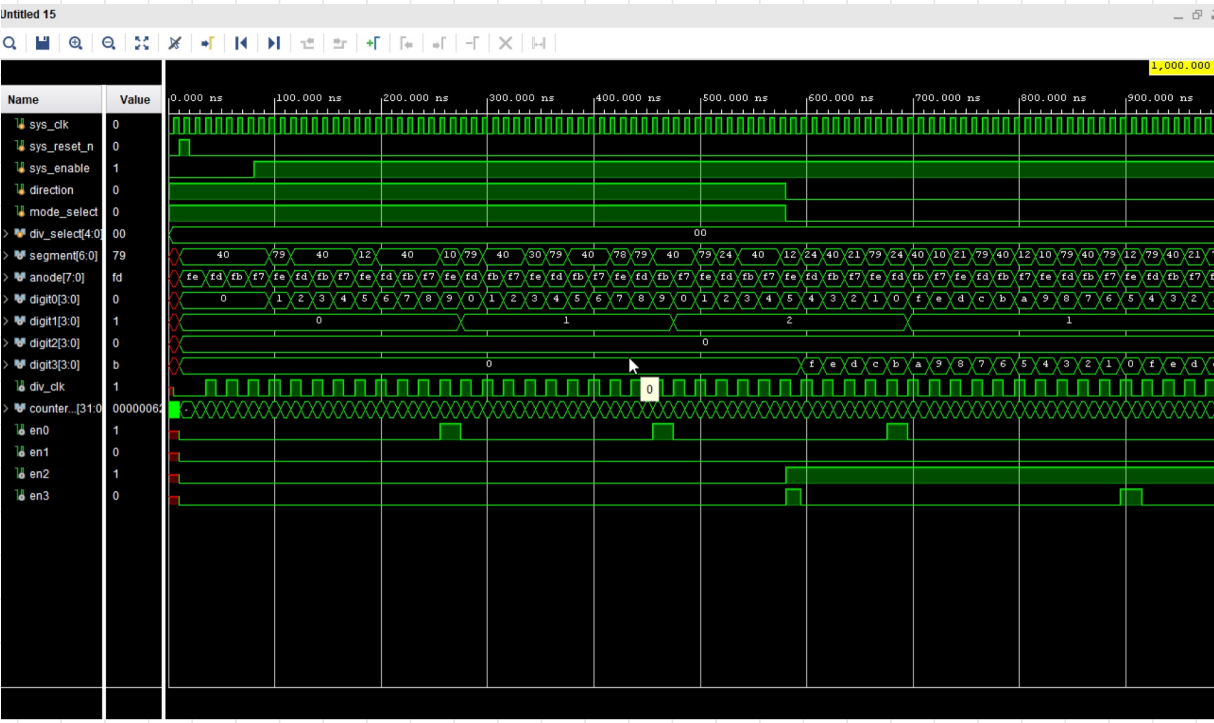

425.206 ns
Name
Value
sys_clk 1
sys_reset_n 0
sys_enable 1
direction 1
mode_select 1
div_select[4:0] 00
segment[6:0] 78
anode[7:0] fe
digit0[3:0] 7
digit1[3:0] 1
digit2[3:0] 0
digit3[3:0] 0
div_clk 0
counter...[31:0] 00000002
en0 0
en1 0
en2 0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns


counter_system.v
counter_unit.v
clk_divider.v
seg_decoder.v
counter_system_tb.v
Untitled 13
1,000.000 ns
Name
Value
sys_clk 0
sys_reset_n 0
sys_enable 1
direction 0
mode_select 1
div_select[4:0] 00
segment[6:0] 40
anode[7:0] fd
digit0[3:0] 4
digit1[3:0] 0
digit2[3:0] 5
digit3[3:0] 3
div_clk 1
counter...[31:0] 00000062
en0 0
en1 1
en2 0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns


1,000.000 ns
Name
Value
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
sys_clk 0
sys_reset_n 0
sys_enable 1
direction 1
mode_select 0
div_select[4:0] 00
segment[6:0] 30
anode[7:0] fd
digit0[3:0] a
digit1[3:0] 3
digit2[3:0] 0
digit3[3:0] 0
div_clk 1
/counter_system_tb/counter_debug[31:0]
en0 0
en1 0
en2 0


Untitled 15
1,000.000
Name
Value
0.000 ns
100.000 ns
200.000 ns
300.000 ns
400.000 ns
500.000 ns
600.000 ns
700.000 ns
800.000 ns
900.000 ns
sys_clk 0
sys_reset_n 0
sys_enable 1
direction 0
mode_select 0
div_select[4:0] 00
segment[6:0] 79
anode[7:0] fd
digit0[3:0] 0
digit1[3:0] 1
digit2[3:0] 0
digit3[3:0] b
div_clk 1
counter...[31:0] 00000062
en0 1
en1 0
en2 1
en3 0