Module mux 4x1
- Define
  - sel input
  - mux4x1_in input
  - mux4x1_out output

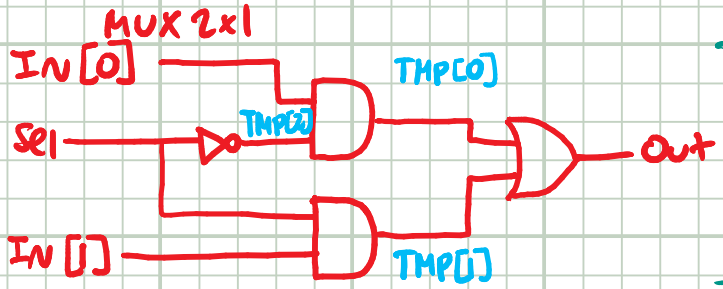
1:0
3:0

4Mux / 2 → level 1: 2(2Mux) / 2; level 2: 1(2Mux)
3 total 2Mux

4 Mux / n-1 mux

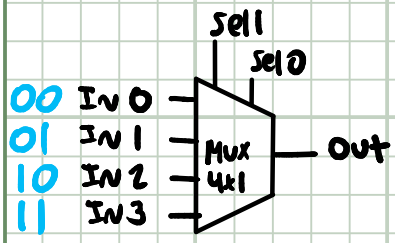
Module mux 2x1
- Define
  - sel input
  - mux2x1_in input
  - mux2x1_out output

1:0

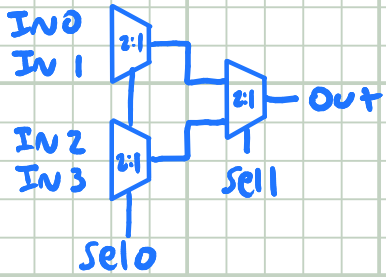



```
wire [2:0] TMP;

not (TMP[2], sel);
and (TMP[0], IN[0], TMP[2]);
and (TMP[1], IN[1], sel);
or (TMP[0], TMP[1];
```

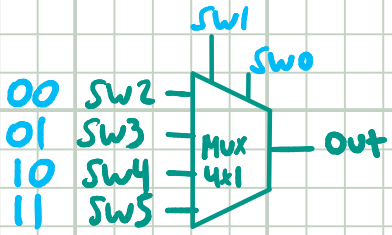


sel1	sel0	out
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3



S1	S0	A	B	C	D	out
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Ex: RED



S: 00 01
R: SW2 SW3
G: SW6 SW7
B: SW10 SW11

10 11
R: SW4 SW5
G: SW8 SW9
B: SW12 SW13