ECE 3300L

Lab 3

Instructor: Dr. Mohamed El-Hadedy

Group A

Sami Elias   012546378   samielias@cpp.edu
Joseph Popoviciu   014357772   jdpopoviciu@cpp.edu

Objective:

    The object of lab 3 is to create an up/down counter using Verilog that can count from 0 to

9. Since we need 4 bits to get to 9, we need to make sure it does not go over 9 because 4 bits can
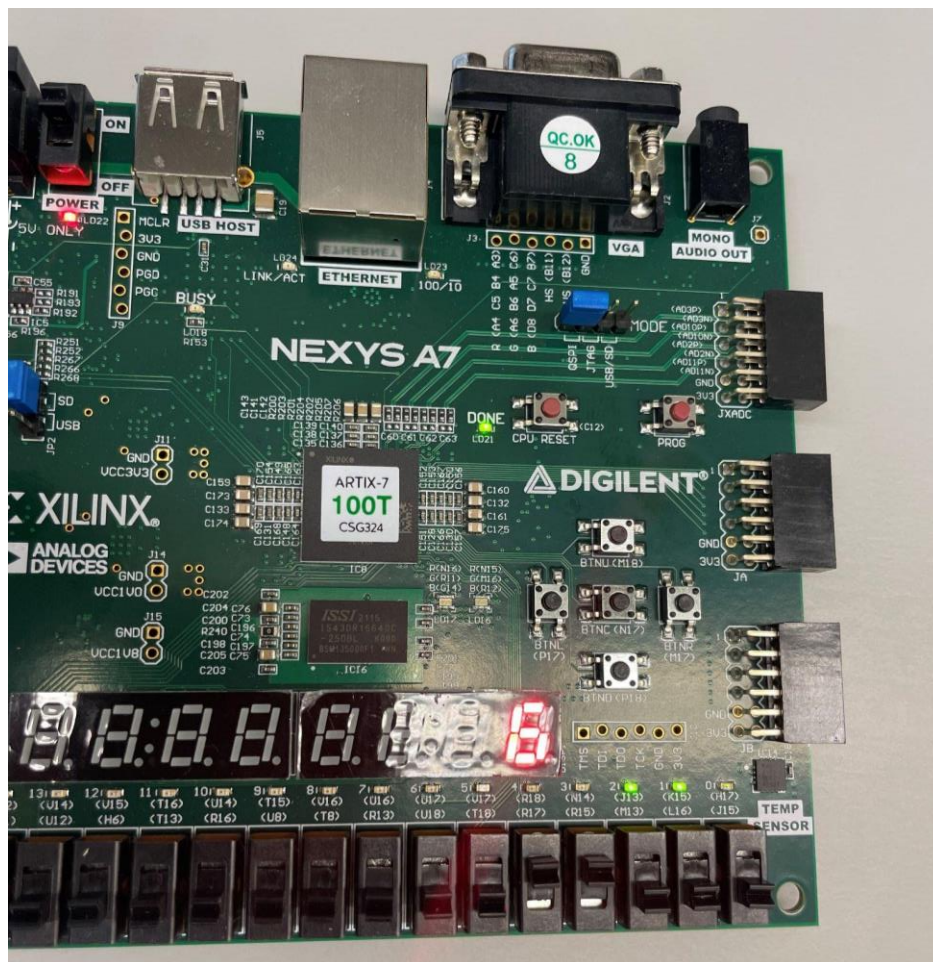
go up to F or 15.

Results:

Image 1

    The 5 switches on the right control the frequency of the clock using a 5 bit select

multiplexer.

The switches go from most significant to least significant, so the switches shown in image 1 show that the two most significant switches have been turned on causing the counter to slow down.
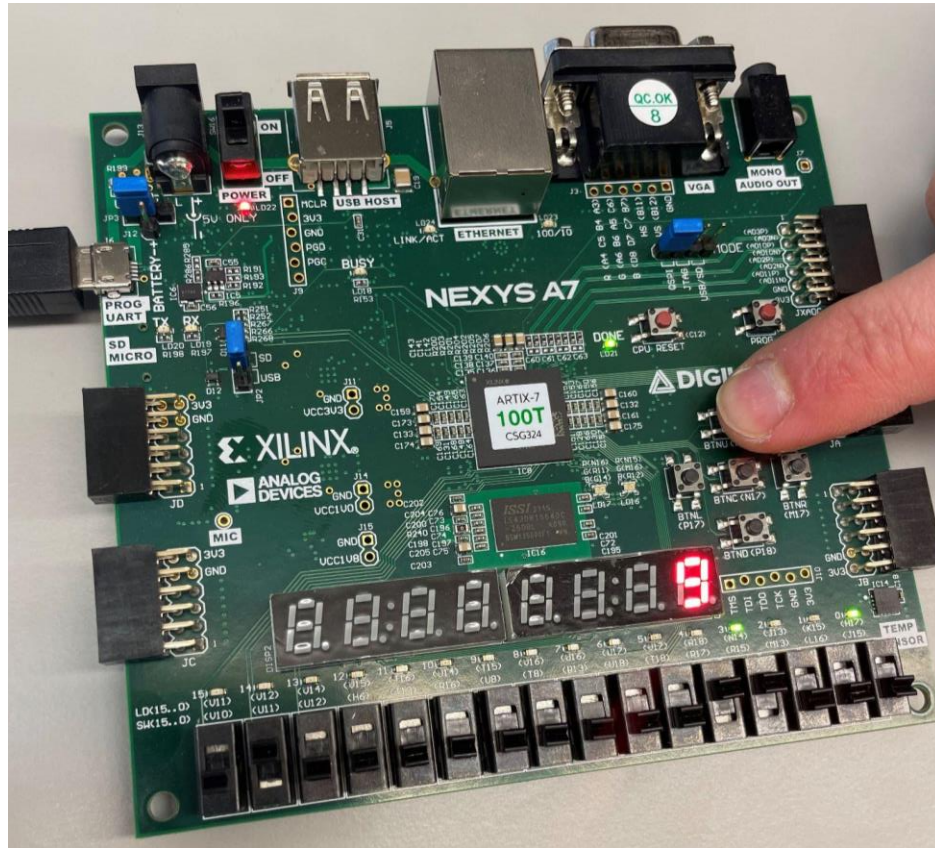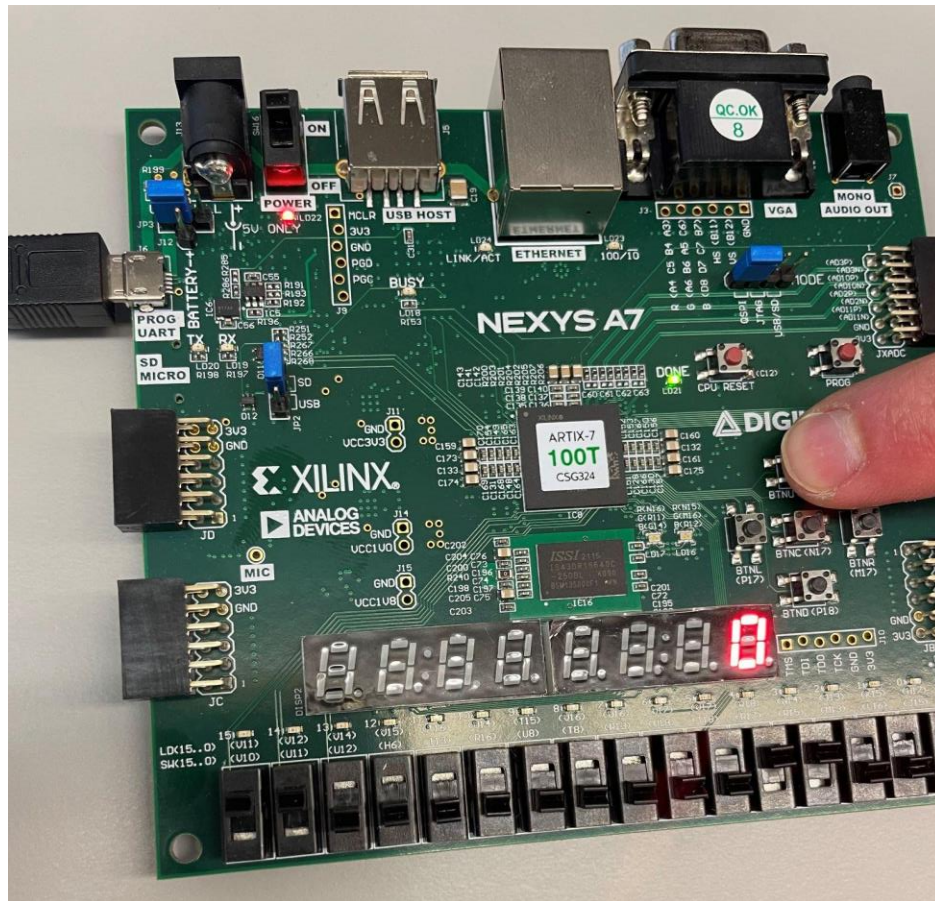

Image 2

Image 3

The switch all the way to the left is the up down counter. The switch to the right of that is the enable switch. If the up down counter switch is on, it will count down, if it is off, it will count up. The enable switch enables the counter to go. The reset button takes it to 0 if we are counting down and 9 if we are counting up. Image 2 shows that the reset button is being pressed and that it is going to count up. Image 3 shows the reset button being pressed, with the down counter enabled.

Conclusion:

We were able to create an up/down counter that can count up or down at different speeds. We used a clock divider to enable us to change the speed of the counting. We also have a reset button that sends the counter back to 0 or 9 depending on if it is going to count up or down. Lastly, we included an enable switch which turns the counter on and off.

Contributions:

Joseph Popoviciu:

I primarily worked on the code, programmed the FPGA board, and created the video demo. I also assisted with the lab report and powerpoint presentation.

Sami Elias:

I assisted with the code, wrote the main points of the report, and did the majority of the PowerPoint.