4300 Homework 1 - Isabel Warth

1.3 [2] <§1.3> Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor.
Looks like the source is first preprocessed to expand macros and directives, then a compiler converts it into assembly language specific to the processor. The assembler turns this into machine code, creates an object file, and then the linker combines object files and libraries to produce an executable, which the operating system loads into memory for the computer processor to run.

1.4 [2] <§1.4> Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.
a. What is the minimum size in bytes of the frame buffer to store a frame?
The total pixels: 1280 × 1024 = 1,310,720 pixels. Each pixel uses 3 bytes, with 1 byte for each color, so the total size is 1,310,720 × 3 = 3,932,160 bytes. The frame buffer will need 3,932,160 bytes.

b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?
Converting 3,932,160 bytes to bits = 31,457,280 bits. With a network speed of 100 Mbit/s, or 100,000,000 bits per second, the transmission time is 31,457,280 ÷ 100,000,000 = 0.3146 seconds, or about 315 milliseconds.

1.5 [4] <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
a. Which processor has the highest performance expressed in instructions per second?
Instructions per second is the clock rate divided by the CPI. For P1, 3 GHz clock rate divided by CPI of 1.5, is IPS = 2 billion. For P2, 2.5 GHz clock rate divided by CPI of 1.0, is IPS = 2.5 billion. For P3, 4 GHz clock rate divided by CPI of 2.2, is IPS = 1.82 billion. So, P2 has the highest performance.

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
Number of cycles is the clock rate multiplied by the execution time. For P1, 3 GHz, the cycles are 30 billion, CPI of 1.5, so the number of instructions is 20 billion. For P2, 2.5 GHz, the cycles are 25 billion, CPI of 1.0, so the instructions are also 25 billion. For P3, 4 GHz, the cycles are 40 billion, CPI of 2.2, so the instructions are around 18.18 billion.

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?
New execution time = 0.7*Old execution time
New CPI = 1.2*Old CPI

Execution time = Number of instructions*CPI/Clock rate

1.6 [5] Consider the table given next, which tracks several performance indicators for Intel desktop processors since 2010. The "Tech" column shows the minimum feature size of each processor's fabrication process. Assume that the die size has remained relatively constant and the number of transistors that comprise each processor scales at $(1/t)^2$, where t = the minimum feature size. For each performance indicator, calculate the average rate of improvement from 2010 to 2019, as well as the number of years required to double each at that corresponding rate.

Max. Clock Speed
Growth rate = (4.90/3.33)^(1/9) −1 = 0.0453 ≈ 4.53%
Doubling time = 704.53 = 15.45 years

Integer IPC/core
Growth rate = (8/4)^(1/9) −1 = 0.0798 ≈ 7.98%
Doubling time = 707.98 = 8.77 years

Cores
Growth rate = (8/2)^(1/9) −1 = 0.1487 ≈ 14.87%
Doubling time = 7014.87 = 4.71 years

Max. DRAM Bandwidth (GB/s):
Growth rate = (42.7/17.1)^(1/9) −1 = 0.1013 ≈ 10.13%
Doubling time = 7010.13 = 6.91 years

SP floating point (Gflop/s):
Growth rate = (627/107)^(1/9) −1 = 0.2126 ≈ 21.26%
Doubling time = 7021.26 = 3.29 years

L3 cache (MiB):
Growth rate = (12/4)^(1/9) −1 = 0.1372 ≈ 13.72%
Doubling time = 7013.72 = 5.1 years

1.7 **[20] <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2?**
Since P2 has fewer clock cycles, it will be faster than P1, even though its clock rate is higher. The main difference is the lower CPI for P2 across all the instruction classes.

a. What is the global CPI for each implementation?
CPIP1 = (0.1*1) + (0.2*2) + (0.5*3) + (0.2*3) = 0.1 + 0.4 + 1.5 + 0.6 = 2.6

b. Find the clock cycles required in both cases.
Clock cycles = CPI*Instruction count
Clock cyclesP1 = 2.6*1.0*106 = 2.6*106 cycles
Clock cyclesP2 = 2.0*1.0*106 = 2.0*106 cycles

1.12 The results of the SPEC CPU2006 bzip2 benchmark running on an AMD Barcelona has an instruction count of 2.389E12, an execution time of 750 s, and a reference time of 9650 s.
1.12.1 [5] <§§1.6, 1.9> Find the CPI if the clock cycle time is 0.333 ns.
CPI = CPU Time*Clock Rate/Instruction Count
Clock Rate = 1/Clock Cycle Time = 1/(3.33*10^−10) ≈ 3*10^9
CPI = (750 s*3*10^9Hz)/(2.389*10^12) ≈ 0.942

1.12.2 [5] <§1.9> Find the SPECratio.
SPECratio = Reference Time/Execution Time
SPECratio = 9650/750 ≈12.87

1.12.3 [5] <§§1.6, 1.9> Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% without affecting the CPI.
New CPU Time = 750*1.10 = 825

1.12.4 [5] <§§1.6, 1.9> Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% and the CPI is increased by 5%.
New CPU Time = 750*1.10*1.05 = 866.25s

1.12.5 [5] <§§1.6, 1.9> Find the change in the SPECratio for this change.
New SPECratio = Reference Time/New CPU Time = 9650/866.25 ≈ 11.14

1.12.6 [10] <§1.6> Suppose that we are developing a new version of the AMD Barcelona processor with a 4 GHz clock rate. We have added some additional instructions to the instruction set in such a way that the number of instructions has been reduced by 15%. The execution time is reduced to 700 s and the new SPECratio is 13.7. Find the new CPI.
CPI = (700*4*10^9)/(2.03065*10^12) ≈ 1.38

1.12.7 [10] <§1.6> This CPI value is larger than obtained in 1.11.1 as the clock rate was increased from 3 GHz to 4 GHz. Determine whether the increase in the CPI is similar to that of the clock rate. If they are dissimilar, why?
The CPI increased because the new version of the processor added instructions, increasing the complexity of the operations. Even though the clock rate increased, the change in instructions led to an ultimately higher CPI.

1.12.8 [5] <§1.6> By how much has the CPU time been reduced?
Time Reduction = 750−700 = 50s

1.12.9 [10] <§1.6> For a second benchmark, libquantum, assume an execution time of 960 ns, CPI of 1.61, and clock rate of 3 GHz. If the execution time is reduced by an additional 10% without affecting the CPI and with a clock rate of 4 GHz, determine the number of instructions.
Instructions = Execution Time*Clock Rate/CPI = (864*10^−9*4*10^9)/(1.61) ≈ 2.146*10^9

1.12.10 [10] <§1.6> Determine the clock rate required to give a further 10% reduction in CPU time while maintaining the number of instructions and with the CPI unchanged.
Clock Rate = CPI*Instructions/Execution Time = (1.61*2.146*10^9)/(777.6*10^−9) ≈ 4.43GHz

1.12.11 [10] <§1.6> Determine the clock rate if the CPI is reduced by 15% and the CPU time by 20% while the number of instructions is unchanged.
Clock Rate = (1.3685*2.146*10^9)/(768*10^−9) ≈ 3.82GHz