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Homework #1

1.3 [2] Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor

Compiled into assembly language program which then is built into machine language program.

1.4 [2] Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.

a. What is the minimum size in bytes of the frame buff er to store a frame?

1024 * 1280 = 1,310,720 * 3 = 3,932,160 bytes/frame

b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

3,932,160 * 8 * 1/100e^5 = 0.31 sec

1.5 [4] Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

3 * 10^9/1.5 = 2 *10^9

2.5 * 10^9 = 2.5 * 10^9

4 * 10^9/2.2 = 1.8 * 10^9

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

10*3*10^9 = 30 * 10^9 sec

10 * 2.5 * 10^9 = 25* 10^9 sec

10 * 4 * 10^9 = 40 * 10^9 sec

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

30 * 10^9/1.5 = 20 * 10^9

25 * 10^9 = 25*10^9

40 * 10^9/2.2 = 18.18*10^9

Clk rate

20*10^9*1.8/7 = 5.14 GHz

25*10^9*1.2/7= 4.28 GHz

18.18*10^9*2.6/7 = 6.75 GHz

1.6 [20] Consider two different implementations of the same instruction set architecture. Th e instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?

Time = (10^5 + 2 * 10^5 * 2 + 5 * 10^5 * 3 + 2 * 10^5 * 3) / (2.5 *10^9) = 10.4 * 10^-4 sec

Time = (10^5 * 2 + 2 * 10^5 * 2 + 5 *10^5 * 2 +2 * 10^5 * 2) / (3 * 10^9) = 10.4 * 10^-4 sec

CPI = 10.4 * 10^ 4 * 2.5 * 10^9 / 10^6 = 2.6

CPI = 6.66 * 10^-4 * 3 * 10^9 / 10^6 = 2

b. Find the clock cycles required in both cases.

Clk cycles = 10^5 + 2 * 10^5 * 2 + 5 *10^5 * 3 +2 *10^5 * 3 = 26 * 10^5

Clk cycles = 10^5 * 2 + 2 * 10^5 *2 + 5 * 10^5 * 2 +2 * 10^5 * 2 = 20 * 10^5

1.7 [15] Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

A Cpi = 1.1

B Cpi = 1.25

b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

1.37

c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

Ta / Tnew = 1.67

Tb /Tnew = 2.27

1.11 The results of the SPEC CPU2006 bzip2 benchmark running on an AMD Barcelona has an instruction count of 2.389E12, an execution time of 750 s, and a reference time of 9650 s.

1.11.1 clk rate = 1 / cycle time = 3 GHz, CPI = 3 * 10^9 * 750 / (2389 * 10^9) = 12.86

1.11.2 spec ratio = 9650 / 750 = 12.86

1.11.4 CPU = 1.1 * 1.05 = 1.155 increased by 15.5%

1.11.5 SPECCratio(after)/Before = 1 / 1.1555 = 0.86 decreased by 14%

1.11.6 CPI = 700 * 4 * 10^9 / (0.85 * 2389 * 10^9) = 1.37

1.11.7 clk rate ratio = 4 / 3 = 1.33, CPI @ 4GHz = 1.37, CPI @ 3 GHz = 0.94, ratio = 1.45

1.11.8 700 / 750 = 0.933 cpu reduced by 6.7%

1.11.9 No instr = 960 * 0.9 * 4 * 10^9 / 1.61 = 2146 * 10^9

1.11.10 clk rate = 1/ 0.9 = 3.33 GHz

1.11.11 clk rate = 0.85 / 0.80 = 3.18 GHz

1.12 Section 1.10 cites as a pitfall the utilization of a subset of the performance equation as a performance metric. To illustrate this, consider the following two processors. P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions.

1.12.1 P1 = 5 * 10^9 * 0.9 / 4* 10 ^9 = 1.125 sec, P2 = 10^9 * 0.75 / (3 * 10^9) = 0.25 sec

1.12.2 p1 = 2.25 * 3 = 1021 sec. P2 = 5 * 0.75 / 3 * 10^9 = 9 * 10^8

1.12.3 MIPS = 4 * 10^9 * 10^-6 / 0.9 = 4.44 * 10^3

MIPS2 = 3 * 10^9 * 10^-6 / 0.75 = 4.0 * 10^3

1.12.4 p1 = 0.4 * 5 * 10^9 * 10^-6 / 1.125 = 175 * 10 ^3

P2 = 0.4 * 10^9 * 10^-6 / 0.25 = 1.60 * 10 ^3