Lab 8 - Colored VGA with UART

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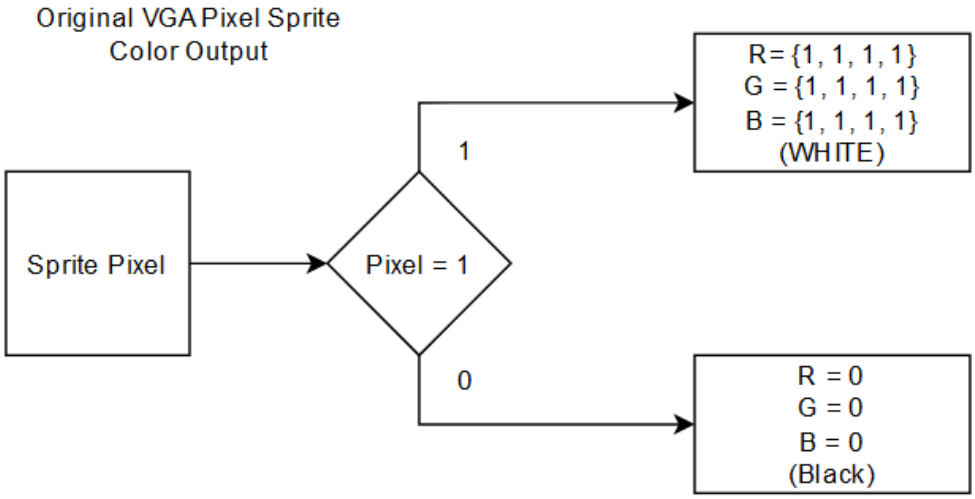
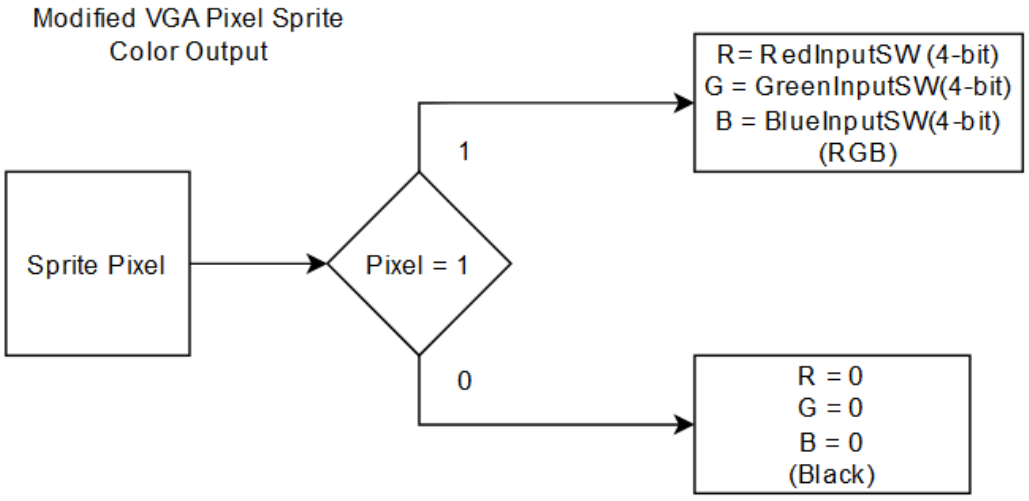
Architecture:

The original code is modified to accommodate for color using switches and pixel position control via UART.

VGA Color Control

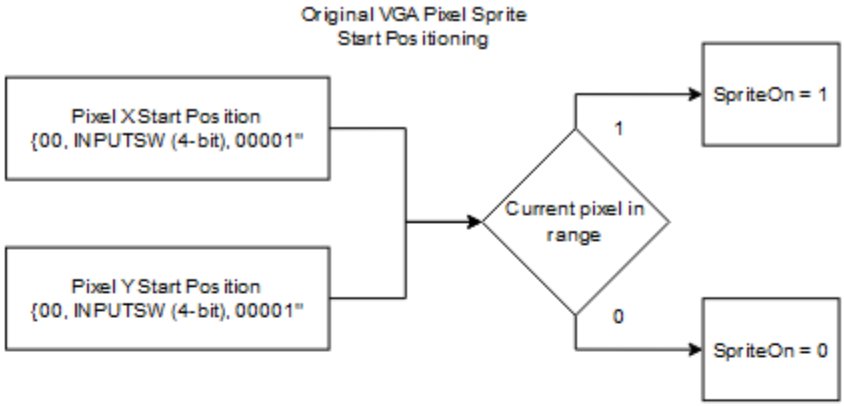
The original VGA outputted a color of white if a sprite pixel is to be enabled. This was done by setting the RGB to a fixed value of 0xF for each color. To add color, it was modified to take in a set of 4 input switches for each color instead.

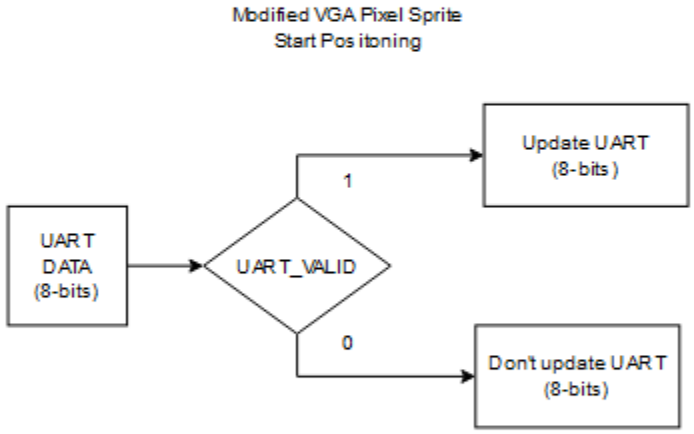


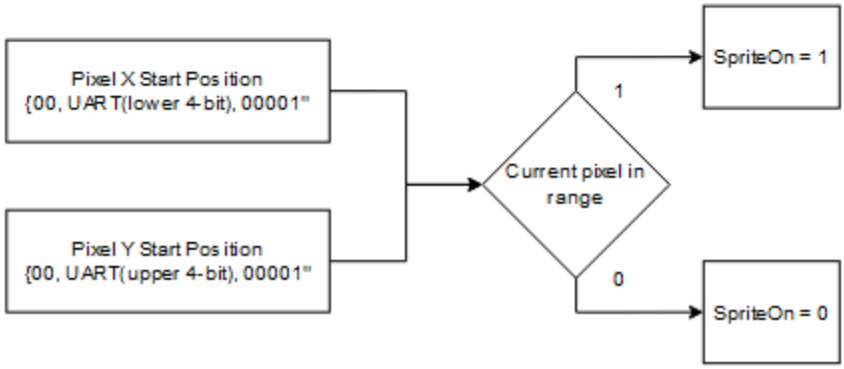


VGA Position Control

The original VGA position is controlled via 8 input switches. To incorporate UART, a variable is updated with the UART data input whenever the value is valid. This value is used instead of the input switches to control the VGA position. The lower 4 bits of the UART input will be used for the starting position on the x-axis while the upper 4 bits will be used for the starting position on the y-axis.







Code Detail:

VGA Color Control

The original code is changed from outputting a fixed value of 0xF if the pixel is supposed to be turned on and 0x0 if the pixel is supposed to be turned off. Instead, the code checks if the pixel is supposed to be turned on, then uses the values from the input switches as the color to be displayed.

VGA Position Control

The UART code is implemented from lab 7. The UART module takes in an 8-bit value and outputs a DATA_VALID flag once finished. The code updates a variable with the current value of the UART data when the DATA_VALID flag is asserted. This value is then used in place of the input switches of the original design for the starting x/y position of the sprite.

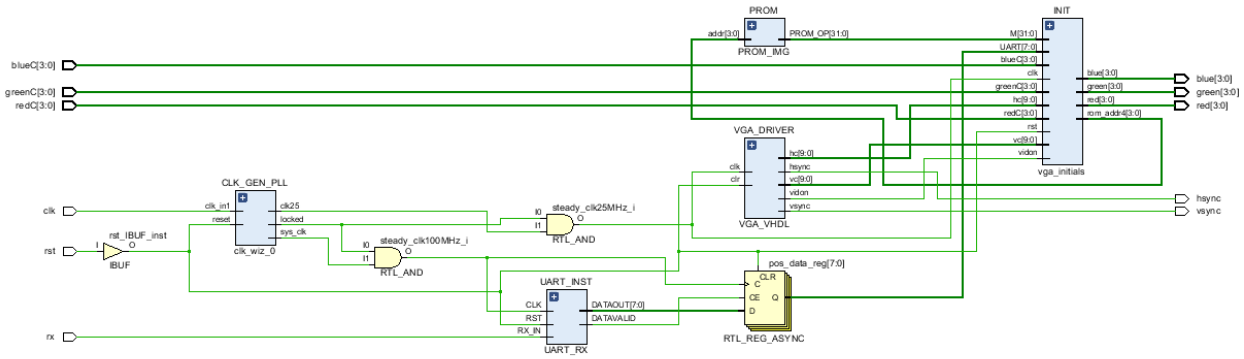
Corner Cases:

VGA Position Control

The UART has data input size set to 8 bits on Realterm, so any invalid number will not be sent to the board (0-FF).

Area/Resource Information:

Elaborated Design of Entire System



Resource Usage of Entire System

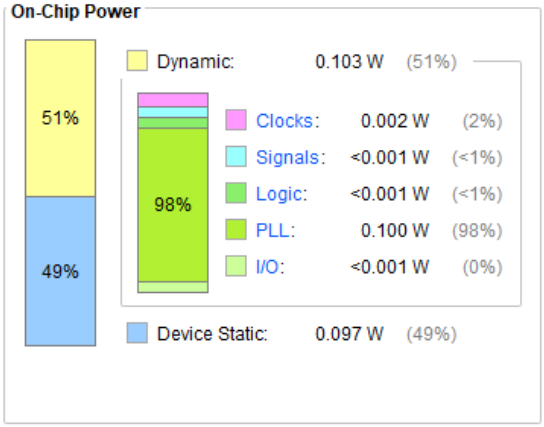
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
✓ synth_1	constrs_1	synth_design Complete!								99	87	0.0	0	0
✓ impl_1	constrs_1	write_bitstream Complete!	4.384	0.000	0.102	0.000	0.000	0.200	0	99	89	0.0	0	0

Power Usage Details

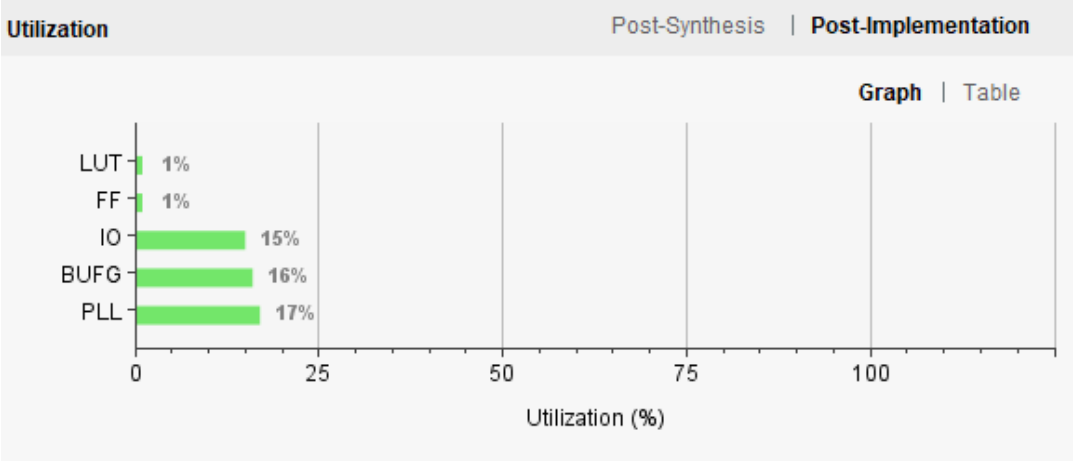
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.2 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.9°C**
Thermal Margin:	59.1°C (12.8 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Utilization



Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	99	63400	0.16
FF	89	126800	0.07
IO	32	210	15.24
BUFG	5	32	15.63
PLL	1	6	16.67