Lab 7 - ALU with FIFO Buffer and UART Inputs

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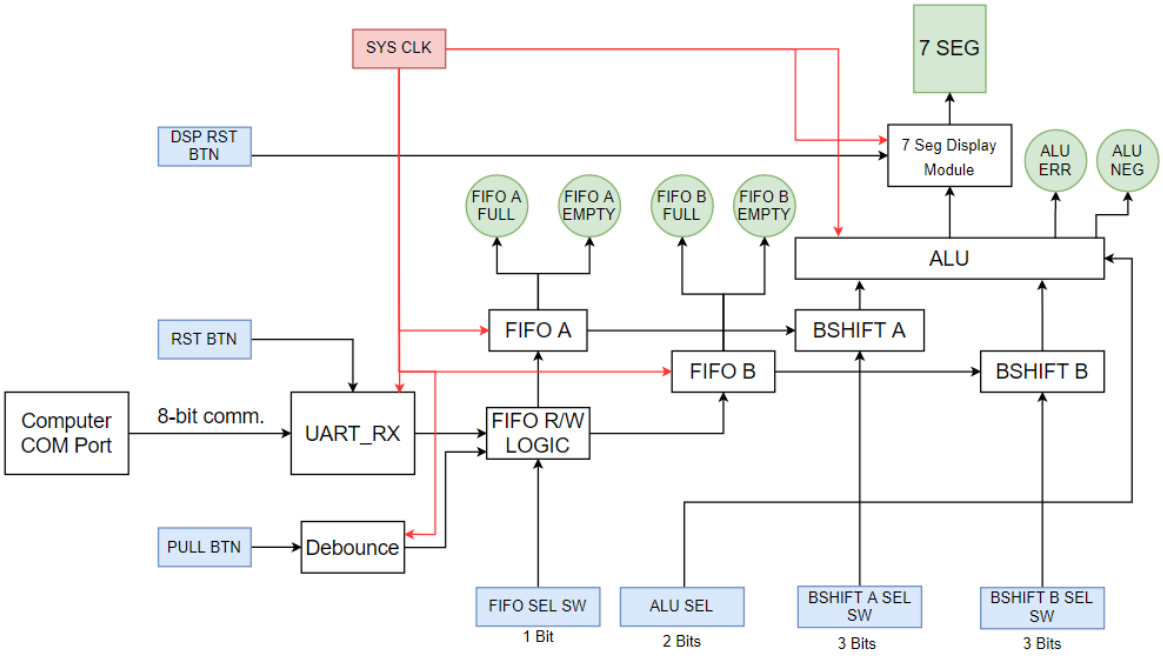
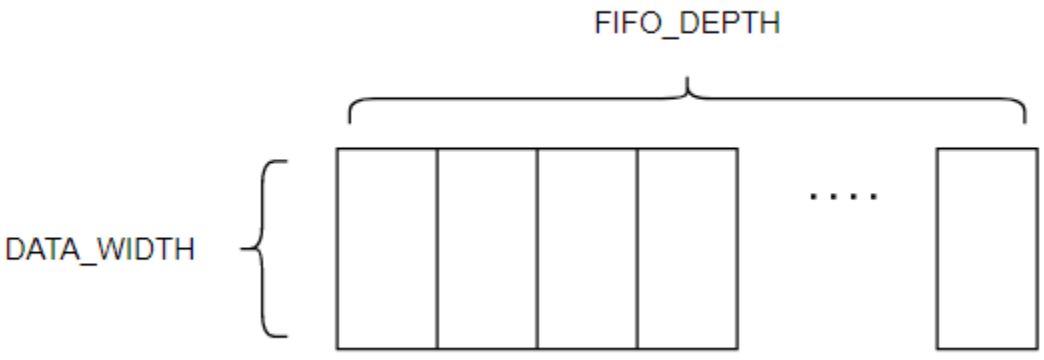
ECE 4304

Architecture:

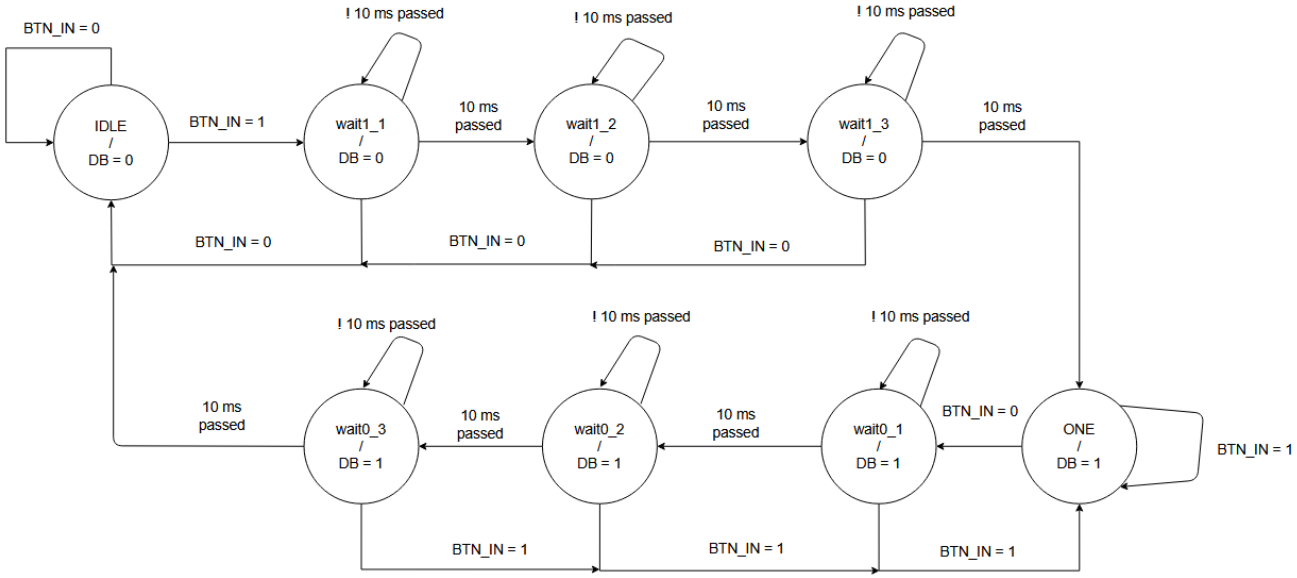
Top Architecture:
The architecture of this lab mainly consists of components from previous labs including the ALU, Barrel Shifter, and 7 segment BCD displayer.



FIFO Architecture:
FIFO's have generic data and depth sizes where data size represents how many bits each entry is and depth represents how many data entries it can store before becoming full. The program uses two pointers, head and tail, and a boolean variable, looped, to determine the empty/full state of the FIFO.



Debounce Architecture:
Debounce FSM:



Code Detail:

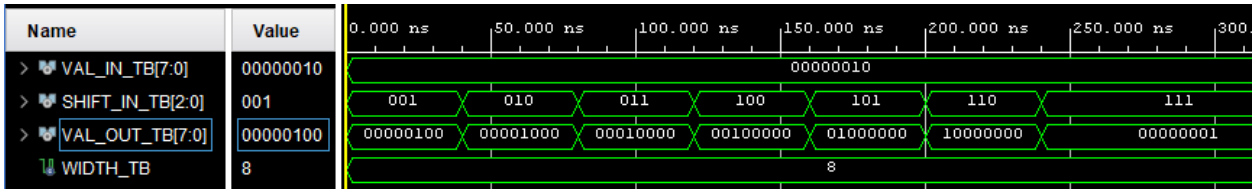
Button Debounce:
When the pull button is pressed once on the FPGA board, the “pull” happens way more than once because the button is pressed down for multiple clock cycles. This is a problem because the entire FIFO could be emptied in one quick press. To prevent this from happening, a debouncer module was created using an FSM as shown in the architecture section.

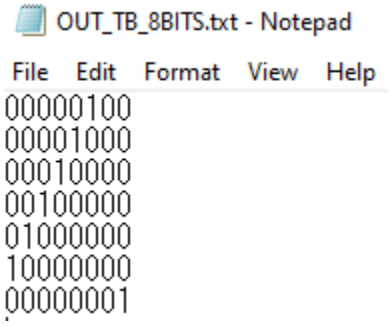
UART:
The UART RX Module which reads in inputs from the computer features a moore-style FSM. Data from the computer is read bit by bit in N states where N is the number of bits the UART communication is. The total number of states is N+3 including the idle, start, and demistart states. D-Flip Flops and a counting process is used to sync the reading to the FPGA clock speed. The module outputs the 8-bit data and a 1 bit validation bit.

Corner Cases:

Barrel Shifter:
When the last bit rotates back to the first bit, as in the most significant bit is roasted to the least significant bit, shown below. If the barrel shifter simply just shifted left, the least significant bit

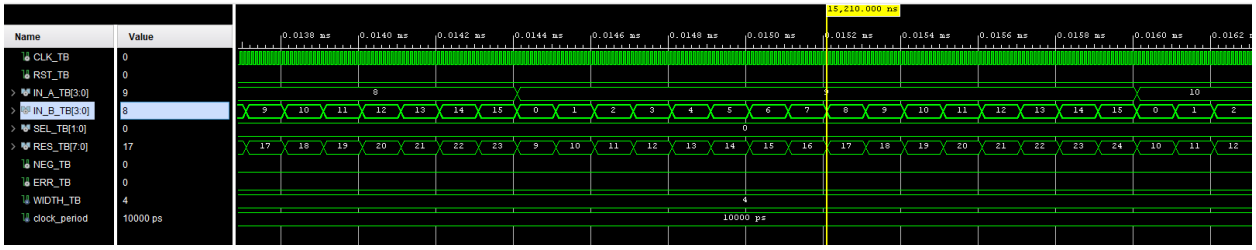
would not become the most significant bit; However, the corner case is verified, proving that the bits are rotated.





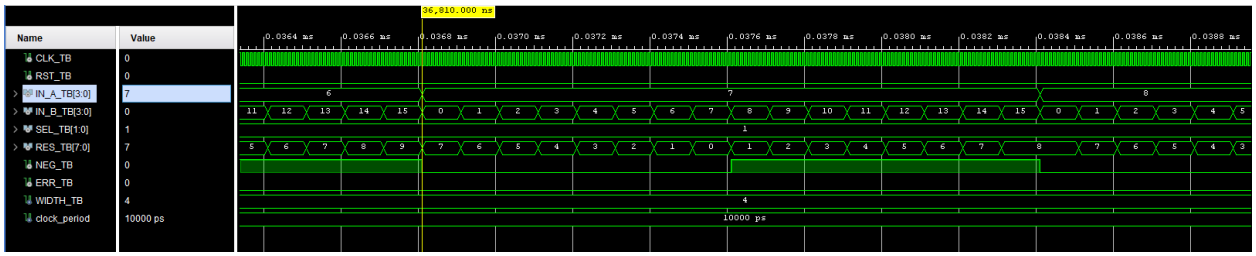
ALU:

Addition Testbench



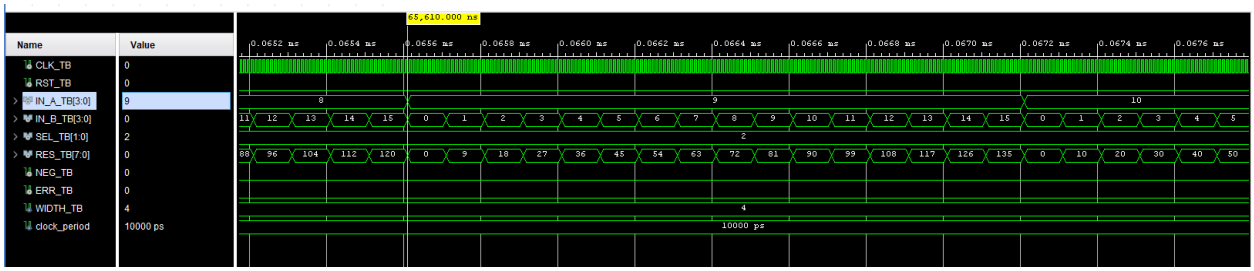
Addition is valid for all values (0-15) + (0-15), covering all possible cases for 4-bit addition.

Subtraction Testbench



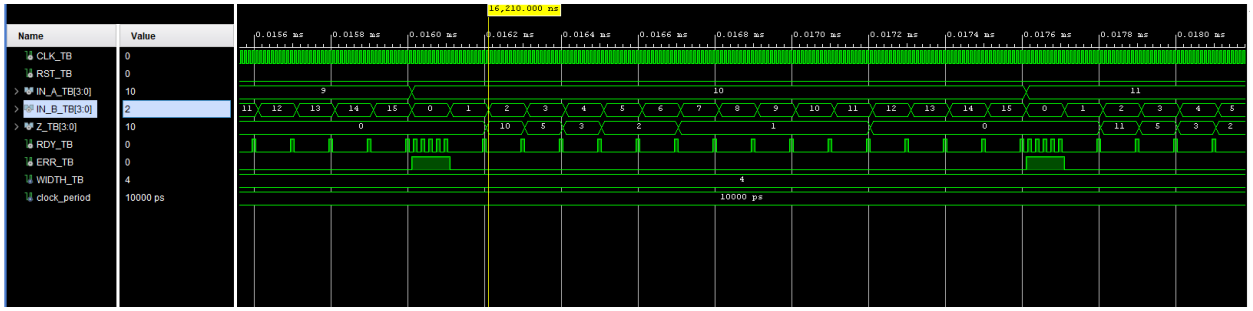
For subtraction, an edge case occurs when the result is a negative number. The testbench shows that the design deals with it promptly, returning the absolute value with a negative flag.

Multiplication Testbench



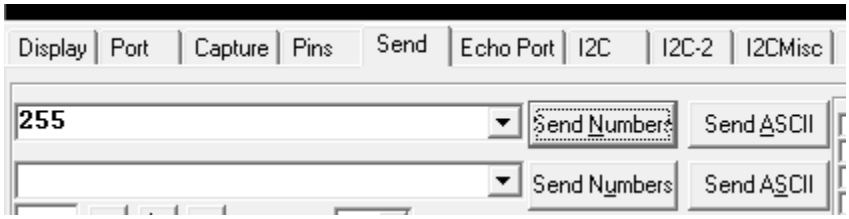
For multiplication, an edge case occurs when the result is larger than 4-bits. The design needs to ensure that the output will fit into 8-bits. The testbench shows that values are valid from 9 * (0-15), which produces results greater than 4-bits.

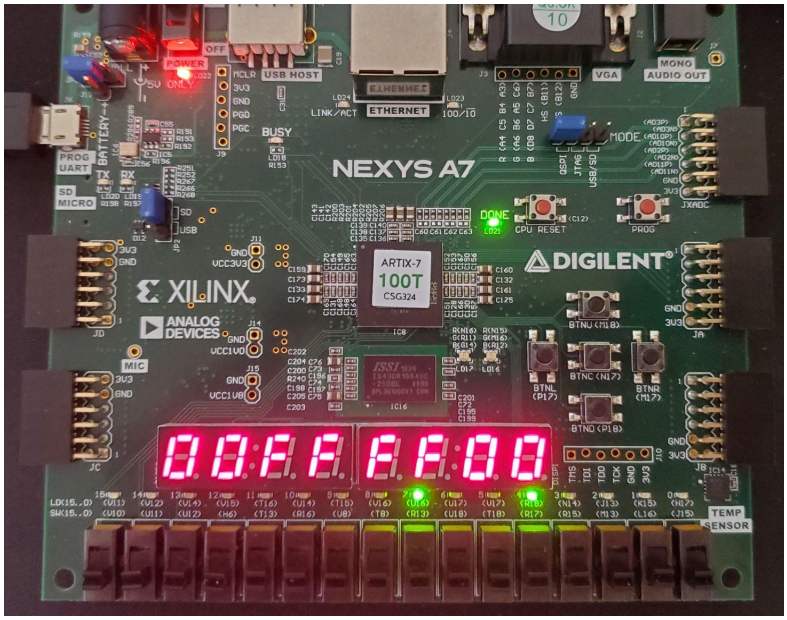
Division Testbench



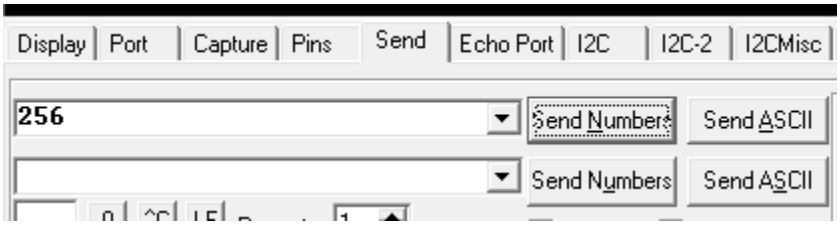
UART Module:

Sending max 8 bit unsigned decimal value: 255 (FF)

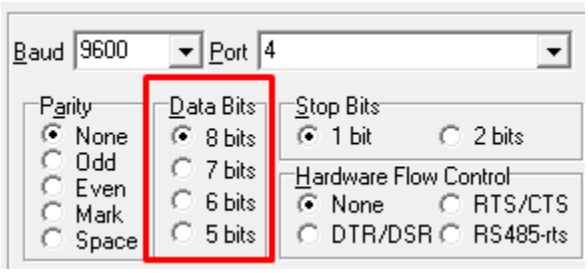




Sending value above max value:



Since the data input size is set to 8 bits on Realterm, any invalid number (over 255 or under 0) will not be sent to the board.



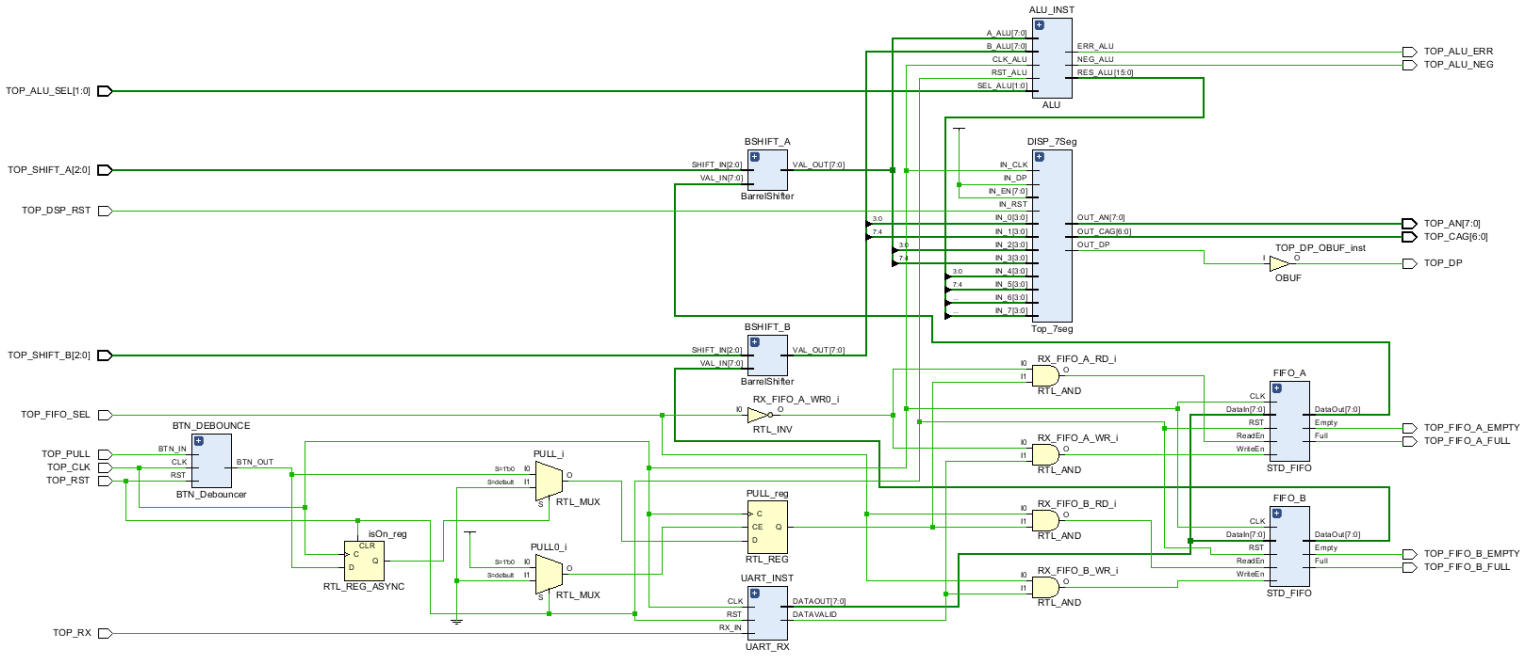
FIFO:

Two corner cases for the FIFO component is when the read is enabled but the FIFO is full and when the write is enabled but the FIFO is empty.

When the FIFO is full and data is being inputted, it will ignore those inputs because there is no more room for them.

When the FIFO is empty and data needs to be written, it will ignore the write request because there is nothing to write from the FIFO.

Area/Resource Information:



Elaborated Design of Entire System

Resource Usage of Entire System

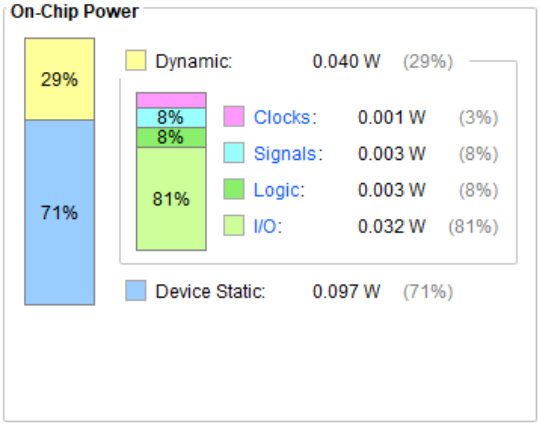
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								314	160	0.0	0	0
impl_1	constrs_1	write_bitstream Complete!	3.426	0.000	0.048	0.000	0.000	0.137	0	312	160	0.0	0	0

Power Usage Details

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.137 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (12.9 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Utilization

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	312	63400	0.49
LUTRAM	16	19000	0.08
FF	160	126800	0.13
IO	36	210	17.14
BUFG	1	32	3.13

Graph | Table