Proiect CID

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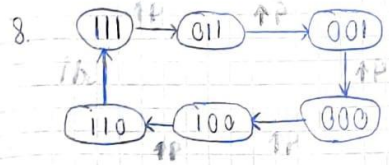
Rezolvare pe hartie:

Să se proiecteze automatul de transmitere a folosind un numărator pe 4 biți, descris de tabelul de adevăr D și un multiplexor IV.

8.

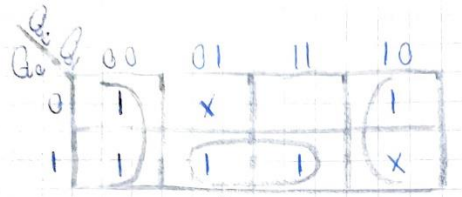


D.

R	clk	ld	en	Action
0	x	x	x	Reset
1	↓	1	x	Load
1	↓	0	0	Count
otherwise				Wait

IV. MUX 4:1 și MUX 2:1

Q_2	Q_1	Q_0	Ld	En	C D_2	B D_1	A D_0
0	0	0	1	x	1	0	0
0	0	1	1	x	0	0	0
0	1	0	x	x	x	x	x
0	1	1	1	x	0	0	1
1	0	0	1	x	1	1	0
1	0	1	x	x	x	x	x
1	1	0	0	0	x	x	x
1	1	1	1	x	0	1	1



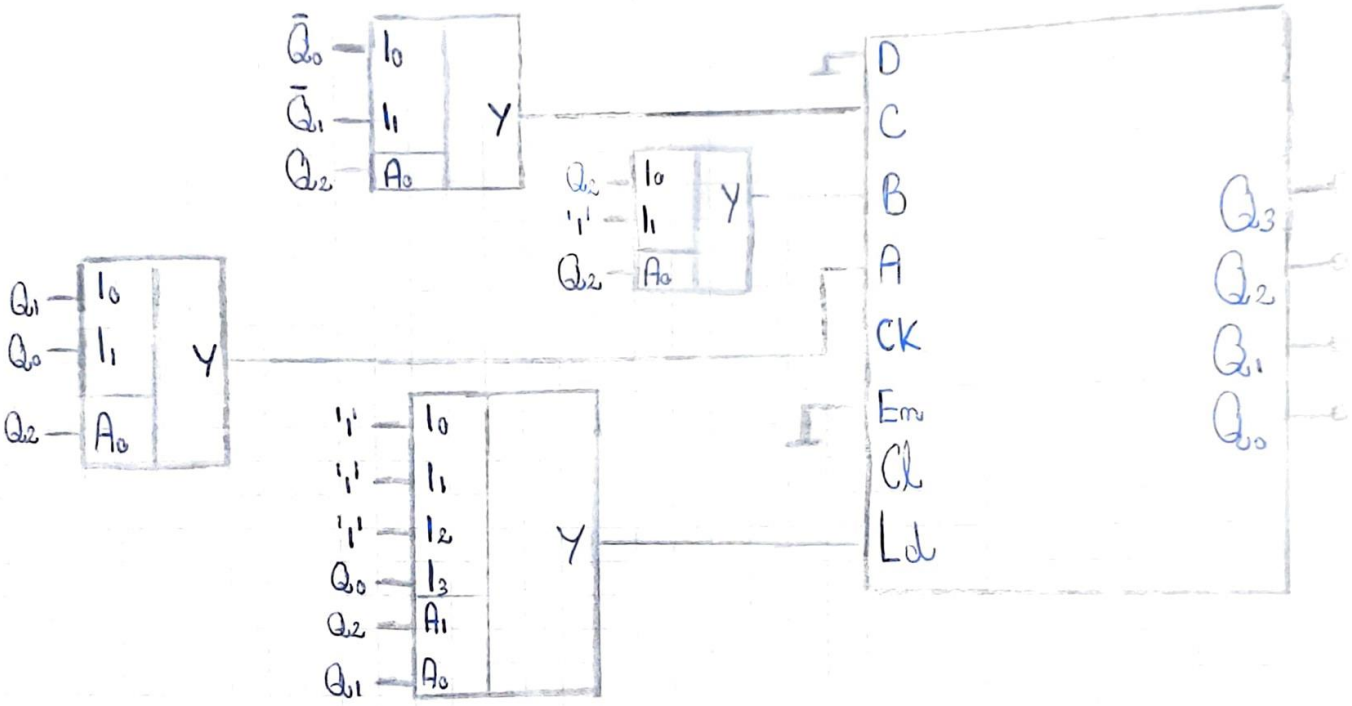
$Ld = \bar{Q}_1 + Q_0 Q_1$

$Em = '0'$

$D_2 = \bar{Q}_0$

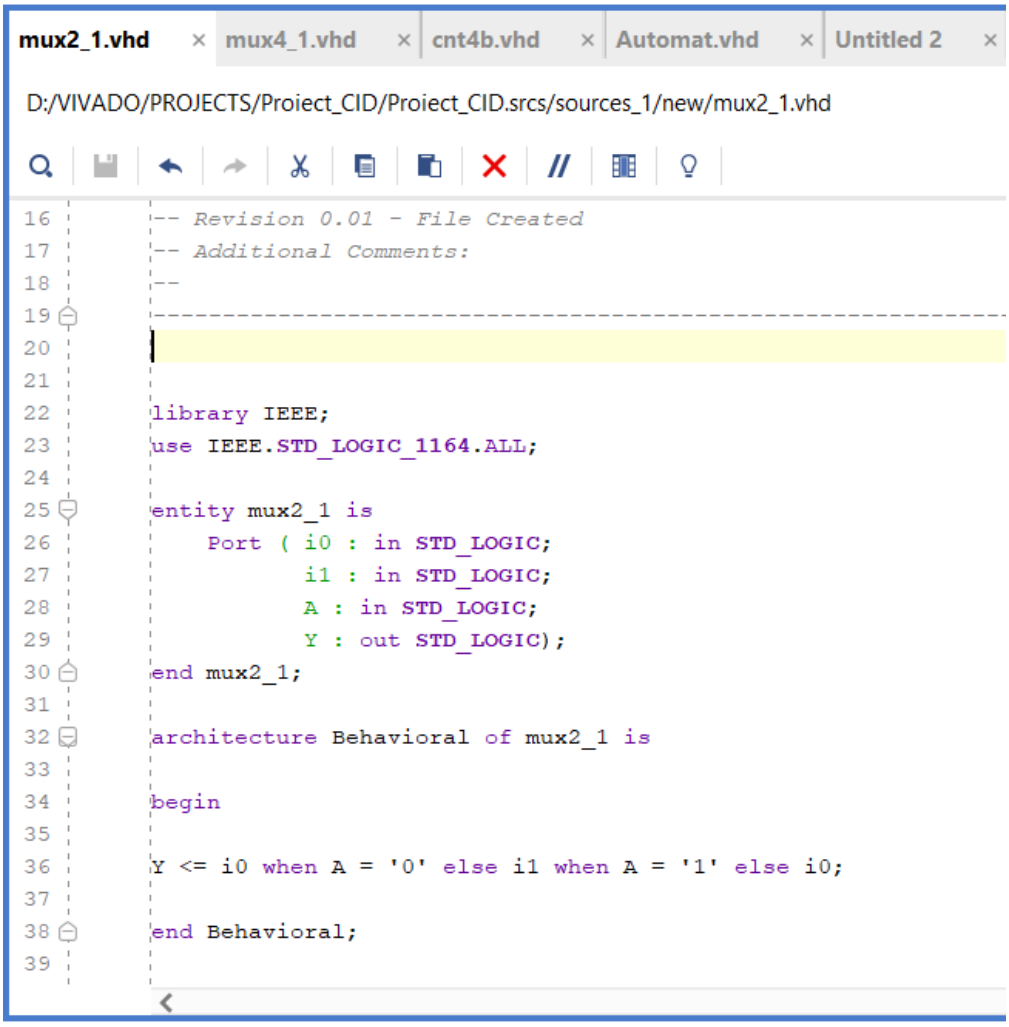
$D_1 = Q_2$

$D_0 = Q_1$



Sursele de proiectare:

Mux2:1:



Mux4:1:

mux2_1.vhd | mux4_1.vhd | cnt4b.vhd | Automat.vhd | Untitled 2

D:/VIVADO/PROJECTS/Proiect_CID/Proiect_CID.srcs/sources_1/new/mux4_1.vhd

```
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  entity mux4_1 is
26      Port ( i0 : in STD_LOGIC;
27             i1 : in STD_LOGIC;
28             i2 : in STD_LOGIC;
29             i3 : in STD_LOGIC;
30             a1 : in STD_LOGIC;
31             a0 : in STD_LOGIC;
32             y : out STD_LOGIC);
33  end mux4_1;
34
35  architecture Behavioral of mux4_1 is
36
37  signal a : std_logic_vector ( 1 downto 0);
38
39  begin
40
41  a <= a1 & a0;
42
43  with a select
44  y <= i0 when "00",
45       i1 when "01",
46       i2 when "10",
47       i3 when "11",
48       i0 when others;
49
50  end Behavioral;
51
```

Numarator 4biti:

mux2_1.vhd | mux4_1.vhd | **cnt4b.vhd *** | Automat.vhd | Untitled 2

D:/VIVADO/PROJECTS/Proiect_CID/Proiect_CID.srcs/sources_1/new/cnt4b.vhd

```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24  use ieee.std_logic_unsigned.all;
25  use ieee.std_logic_arith.all;
26
27  entity cnt4b is
28      Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
29             clk : in STD_LOGIC;
30             r : in STD_LOGIC;
31             en : in STD_LOGIC;
32             ld : in STD_LOGIC;
33             q : out STD_LOGIC_VECTOR (3 downto 0);
34             cy : out STD_LOGIC);
35  end cnt4b;
36
37  architecture Behavioral of cnt4b is
38
39  signal qint : std_logic_vector (3 downto 0):= "0000";
40
41  begin
42
43  q <= qint;
44  cy <= '1' when (qint= "1111" and en = '1') else '0';
45
46  count4b: process(r, clk)
47  begin
48  if r = '0' then
49     qint <= "0000";
50  elsif (falling_edge(clk) and ld = '1') then
51     qint <= d;
52  elsif(falling_edge(clk) and ld = '0' and en = '0') then
53     qint <= qint + 1;
54  else
55     qint <= qint;
56  end if;
57  end process;
58
59  end Behavioral;
60
```

Automat:

Project Summary | Automat.vhd

D:/VIVADO/PROJECTS/Proiect_CID/Proiect_CID.srcs/sources_1/new/Automat.vhd

```
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  entity Automat is
26      Port ( r : in STD_LOGIC;
27             clk : in STD_LOGIC;
28             q : out STD_LOGIC_VECTOR (3 downto 0));
29  end Automat;
30
31  architecture Behavioral of Automat is
32
33  component cnt4b is
34      Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
35             clk : in STD_LOGIC;
36             r : in STD_LOGIC;
37             en : in STD_LOGIC;
38             ld : in STD_LOGIC;
39             q : out STD_LOGIC_VECTOR (3 downto 0);
40             cy : out STD_LOGIC);
41  end component cnt4b;
42
43  component mux2_1 is
44      Port ( i0 : in STD_LOGIC;
```

Project Summary × **Automat.vhd** ×

D:/VIVADO/PROJECTS/Proiect_CID/Proiect_CID.srcs/sources_1/new/Automat.vhd

```
45              i1 : in STD_LOGIC;
46              A : in STD_LOGIC;
47              Y : out STD_LOGIC);
48  end component mux2_1;
49
50  component mux4_1 is
51      Port ( i0 : in STD_LOGIC;
52             i1 : in STD_LOGIC;
53             i2 : in STD_LOGIC;
54             i3 : in STD_LOGIC;
55             a1 : in STD_LOGIC;
56             a0 : in STD_LOGIC;
57             y : out STD_LOGIC);
58  end component mux4_1;
59
60  signal qint: std_logic_vector(3 downto 0);
61  signal en , ld : std_logic;
62  signal d: std_logic_vector (3 downto 0);
63  signal net1, q0_neg, q1_neg :std_logic;
64
65  begin
66
67  U: cnt4b port map ( d => d,
68                      clk => clk,
```

Project Summary | Automat.vhd

D:/VIVADO/PROJECTS/Proiect_CID/Proiect_CID.srcs/sources_1/new/Automat.vhd

```
69                      en => en,
70                      r => r,
71                      ld => ld,
72                      q => qint);
73
74  q0_neg <= not qint(0);
75  q1_neg <= not qint(1);
76
77  U1: mux2_1 port map ( i0 => q0_neg,
78                        i1 => q1_neg,
79                        A => qint(2),
80                        Y => d(2));
81
82  U2:  mux2_1 port map ( i0 => qint(2),
83                         i1 => '1',
84                         A => qint(2),
85                         Y => d(1));
86
87  U3:  mux2_1 port map ( i0 => qint(1),
88                         i1 => qint(0),
89                         A => qint(2),
90                         Y => d(0));
91
92  U4:  mux4_1 port map ( i0 => '1',
93                         i1 =>'1',
94                         i2 => '1',
95                         i3 => qint(0),
96                         a1 => qint(2),
97                         a0 => qint(1),
98                         y => ld);
99
100 en <= '0';
101 q <= qint;
102 d(3) <= '0';
103 end Behavioral;
104
```

Sursa de simulare:

Automat.vhd | testbench.vhd | Untitled 2

D:/VIVADO/PROJECTS/Proiect_CID/Proiect_CID.srcs/sim_1/new/testbench.vhd

```
21
22      library IEEE;
23      use IEEE.STD_LOGIC_1164.ALL;
24
25
26      entity testbench is
27      --  Port ( );
28      end testbench;
29
30      architecture Behavioral of testbench is
31
32      component Automat is
33          Port ( r : in STD_LOGIC;
34                 clk : in STD_LOGIC;
35                 q : out STD_LOGIC_VECTOR (3 downto 0));
36      end component Automat;
37
38      signal r, clk:std_logic;
39      signal q:std_logic_vector (3 downto 0);
40
41      begin
42
43      UUT: Automat port map (r => r, clk => clk, q => q);
44
```

```
44
45      generate_clk:process
46
47      begin
48      clk <= '1'; wait for 1 ns;
49      clk <= '0'; wait for 1 ns;
50      end process;
51
52      r <= '1';
53
54      end Behavioral;
55
```

Rezultatul simularii: