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Store prefetch policies

Analysis and new proposals

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Abstract

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This work will be focusing on how to gain performance when executing programs on a CPU. More specifically the store instructions will be studied. The memory instructions often causes huge delays while waiting on data to be brought in from main memory to the L1 cache. If an out-of-order (OoO) CPU cannot be fed with useful instructions, cycles will be wasted. To try to over overcome this issue, my supervisor, Alberto Ros Bardisa, have come up with the idea to use predictors to try to predict which data to be needed in the feature and brought it in to the L1 cache in advance. This is similar to the branch predictor that has been around for a while, where the CPU is fed with instructions to start working in advance based on the prediction whether or not a branch is to be taken. In this case we guess on which data to be brought in to the L1 case instead of which instructions to be brought in, in advance. Of course you want the prediction to be correct, but even if we assume that it always prefetches useful data there might still be a problem: When to bring in the data? Too late an you still need to wait since the need of it occur before it is in place. Too early and it will be evicted from the L1 cache due to space issues and there will be a waiting time to brought it in again when the need occur. The latest will also be a waste of energy since we brought in something to be evicted before use. The question I will try to answer with this master thesis is when to prefetch data to gain optimal performance.

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