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Store prefetch policies

Analysis and new proposals

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Abstract

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This thesis is focusing on how to gain performance when executing programs on a CPU. More specifically the store instructions are studied. These instructions often cause huge delays while waiting on write permission for a particular data block. If an out-of-order (OoO) CPU fills up the entire store buffer with stores waiting for write permission, the CPU has to stall, and cycles are going to be wast. To over overcome this issue, the idea is to use predictors to try to predict which write permissions that are needed in the future and brought it to the L1 cache in advance. This method is similar to that of the branch predictor where the CPU is fed with instructions to start working in advance based on the prediction of whether or not a branch is to be taken. In this case, we guess which data to be brought in to the L1 case instead of which instructions to be retrieved, in advance. Naturally, you would want the prediction to be correct, but even if we assume that the predictor always grants needed write permission ahead of time there might still be a problem, and that is when to grant store permission for the data block. Too late and you still need to wait since the need for it occurs before it is in place. Too early and it is going to be evicted from the L1 cache due to space issues, and there are going to be an idle time bring it back in when the need occurs. Furthermore, it is also a waste of energy since we brought in something to be evicted before use. The question I aim to answer with this master thesis is when to prefetch data to gain optimal performance.

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