

|     |     |   |                                       |
|-----|-----|---|---------------------------------------|
|     |     |   |                                       |
| (b) | (i) | <ul style="list-style-type: none"><li>● increasing cores</li><li>● increasing clock speed</li><li>● increasing or adding cache</li><li>● increasing width of data bus</li></ul> | 1<br>Award 1 mark for any one bullet. |