

	(ii)	<ul style="list-style-type: none"><li>• allows multiple instructions simultaneously</li><li>• more instructions executed per second</li><li>• faster access time compared to slower main memory/increased number of cache hits</li><li>• more bits transferred in a single operation/less fetch executes required</li></ul>	1	<p>Award 1 mark for bullet that matches method stated in part (i).</p> <p>If mark for (i) not awarded, candidate can be awarded for suitable description.</p>
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