

Matrix Operation Instructions in RISC-V Processor

Project specification

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1 Introduction

Many matrix operations involve computing many simpler calculations on the components of the matrix. These calculations are often independent and can be performed in parallel. A processor would compute these sequentially but a specific hardware implementation would be able to compute them in parallel. Adding hardware-based matrix operations to a processor instruction set would allow programs to reduce the number of cycles needed to get the result and so reduce the time taken. As the average clock speed of CPUs has seen very little increase since the early 2000s moving more complicated operations to hardware allows for run time to decrease without decreasing cycle time.

This project aims to develop hardware that can perform matrix operations and integrate that into the instructions of a RISK-V processor to allow improvement in the execution time of matrix heavy programs.

2 Background

2.1 FPGAs

As this project will use a hardware implementation, a platform is needed that can allow fast development and iterations on hardware designs. An FPGA (Field Programmable Gate Array) is a semiconductor device based around a matrix of configurable logic blocks [2]. The user can define what logic function these blocks perform and how they are connected using HDL (Hardware Description Language) programming. Hardware can be designed in HDL and constructed on the FPGA without needing to manually build the circuit.

2.2 Matrix Operations

2.3 RISK-V and Rocket Chip

3 Objectives

3.1 Hardware-Based Matrix Operations

3.2 Integration to RISC-V Core

3.3 Comparison of Hardware Solution Against Software

4 Methodology

5 Timeline

6 Resources

This project will require hardware and software resources listed below as well as open source tools such as Rocket Chip.

1. FPGA Development Board - Nexys A7

This board will be used to synthesise the HDL generated by this project. It is on loan from the School of Engineering.

2. Vivado Design Suit

Provides tools to synthesise and analyse HDL for FPGAs. Educational licence through the School of Engineering

3. vivado-risk-v project [1]

An open-source project that generates RISC-V processors for FPGAs using Rocket Chip.

4. Linux Workstation PC

A PC capable of running the Vivado Design Suit tools and the Ubuntu 20.04 environment that is needed for the vivado-risk-v project. My PC fulfils these requirements.

7 Risks

Three main risks could harm this project. These are listed below along with mitigations and solutions.

1. Damage to FPGA Development Board

This board is on loan from the School of Engineering so a replacement could be obtained. To reduce the chance of damage the board will only be transported when necessary and kept in its protective packaging when not in use.

2. Damage to Workstation

Engineering computer labs could be used to run Vivado Design Suit and DCS labs can provide a Linux environment if needed.

3. Data Loss

Git version control will be used to track changes and all data relevant to the project will be backed up to GitHub providing an easy way to recover data. A log will be kept of the process to generate data such as the use of vivado-risk-v so it can be repeated if necessary.

8 Legal, Social, Ethical and Professional Issues

This project should not present any social, ethical or professional issues and does not require working with people. There is no intent to profit from this project so no legal issues should arise.

References

- [1] Tarassov, Eugene. `vivado-risk-v`. github.com/eugene-tarassov/vivado-risk-v.
- [2] Xilinx, AMD. What is an fpga? xilinx.com/products/silicon-devices/fpga/what-is-an-fpga.html. (Accessed October 2023).