Matrix Operation Instructions in RISC-V Processor

Project specification

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1 Introduction

Many matrix operations involve computing many simpler calculations on the components of the matrix. These calculations are often independant and can be performed in parralel. A processor would compute these sequentaly but a specific harware implementation would be able to compute them in parralell. Adding hardware based matrix operations to a processor instruction set would allow programs to reduce the number of cycles needed to get the result and so reduce the time taken. As the average clock speed of CPUs has seen very little increase since the early 2000s moving more complicated operations to hardware allows for run time to decrease without decreasing cycle time.

The aim of this project is to develop hardware that can perform matrix operations and integrate that into the instructions of a RISK-V processor to allow improvement in run time of matrix heavy programs.

2 Background

2.1 FPGAs

As this project will use a hardware implementation, a platform is needed that can allow fast development and interations on hardware designs. An FPGA is a semiconductor based arround a matrix of configurable logic blocks.(Xilinx)

2.2 RISK-V and Rocket Chip

2.3 Matrix Operations

3 Objectives

4 Project Managment

References

Xilinx, AMD. What is an fpga? https://www.xilinx.com/products/silicon-devices/fpga/what-is-an-fpga.html. (Accessed October 2023).