vgaclk

inclk0

inclk0 frequency: 50.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (dg)	DC (%)
c0	1007/2000	0.00	50.00

c0

inst   Cyclone IV E

PIN_23 — external_clock — INPUT/GND — 50MHZ_CLK_WIRE

c0_vgaclk — OUTPUT — VGA_CLKOUT_PIN7 — PIN_76

c0_vgaclk

vga_out

vgaclk
bit_from_ram

vr[1..0]
vg[1..0]
vb[1..0]
vsync
hsync
raddr[17..0]

inst2

vr[1] — OUTPUT — vr[1] — PIN_52
vr[0] — OUTPUT — vr[0] — PIN_50
vg[1] — OUTPUT — vg[1] — PIN_46
vg[0] — OUTPUT — vg[0] — PIN_43
vb[1] — OUTPUT — vb[1] — PIN_39
vb[0] — OUTPUT — vb[0] — PIN_34

w_vga_vsync — OUTPUT — vga_vsync — PIN_58
w_vga_hsync — OUTPUT — vga_hsync — PIN_54

m4_input

hsync
vsync
video
dotclk

waddr[17..0]
pixel_state
wren
leds0
leds1
leds2
leds3

inst5

PIN_136 — m4_hsync — INPUT/GND
PIN_133 — m4_vsync — INPUT/GND
PIN_129 — m4_video — INPUT/GND
PIN_127 — m4_dotclk — INPUT/GND

w_pixel_state
w_wren

NOT inst6

framebuffer

153600 bit RAM

data[0]
wraddress[17..0]
wren
rdaddress[17..0]
wrclock
rdclock

q[0]

inst1   Block Type: AUTO

bit_from_framebuffer

OUTPUT — FB_DATAOUT_PIN7 — PIN_74

rdaddress[17..0]

OUTPUT — DOTCLKP2_PIN64 — PIN_64

OUTPUT — LEDS0 — PIN_3
OUTPUT — LEDS1 — PIN_7
OUTPUT — LEDS2 — PIN_10
OUTPUT — LEDS3 — PIN_11

OUTPUT — PIXSTATE_PIN59 — PIN_59

waddr[0] — OUTPUT — WADDR0_PIN66 — PIN_66
waddr[1] — OUTPUT — WADDR1_PIN68 — PIN_68
waddr[2] — OUTPUT — WADDR2_PIN70 — PIN_70
waddr[3] — OUTPUT — WADDR3_PIN72 — PIN_70

waddr[17..0]

PIN_72