INTERSIL

IM5603/IM5623 Electrically Programmable 1024 Bit Bipolar Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - — Superior Reliability
  - — High Programming Yield
  - — Fast Programming Speed < 1 sec
  - — TTL Processing Compatibility
- Low Power Consumption 439 μW/bit
- Operating Speed
  - — Address to Output — 60nS
  - — Chip Enable to Output — 35nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - — 5603 Open Collector
  - — 5623 Active Pull-up
- Chip Enables Facilitate Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5603 and IM5623 are high speed, electrically programmable, fully decoded, bipolar 1024 bit read only memories organized as 256 words by 4 bits. On-chip address decoding, chip enable inputs and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

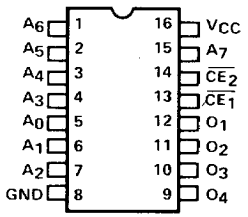
Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

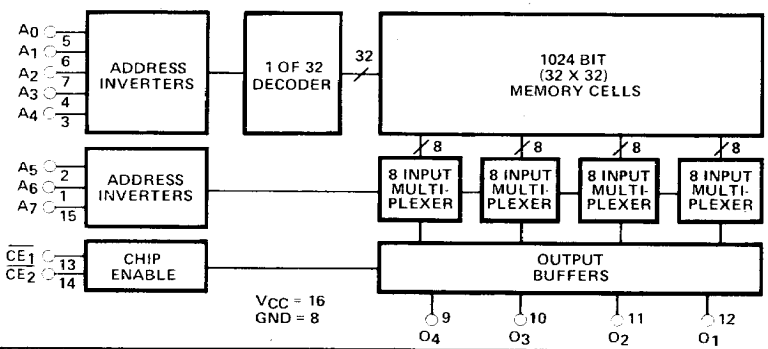
Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

PIN CONFIGURATION



TOP VIEW
(outline dwgs JE, PE, flatpak outline dwg FE)

BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5603	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5603CFE IM5603MFE*
	16 Pin Plastic DIP	0°C to +75°C	IM5603CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial −55°C to +125°C Military	IM5603CJE IM5603MJE*
IM5623	16 Pin Flatpack	0°C to +75°C Commercial −55°C to +125°C Military	IM5623CFE IM5623MFE*
	16 Pin Plastic DIP	0°C to +75°C	IM5623CPE
	16 Pin Cerdip DIP	0°C to +75° C Commercial −55°C to +125°C Military	IM5623CJE IM5623MJE*

* If 883B processing is desired add /883B to order number.

Per Dent Robins, these IM5603 are all "A" Versions

TRUTH TABLE

ADDRESS INPUTS A_0-A_7	CHIP ENABLE INPUTS $\overline{CE_1}$	CHIP ENABLE INPUTS $\overline{CE_2}$	ANY OUTPUT O_1-O_4
Any one of 256 possible addresses	L	L	H-if the bit uniquely associated with this output and address has been electrically programmed. L - if it has not been programmed.
Any one of 256 possible addresses	H X	X H	All outputs are forced to a high impedance state regardless of address.

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input Voltage Applied ..... −1.5V to 5.5V
Output Voltage Applied ..... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) ..... 210 mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature Range*
(IM5603C and IM5623C) ..... 0°C to +75°C
(IM5603M and IM5623M) ..... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C MIN	TYP	MAX	LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C MIN	TYP	MAX	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		V_{CE} = 0.4V
I_{RA}	Address Input Leakage Current		5	40		5	60	µA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5	40		5	60		V_{CE} = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA, $V_{\overline{CE1}} = V_{\overline{CE2}}$ = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		90	130		90	130	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1	40		<1	100	µA	V_O = 5.5V, $V_{\overline{CE1}}$ or
I_O (High R State)	Output Leakage Current		<−1	−40		<−1	−100		V_O = 0.4V, $V_{\overline{CE2}}$ = 2.4V
C_{IN}	Input Capacitance		5			5		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7			7			V_O = 2.0V, V_{CC} = 0V

The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE1}$ and $\overline{CE2}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1	100		<1	100	µA	V_O = 5.5V
V_{OH} (IM5603)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_{OH} = −0.4 mA
V_{OH} (IM5623)	Output High Voltage	2.4	3.2		2.4	3.2			I_{OH} = −2.4 mA (IM5623C) I_{OH} = −1.0 mA (IM5623M)
I_{SC} (IM5603)	Output Short Circuit Current	−1.0	−3.0	−6.0	−1.0	−3.0	−6.0	mA	V_O = 0V
I_{SC} (IM5623)	Output Short Circuit Current	−15	−30	−60	−15	−30	−60		V_O = 0V

NOTE: Typical characteristics are for V_{CC} = 5.0V T_A = 25°C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V T_A = 25°C MIN	LIMITS V_{CC} = 5.0V ±5% T_A = 0°C to +75°C MIN	LIMITS V_{CC} = 5.0V ±10% T_A = −55°C to +125°C MIN	MAX	UNITS
t_{aa}	Access Time (Via Address Inputs) (See Figure 1)	20	60	20	70	20	80	ns
t_{dis}	Output Disable Time* (See Figure 2)	10	35	10	50	10	60	ns
t_{en}	Output Enable Time* (See Figure 2)	5	35	5	50	5	60	ns

*NOTE: Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

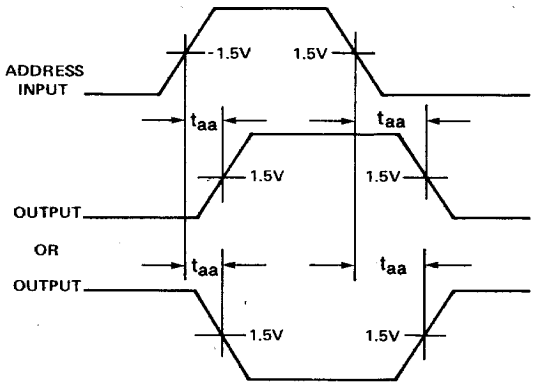


FIGURE 1: Access Time Via Address Inputs

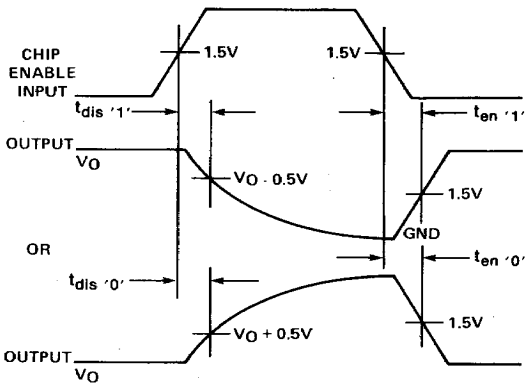


FIGURE 2: Output Enable And Disable Times

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SWITCHING TIME TEST CONDITIONS

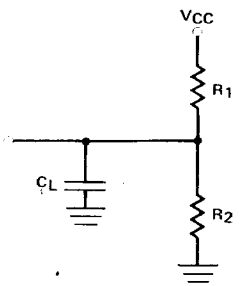


FIGURE 3: Output Load Circuit

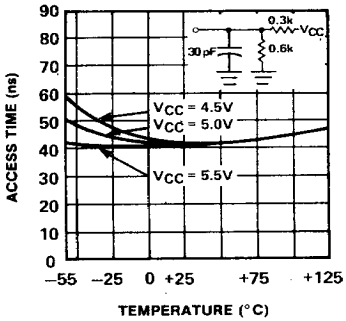
SWITCHING PARAMETER	IM5603 R_1	IM5603 R_2	IM5603 C_L	IM5623 R_1	IM5623 R_2	IM5623 C_L
t_{aa}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{dis} '1'	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{dis} '0'	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{en} '1'	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{en} '0'	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

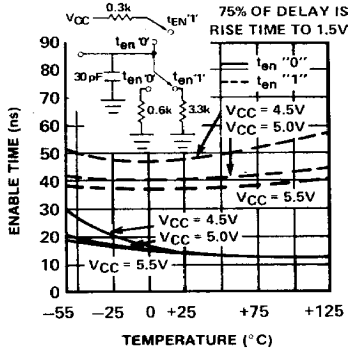
Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

TYPICAL SWITCHING CHARACTERISTICS

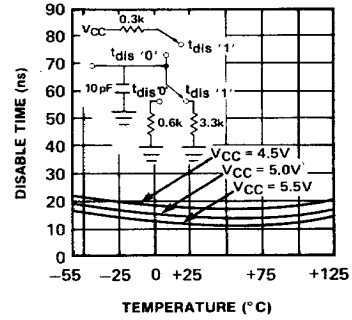
IM5603 ADDRESS TO OUTPUT ACCESS DELAY (T_{AA}) VS TEMPERATURE



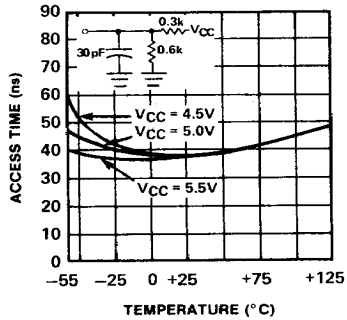
IM5603 CHIP ENABLE TO OUTPUT ACCESS DELAY (t_{EN}) VS TEMPERATURE



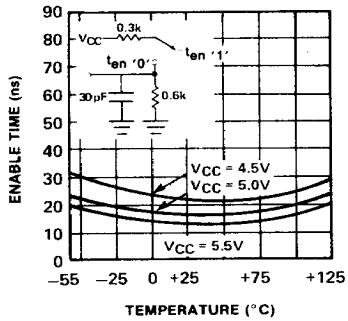
IM5603 CHIP ENABLE TO OUTPUT DISABLE TIME DELAY (t_{DIS}) VS TEMPERATURE



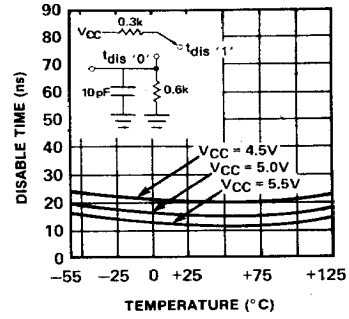
IM5623 ADDRESS TO OUTPUT ACCESS DELAY (t_{AA}) VS TEMPERATURE



IM5623 CHIP ENABLE TO OUTPUT ACCESS DELAY (t_{EN}) VS TEMPERATURE



IM5623 CHIP ENABLE TO OUTPUT DISABLE TIME DELAY (t_{DIS}) VS TEMPERATURE



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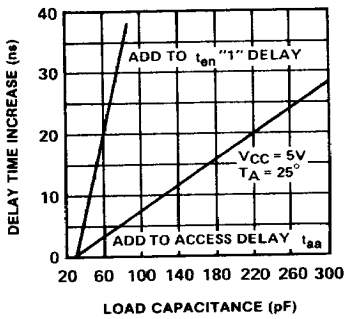
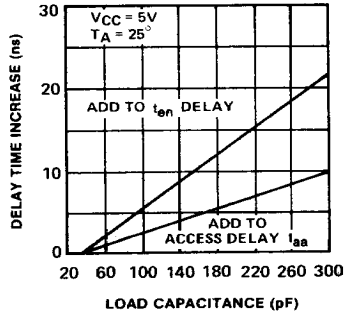
IM5603 DELAY INCREASE WITH LOAD CAPACITANCE

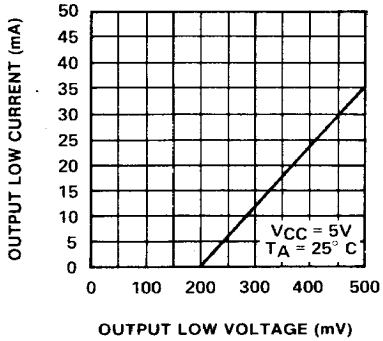


IM5623 DELAY INCREASE WITH LOAD CAPACITANCE

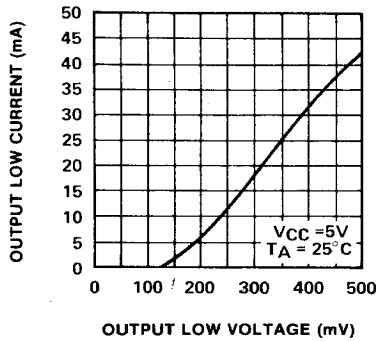


TYPICAL DC CHARACTERISTICS

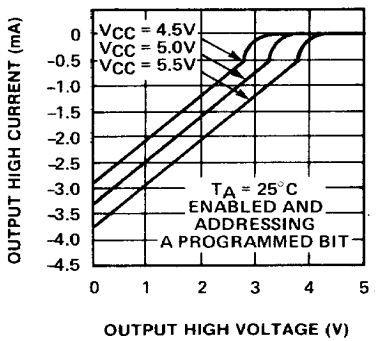
IM5603 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})



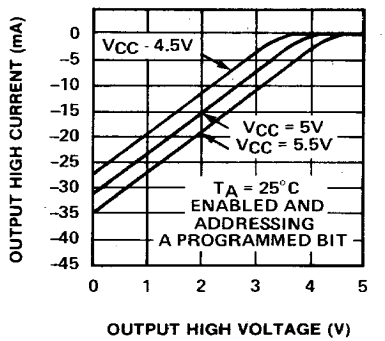
IM5623 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})



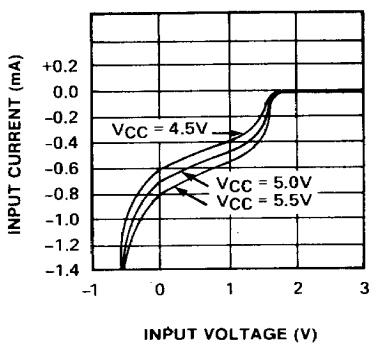
IM5603 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})



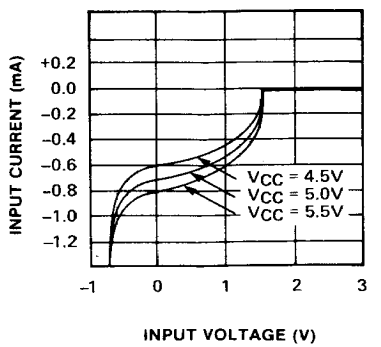
IM5623 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})



IM5603 OR IM5623 CHIP ENABLE INPUT CURRENT VS INPUT VOLTAGE



IM5603 OR IM5623 ADDRESS INPUT CURRENT VS INPUT VOLTAGE



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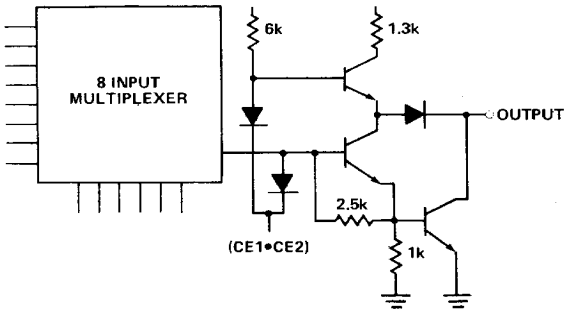
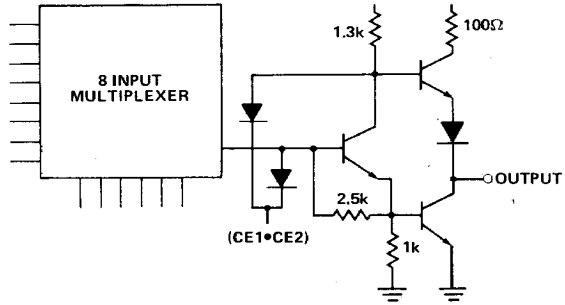
OUTPUT STAGE SCHEMATICS

IM5603



IM5623



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