

Lab 4: Performance
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Matmul with intadd and intmul for size 128:

69,166.04 msec	task-clock:u	1.000 CPUs utilized
0	context-switches:u	0.000 K/sec
0	cpu-migrations:u	0.000 K/sec
30	page-faults:u	0.000 K/sec
138,267,789,131	cycles:u	1.999 GHz
86,580,653,878	instructions:u	0.63 insn per cycle
26,682,937,473	branches:u	385.781 M/sec
636,034,870	branch-misses:u	2.38% of all branches

69.177124220 seconds time elapsed

$$T = \frac{\text{Instructions}}{\text{Program}} * \frac{\text{Clock Cycles}}{\text{Instruction}} * \frac{\text{Seconds}}{\text{Clock Cycle}}$$

$$T = \frac{86,580,653,878 \text{ instructions}}{0.63 \text{ ins/cycle} * 1997000000 \text{ seconds/cycle}} = 68.75 \text{ seconds}$$

Percent Diff = 0.619348%

Matmul with arm MUL and ADD for size 128:

88.54 msec	task-clock:u	0.698 CPUs utilized
0	context-switches:u	0.000 K/sec
0	cpu-migrations:u	0.000 K/sec
30	page-faults:u	0.339 K/sec
175,050,191	cycles:u	1.977 GHz
43,376,323	instructions:u	0.25 insn per cycle
3,806,681	branches:u	42.994 M/sec
139,495	branch-misses:u	3.66% of all branches

0.126871557 seconds time elapsed

$$T = \frac{\text{Instructions}}{\text{Program}} * \frac{\text{Clock Cycles}}{\text{Instruction}} * \frac{\text{Seconds}}{\text{Clock Cycle}}$$

$$T = \frac{43,376,323 \text{ instructions}}{0.25 \text{ ins/cycle} * 1977000000 \text{ seconds/cycle}} = 0.0878 \text{ seconds}$$

Percent Diff = 36.4432% difference