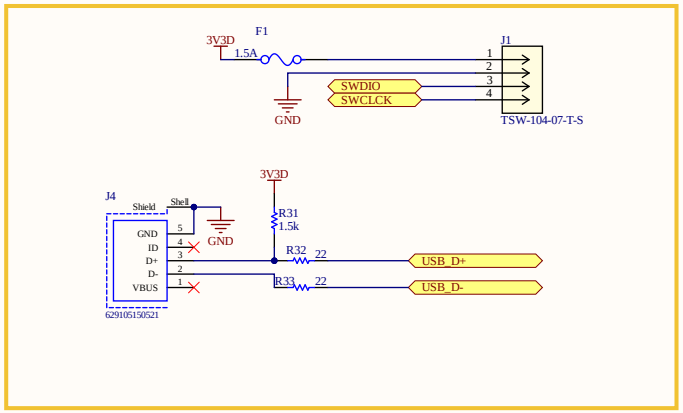
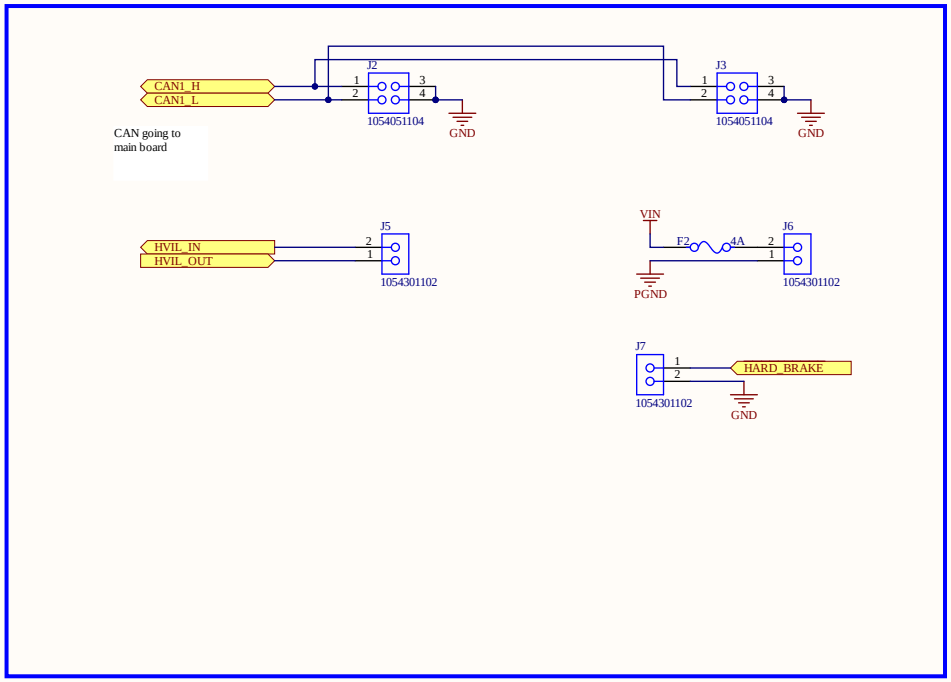
Debug Connections

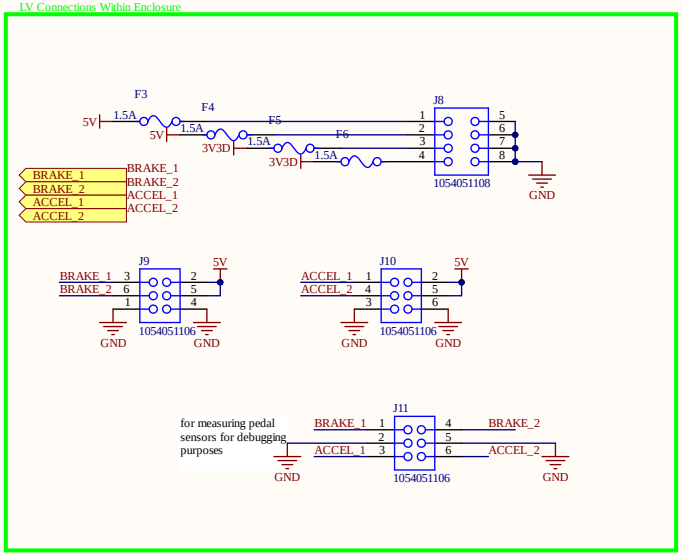


System Connections

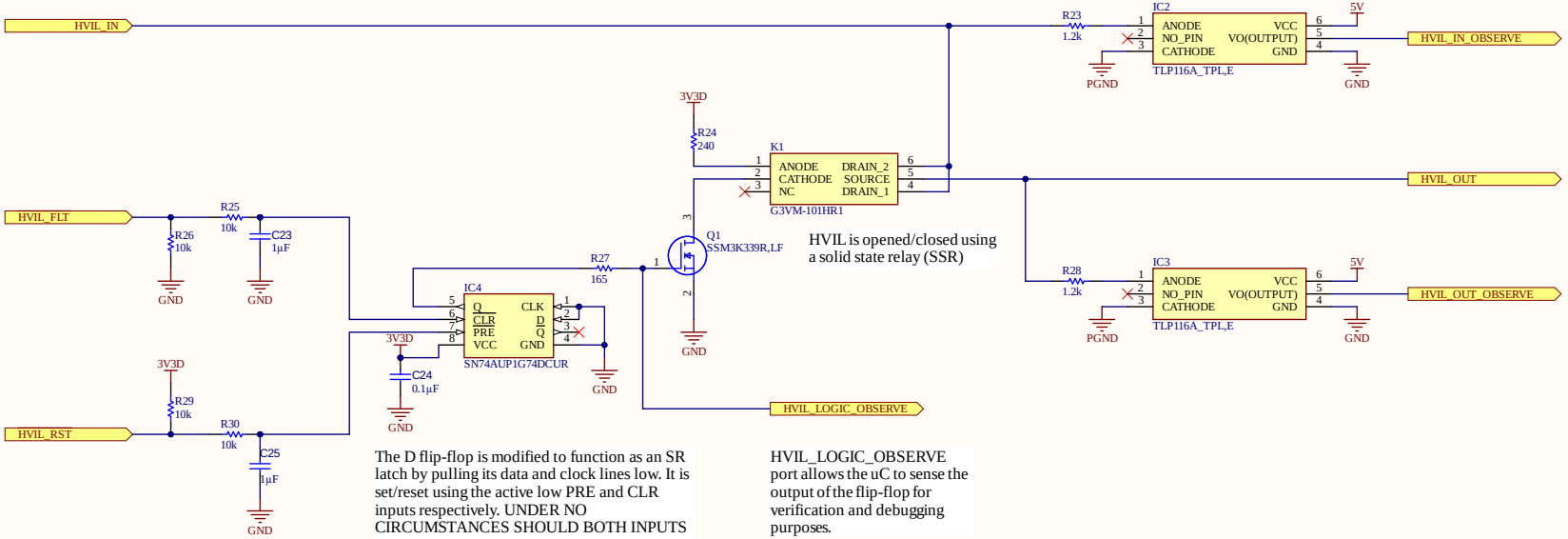
Place connectors that go to other boards in here



LV Connections Within Enclosure



Title: IO Board Connectors		
Size: A3	Number:	Revision:
Date: 9/23/2020		Sheet of
File: C:\Users\..\Connectors.SchDoc		Drawn By:



To ensure proper isolation between PGND and GND, optoisolators are used to monitor HVIL_IN and HVIL_OUT

HVIL is opened/closed using a solid state relay (SSR)

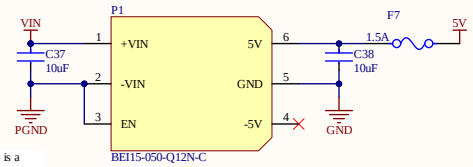
The D flip-flop is modified to function as an SR latch by pulling its data and clock lines low. It is set/reset using the active low PRE and CLR inputs respectively. UNDER NO CIRCUMSTANCES SHOULD BOTH INPUTS BE PULLED LOW AT THE SAME TIME.

HVIL_LOGIC_OBSERVE port allows the uC to sense the output of the flip-flop for verification and debugging purposes.

Title: IO Board Interlock		
Size: A3	Number:	Revision:
Date: 9/23/2020		Sheet of
File: C:\Users\..\Interlock.SchDoc		Drawn By:

PGND AND GND(SGND) ISOLATION MUST BE MAINTIANED THROUGHOUT THE SCHEMATIC!!

Isolated DC Converter 2 Output 5V
-5V 1.5A, 1.5A 9V - 36V Input

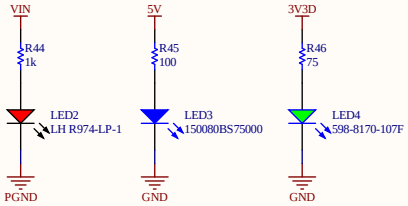


The BEI15-050-Q12N-C isolated DC/DC converter takes in 24V relative to PGND and provides 5V and GND (signal ground) to the other components in the schmetic. The VIN/PGND and 5V/SGND isolation provides protection upto 2000VDC.

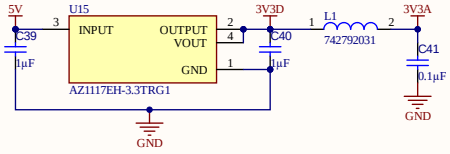
The BEI15-050-Q12N-C is a negative logic model and turns on when EN is grounded with respect to -VIN

Bypass capacitors must be placed close to pins

Power Indicator LEDs



AZ1117EH-3.3TRG1 Linear Regulator 3.3V 1A Output 70dB PSSR

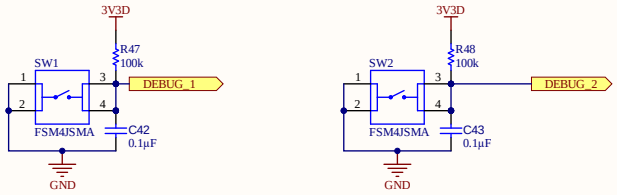


3V3A should be used to power and provide a voltage reference to sensitive analog components such as ADCs.

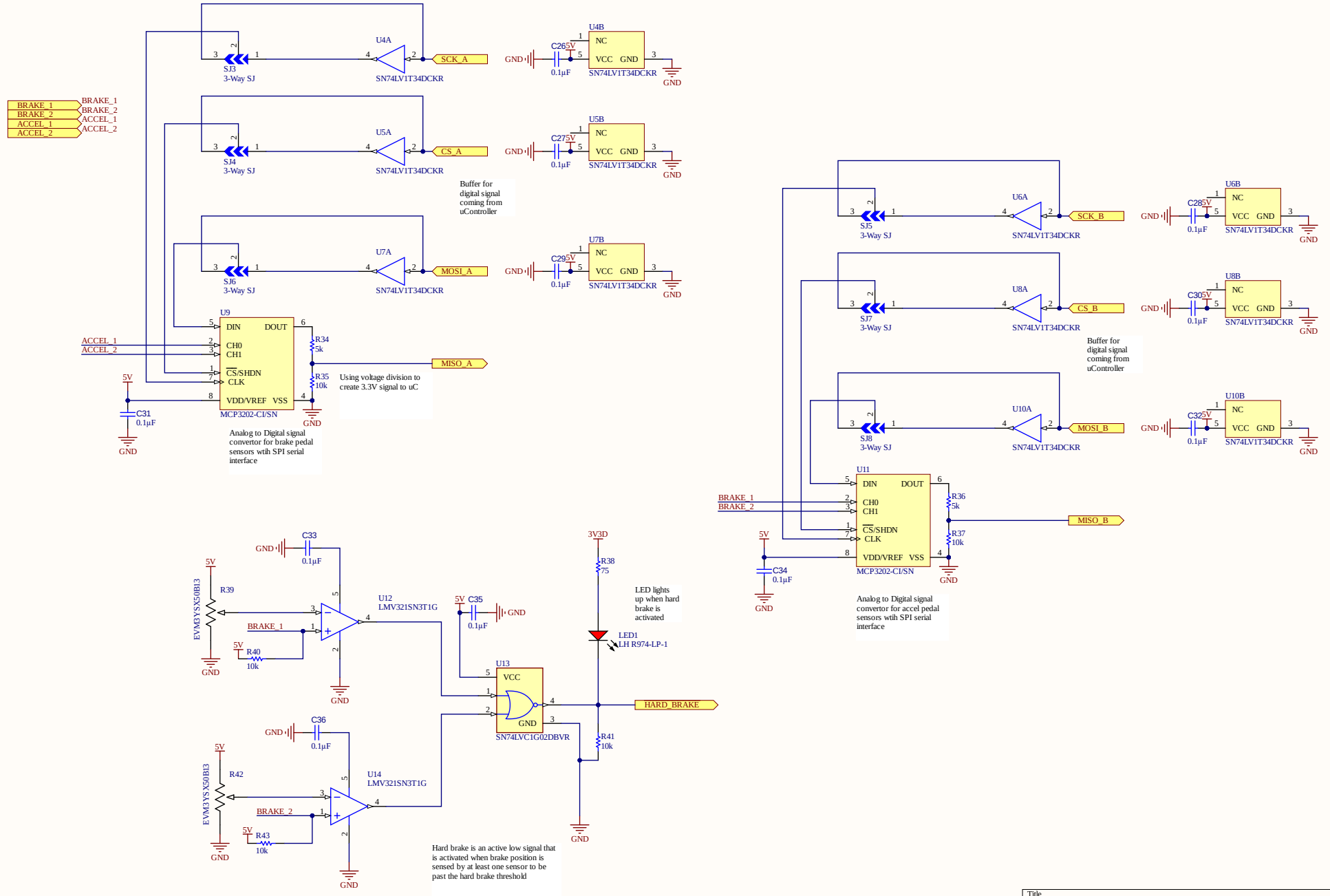
A ferrite bead is used to isolate the analog voltage rail from AC interference induced by switching on the digital rail. The 742792031 reaches a maximum impedance at 200MHz and the 180MHz frequency of the STM32 is within the resistive band of the ferrite bead.

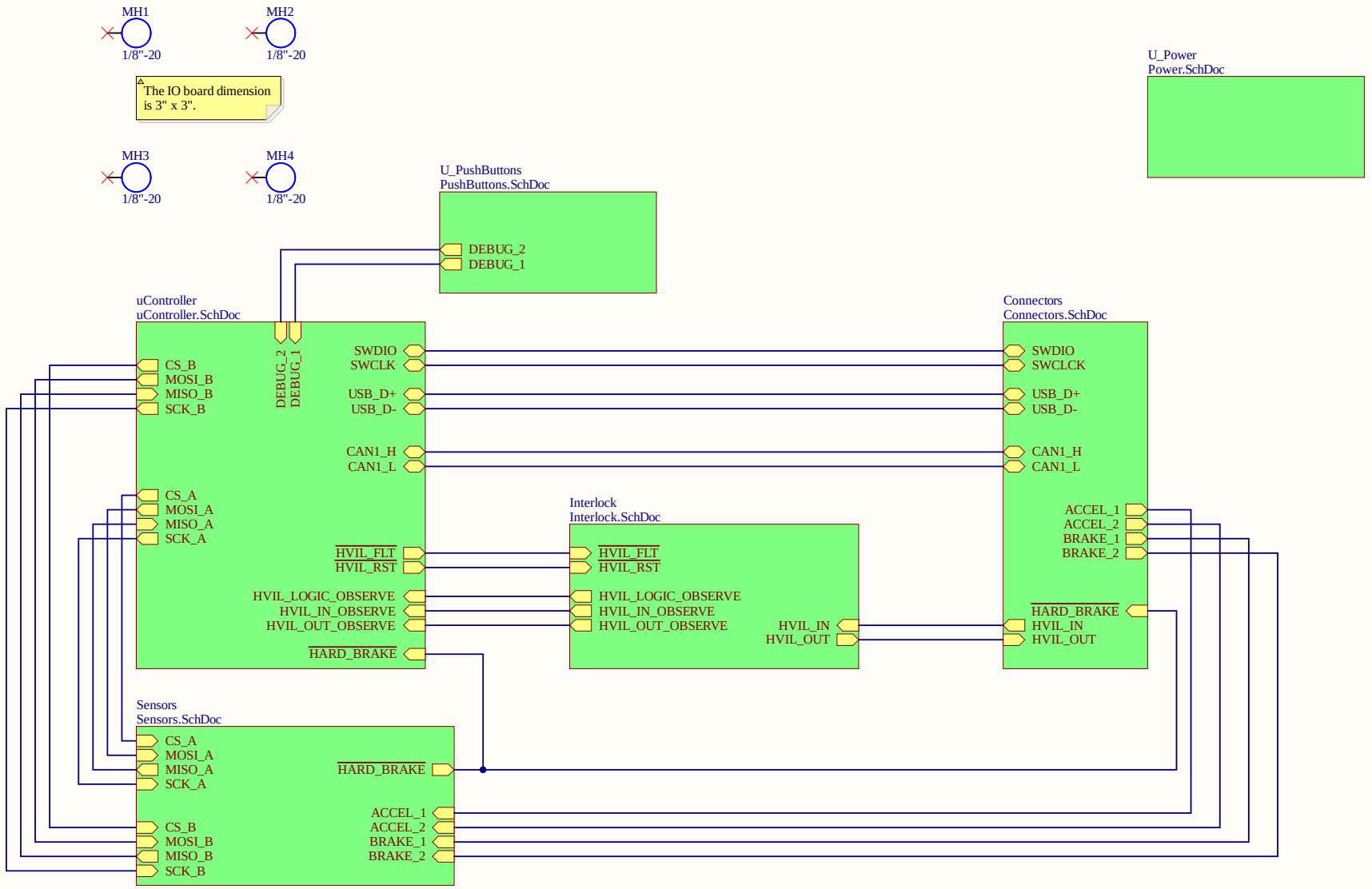
Title: IO Board Power		
Size: A3	Number:	Revision:
Date: 9/23/2020		Sheet of
File: C:\Users\..\Power.SchDoc		Drawn By:

Pushbutton uC GPIO Input for manually opening interlock



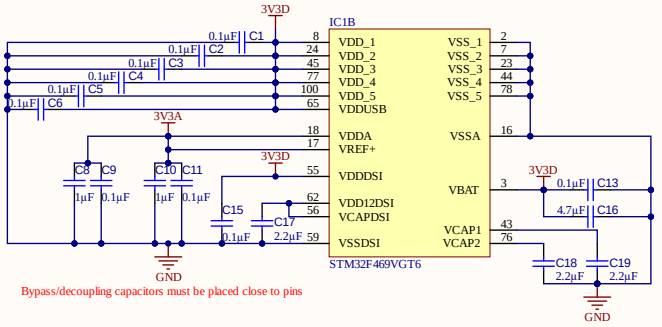
Title	IO Board Push Button	
Size: A3	Number	Revision
Date: 9/23/2020		Sheet of
File: C:\Users\..\PushButtons.SchDoc		Drawn By:


BRAKE_1
BRAKE_2
ACCEL_1
ACCEL_2
BRAKE_1
BRAKE_2
ACCEL_1
ACCEL_2
U4A
SJ3
3-Way SJ
SN74LV1T34DCKR
SCK_A
U4B
C26
0.1µF
SN74LV1T34DCKR
U5A
SJ4
3-Way SJ
SN74LV1T34DCKR
CS_A
U5B
C27
0.1µF
SN74LV1T34DCKR
Buffer for digital signal coming from uController
U7A
SJ6
3-Way SJ
SN74LV1T34DCKR
MOSI_A
U7B
C29
0.1µF
SN74LV1T34DCKR
U9
DIN
DOUT
CH0
CH1
CS/SHDN
CLK
VDD/VREF
VSS
MCP3202-CI/SN
ACCEL_1
ACCEL_2
R34
5k
R35
10k
MISO_A
Using voltage division to create 3.3V signal to uC
C31
0.1µF
Analog to Digital signal convertor for brake pedal sensors with SPI serial interface
U6A
SJ5
3-Way SJ
SN74LV1T34DCKR
SCK_B
U6B
C28
0.1µF
SN74LV1T34DCKR
U8A
SJ7
3-Way SJ
SN74LV1T34DCKR
CS_B
U8B
C30
0.1µF
SN74LV1T34DCKR
Buffer for digital signal coming from uController
U10A
SJ8
3-Way SJ
SN74LV1T34DCKR
MOSI_B
U10B
C32
0.1µF
SN74LV1T34DCKR
U11
DIN
DOUT
CH0
CH1
CS/SHDN
CLK
VDD/VREF
VSS
MCP3202-CI/SN
BRAKE_1
BRAKE_2
R36
5k
R37
10k
MISO_B
C34
0.1µF
Analog to Digital signal convertor for accel pedal sensors with SPI serial interface
C33
0.1µF
EVM3YSX50B13
R39
U12
LMV321SN3T1G
BRAKE_1
R40
10k
C35
0.1µF
3V3D
R38
75
LED lights up when hard brake is activated
LED1
LH R974-LP-1
U13
VCC
GND
SN74LVC1G02DBVR
HARD_BRAKE
R41
10k
C36
0.1µF
EVM3YSX50B13
R42
U14
LMV321SN3T1G
BRAKE_2
R43
10k
Hard brake is an active low signal that is activated when brake position is sensed by at least one sensor to be past the hard brake threshold
Title
IO Board Sensors
Size
A3
Number
Revision
Date:
9/23/2020
Sheet of
File:
C:\Users\..\Sensors.SchDoc
Drawn By:



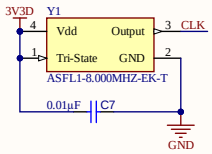
Title: IO Board Top Level		
Size: A4	Number:	Revision:
Date: 9/23/2020		Sheet of
File: C:\Users\..\TopLevel.SchDoc		Drawn By:

uController Power

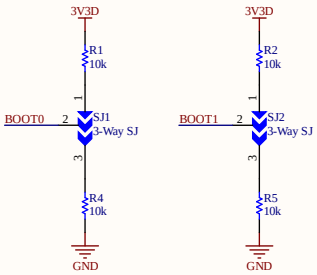


Bypass/decoupling capacitors must be placed close to pins

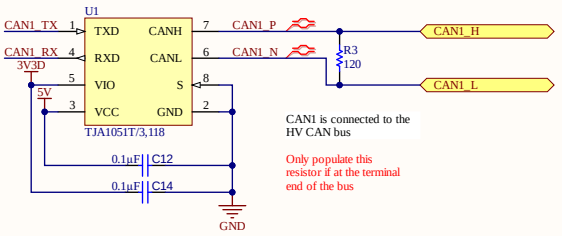
8.000MHz Clock



Boot Mode Selectors



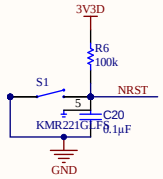
CAN Transceiver



CAN1 is connected to the HV CAN bus

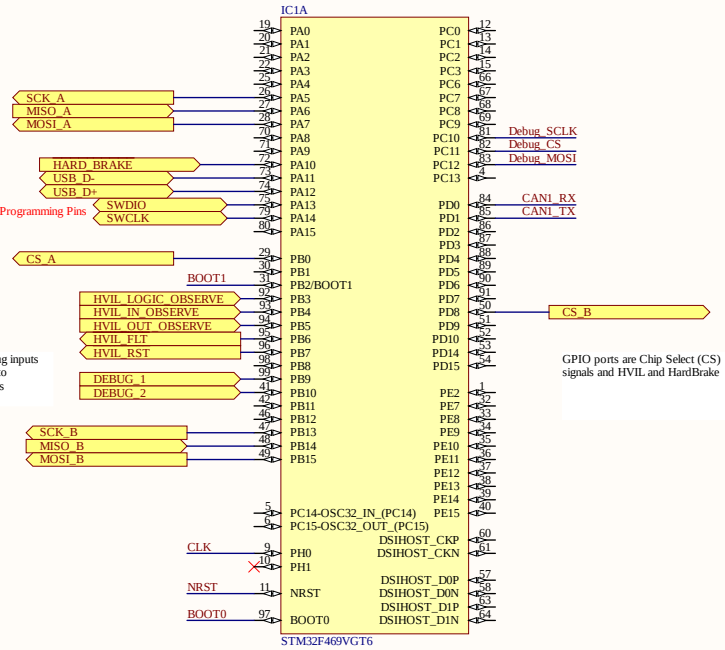
Only populate this resistor if at the terminal end of the bus

Reset Switch



You may want to have a few debuging pushbuttons to test functionality like manually opening or closing the interlock, etc. I recommend adding this in another sheet and connecting it at the TopLevel so that you can continue to use the Altium sinppets tool without any issues.

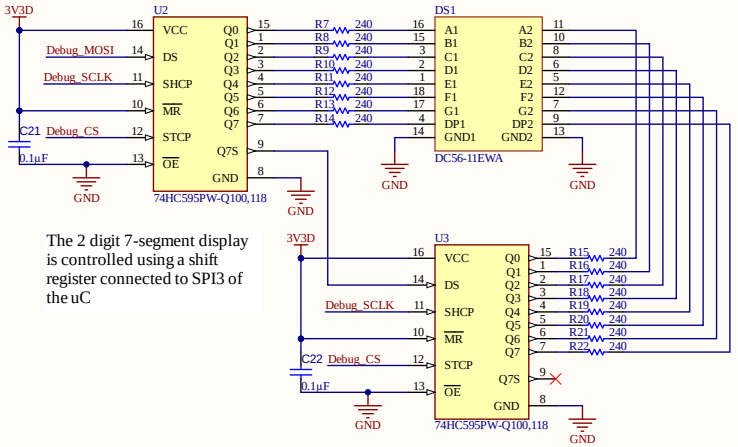
uController I/O



HVIL Debug inputs connected to pushbuttons

GPIO ports are Chip Select (CS) signals and HVIL and HardBrake

2 Digit 7-Seg Debug Display



The 2 digit 7-segment display is controlled using a shift register connected to SPI3 of the uC

Title: IO Board uController		
Size: A3	Number	Revision
Date: 9/23/2020		Sheet of
File: C:\Users\..\uController.SchDoc		Drawn By: