

Dynamic Modeling and Controller Design of Flyback Converter

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The accurate dynamic modeling and quantitative controller design for an isolated converter with optocoupler isolation in its feedback loop are considered to be difficult issues, since the transfer characteristics of some blocks are highly nonlinear and difficult to be modeled analytically. First a current-mode controlled flyback converter with an optically isolated feedback path is designed. Then the equivalent control system block diagram is constructed, and its block transfer functions are found. To increase the accuracy, the dynamic models of some critical blocks are estimated from measurements. In order to facilitate the controller design, the model simplification is further made. Finally, based on the reduced dynamic model, a quantitative design procedure is derived to find the parameters of the voltage controller to meet the prescribed regulating specifications. Validity of the estimated dynamic model and the proposed controller design approach is demonstrated by some simulation and experimental results.

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I. INTRODUCTION

Among the currently-existing transformer-coupled switching-mode DC-to-DC converters, the flyback converter is the simplest topology, since no choke is required, only one power switch is used and the high-frequency power transformer with unifilar windings is employed. In addition to these structural advantages, it also possesses the merits of easy to obtain wide-range output voltage and multiple output voltage with good transient response [1–5]. As a result, it has been extensively designed for many applications [1, 5], and some physical dynamic modeling and controller design techniques have been devised for improving its dynamic behavior [2–5].

It is known that an isolated feedback path is indispensable to achieve the complete galvanic isolation from input to output for an isolated closed-loop controlled converter. The possible arrangements of isolating feedback loops and their features have been thoroughly reviewed in [6]. It is shown that the technique of isolating the analog error signal using optocoupler is perhaps the most popular and widely used one for providing the necessary isolation between the error amplifier and the pulsewidth modulation (PWM) modulator. Since the transfer characteristic of the optocoupler-based isolation circuit is highly nonlinear, the control system block diagram with accurate block transfer functions of an isolated flyback converter is difficult to construct. During the past years, although some approaches [2–5, 7–11] have been applied to find the dynamic model of the power stage of flyback converter, it still lacks of studies for obtaining the accurate dynamic model of a whole isolated converter system with optocoupler feedback path. In addition, most of the existing controller design methods [1–5] emphasize treating the closed-loop stability using the concept of gain and phase margins, and no quantitative design approaches are provided to find the controller parameters according to the prescribed voltage regulation control specifications.

Here the circuit design of a current-mode controlled flyback converter with optically isolated feedback path is first described. Then a suitable equivalent block diagram for the control system diagram is constructed. An estimation approach is proposed to find the transfer functions of some critical blocks. The dynamic behavior of power stage is much simplified by applying the current-mode control. The compensation and model reduction techniques are employed to establish the reduced plant model for the voltage controller design. Based on the reduced dynamic model, a quantitative design procedure is derived to find the parameters of the voltage controller according to prescribed regulating specifications [10]. Some simulation and experimental results are provided to demonstrate the validity of the proposed dynamic modeling and controller design methods.

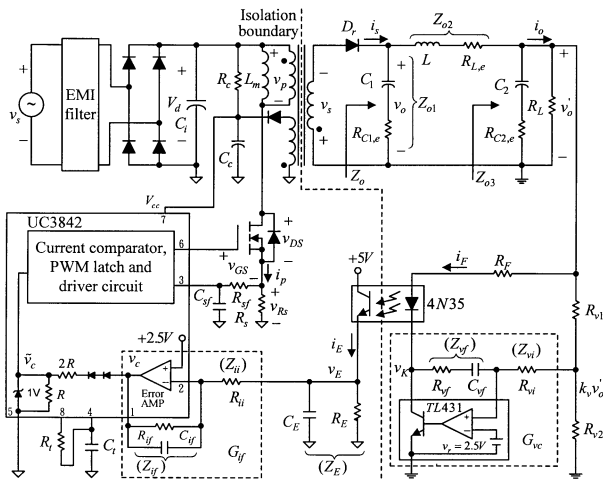


Fig. 1. Schematic diagram of the current-mode controlled flyback converter with optically isolated feedback loop.

II. DESIGN OF AN ISOLATED FLYBACK CONVERTER

The detailed system configuration of a current-mode controlled flyback converter with optically isolated feedback loop is drawn in Fig. 1. The circuit structure, analysis and design of this converter system are described as follows [12].

Specifications:

Input voltage: $v_s = 85 \sim 262$ Vac rms or $100 \sim 370$ Vdc,

Nominal output voltage: $V_0 = 16$ Vdc,

Output current range: $0.5 \text{ A} \leq I_0 \leq 2.5 \text{ A}$,

Maximum duty ratio: $D_{\max} = 0.4$,

System efficiency at full load $\eta \geq 80\%$,

Switching frequency $f_s = 100$ kHz.

A. Input Rectifier and Starting Circuits

A full-bridge rectifier (600 V/1 A) with inrush current suppressing thermistor and common-mode electromagnetic interference (EMI) filter in its input side is employed. For the hold-up time $T_{\text{hold}} = 8.3$ ms at $v_s = 110$ Vac rms, its filtering capacitor is found using known system parameters to be $C_i = 68 \mu\text{F}$ (400 V). According to the minimum starting current requirement (1 mA) and the maximum allowable power dissipation at maximum input voltage given by the UC3842 IC, the start-up resistance is set as $R_c = 100 \text{ k}\Omega$ (1 W), and the start-up capacitance is determined to be $C_c = 47 \mu\text{F}$ (25 V) for the chosen start-up time 8.3 ms.

B. Current-Mode Controlled Flyback Converter

1) *Current-Mode Controller*: It is known that the current-mode controlled converter possesses many advantages, such as dynamic model simplification, with input voltage feedforward characteristic, ease of making current limiting and ease of parallel

operation, ..., etc. There are many current-mode control techniques and current sensing approaches been developed [1, 6]. To simplify the circuit configuration, the commercially available IC UC3842 is employed here to implement the current-mode switching control of the flyback converter. The fixed-frequency with turn-on at clock time current control is adopted for regulating the peak switch current to closely follow its command, which is generated from the outer voltage control loop. The voltage across the current shunt $R_s = 0.56 \Omega$ is low-pass filtered ($R_{sf} = 1 \text{ k}\Omega$, $C_{sf} = 0.82 \text{ nF}$) to suppress the high voltage spike and fed back for making current control. With the circuit arrangement set in UC3842 and its excellent current regulating ability, the peak switching current \hat{i}_p is related to its command v_c by the relationship of $v_c = 3k_s\hat{i}_p + 1.4$, where the conversion factor k_s is determined by the filtered current sensing circuit and its accurate value will be found using the estimation approach introduced later. It is worthy of mentioning that owing to the maximum duty ratio of 0.4 being set, the slope compensation for eliminating the inherent unstable phenomenon of peak current-mode control at duty ratio exceeding 0.5 is not required.

2) *Flyback Converter*: According to the switching nature of flyback converter [1], the peak voltage of the switch, which occurs at turn-off, must be chosen as

$$V_{DSm} = V_{d,\max} + n(v_0 + V_{rf}) \quad (1)$$

where $V_{d,\max}$ denotes the maximum value of V_d , V_{rf} is the on-state voltage of diode D_r and n is the primary-to-secondary turn ratios. The peak switch current rating determined at turn-on is $I_{Dm} = \hat{i}_s/n$, with \hat{i}_s being the transformer secondary peak current. The estimate of I_{Dm} can be further approximately expressed in terms of the maximum output power P_{om} and the maximum duty ratio D_{\max} to be

$$I_{Dm} = \frac{P_{om}}{\eta_T V_{d,\min} D_{\max}} + \frac{V_{d,\min} D_{\max}}{2L_m f_s} \quad (2)$$

where η_T denotes the overall efficiency including the transformer, the rectifier, and the output filters. It is reasonably assumed $\eta_T = \sqrt{\eta}$ here for making the estimation of I_{Dm} . $L_m (= 710 \mu\text{H})$, the transformer is designed below) is the primary magnetizing inductance of the isolation transformer. Applying the known system parameters, it is found the $V_{DSm} = 450 \text{ V}$ (occurred at $v_s = 370 \text{ Vdc}$) and $I_{Dm} = 1.3 \text{ A}$ (occurred at $v_s = 100 \text{ Vdc}$). Accordingly the metal-oxide semiconductor field-effect transistor (MOSFET) IRF 830 (500 V, 4.5 A) is adopted.

The transformer in a flyback converter plays many roles: a) as an energy storage choke; b) Galvanic isolation in power stage; and c) current limiting inductor. Since it is driven in unidirectional core excitation, it possesses a considerable dc current

component. Thus, it is more difficult to design than other types of isolated converters. Generally, this will result in a core with larger volume and air gap. According to the given system data, a systematic transformer design procedure is derived in [12]; the results are summarized as follows.

Core: TDK EI-28

$N_1 = 77$ turns, AWG #32, 339 cm

$N_2 = 16$ turns, AWG #21 \times 2, 83 cm

$N_3 = 12$ turns, AWG #29, 62 cm.

The magnetizing inductance referred to primary side is measured to be $L_m = 710 \mu\text{H}$.

C. PWM Modulator and Isolated Feedback Loop

For the chosen switching frequency of $f_s = 100$ kHz, the components of timing network are determined following the formula in data sheet of UC3842 to be $R_t = 5.2 \text{ k}\Omega$ and $C_t = 3.3 \text{ nF}$.

In the feedback loop of a completely isolated current-mode controlled converter, the necessary components include the voltage sensing divider, precision voltage reference, the voltage error calculation circuit, the current regulator, and the optocoupler. The TL431-based optically isolated feedback loop configuration is shown in Fig. 1. The TL431, which consists of voltage reference, amplifier and driver, is designed as a shunt regulator for modulating the LED current in response to the feedback voltage error. Then an error voltage is yielded from the optocoupler output, and the current command is further generated from the compensator G_{if} , which is implemented using the compensation network ($Z_{ii} = R_{ii}$ and $Z_{if} = R_{if} / (1/C_{if}s) = R_{if} / (R_{if}C_{if}s + 1)$) connected externally. Through properly choosing the low-pass filter capacitor C_E and resistor R_E and the current compensation network according to the power stage dynamic behavior, the excellent current mode control is yielded. The designed circuit elements of this part are listed as follows:

$$\begin{aligned} R_F = 320 \Omega, \quad R_{v1} = 1.1 \text{ k}\Omega, \quad R_{v2} = 203 \Omega, \\ R_E = 470 \Omega, \quad C_E = 10 \text{ nF}. \end{aligned} \quad (3)$$

The design of the elements Z_{ii} , Z_{if} , Z_{vi} and Z_{vf} of the current controller and voltage controller will be introduced later after the dynamic converter model having been found.

D. Output Filters

A $LC - \pi$ output filter is adopted here to yield low-ripple dc output voltage. The values of inductance and capacitances accompanying with their equivalent series resistances are listed as follows:

$$\begin{aligned} L = 2 \mu\text{H}, \quad R_{L,e} = 5 \text{ m}\Omega, \\ C_1 = C_2 = 1000 \mu\text{F}, \quad R_{c1,e} = R_{c2,e} = 0.05 \Omega. \end{aligned} \quad (4)$$

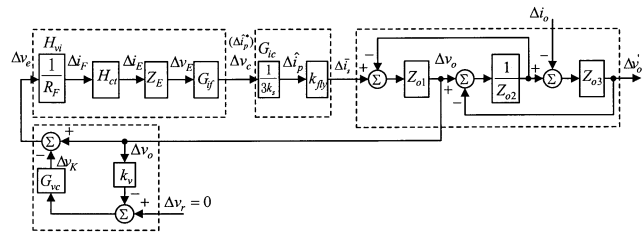


Fig. 2. Transfer function block diagram of proposed flyback converter.

Since the values of L and $R_{L,e}$ are comparatively small, the dynamic modeling of the output filters can be simplified within the main dynamic frequency range. The related dynamic modeling process is treated in detail in the next section.

III. CONTROL SYSTEM BLOCK DIAGRAM ESTABLISHMENT

A. Exact Configuration

Carefully observing, it is found that the dynamic behavior of the converter system shown in Fig. 1 can be reasonably expressed by the control system block diagram drawn in Fig. 2. The correspondence between the circuit components and their transfer functions is briefly described as follows.

1) Voltage Sensing and Feedback Controller:

$$k_v = \frac{R_{v2}}{R_{v1} + R_{v2}} \quad (5)$$

where the voltage reference, amplifier and driver included in the TL431 are employed to realize the output voltage feedback controller. The controller type is determined by the branches Z_{vi} and Z_{vf} connected externally. Here the following PI-type (proportional-integral) controller for G_{vc} is adopted:

$$G_{vc} = \frac{Z_{vf}}{Z_{vi}} = K_P + \frac{K_I}{s} \quad (6)$$

with

$$K_P = \frac{R_{vf}}{R_{vi}}, \quad K_I = \frac{1}{R_{vi}C_{vf}}. \quad (7)$$

The branches Z_{vi} and Z_{vf} are quantitatively designed in the next section.

2) *Isolated Transmission Path:* The optocoupler-based feedback signal path from Δv_e ($\triangleq \Delta v_0 - \Delta v_k$) to the current command Δv_c ($\triangleq \Delta \hat{i}_p^*$) consists of the following blocks.

a) *Error voltage to input LED current transfer block* H_{vi} :

$$H_{vi} \triangleq \frac{\Delta i_F}{\Delta v_e} = \frac{1}{R_F}. \quad (8)$$

b) *Current transfer ratio of LED* H_{ct} :

$$H_{ct} \triangleq \frac{\Delta i_E}{\Delta i_F}. \quad (9)$$

c) *Optocoupler output current to voltage transfer impedance* Z_E :

$$Z_E \triangleq \frac{\Delta v_E}{\Delta i_E} = R_E // \frac{1}{C_E s} \triangleq \frac{R_E}{\mu_E s + 1}, \quad \mu_E = R_E C_E. \quad (10)$$

The low-pass filter formed by R_E and C_E is employed here to reduce the high-frequency noise. Generally, the time constant $\mu_E = R_E C_E$ is so small compared with the main dynamic response speed of the whole converter system that it can be regarded as purely resistive in the dynamic modeling process.

d) *Current command compensator* G_{if} :

$$G_{if} \triangleq \frac{\Delta v_c}{\Delta v_E} = \frac{\Delta \hat{i}_p^*}{\Delta v_E} = \frac{-Z_{if}}{Z_{ii}} \triangleq \frac{-k_i}{\mu_i s + 1} \quad (11)$$

with

$$k_i = \frac{R_{if}}{R_{ii}}, \quad \mu_i = R_{if} C_{if} \quad (12)$$

where the pole ($-1/\mu_i$) of G_{if} is chosen to cancel the zero of the output filter network, and its gain k_i is properly set to obtain suitable dc loop gain.

3) *Current-Mode Controlled Flyback Converter*:

a) *Current-mode control scheme*: From the relationship $v_c = 3k_s \hat{i}_p + 1.4$ of the current control scheme designed previously, the small-signal relationship is found to be

$$\frac{\Delta \hat{i}_p}{\Delta v_c} = \frac{1}{3k_s}. \quad (13)$$

Hence the flyback converter dynamic model has been much simplified by eliminating the dynamic effect of the transformer magnetizing inductance.

b) *Flyback converter*: Assuming that Z_0 denotes the output impedance of the output filter network and \bar{i}_s is the average secondary current of the isolating transformer, the output voltage variation Δv_0 is related to $\Delta \bar{i}_s$ by

$$\Delta v_0 = \Delta \bar{i}_s Z_0. \quad (14)$$

And the transfer characteristic between $\Delta \bar{i}_s$ and $\Delta \hat{i}_p$ is derived as follows.

i) *Discontinuous mode*: According to the key waveforms sketched in Fig. 3(a), the relationship between the peak primary current and the average secondary current is obtained from energy transfer conservation:

$$\frac{1}{2} L_m \hat{i}_p^2 = v_0 \bar{i}_s T \quad (15)$$

where L_m is the magnetizing inductance of transformer and T denotes the switching period. Applying the well-known perturbation and linearization techniques, one can find

$$k_{\text{fly}} \triangleq \frac{\Delta \bar{i}_s}{\Delta \hat{i}_p} = \frac{D V_d}{2 V_0} \quad (16)$$

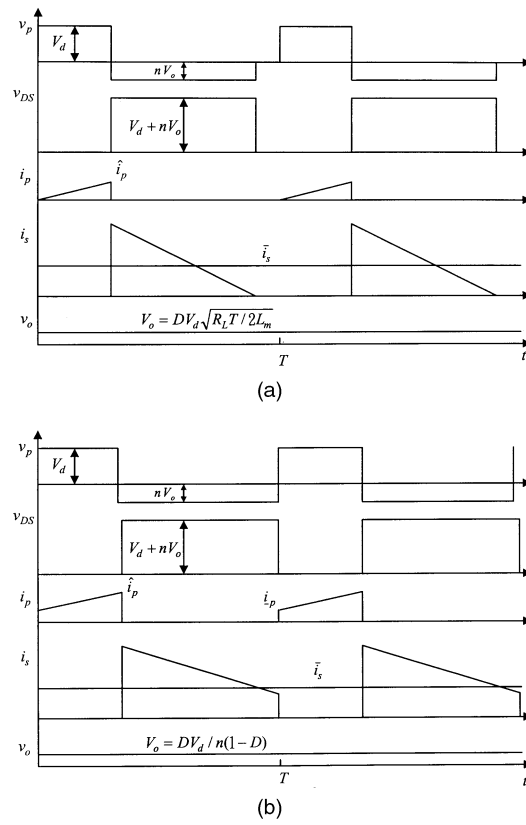


Fig. 3. Some key waveforms of flyback converter. (a) Discontinuous mode. (b) Continuous mode.

where V_d and V_0 are the input and output dc voltages, and the steady-state duty D is found from [12]

$$D = \frac{V_0}{V_d} \sqrt{\frac{2 L_m}{R_L T}}. \quad (17)$$

ii) *Continuous mode*: The waveforms in Fig. 3(b) show that the input and output energies are related by

$$\frac{1}{2} L_m (\hat{i}_p^2 - \hat{i}_p'^2) = v_0 \bar{i}_s T. \quad (18)$$

Similarly, one can find the same small-signal model as that listed in (16) but with

$$D = \frac{n V_0}{V_d + n V_0}. \quad (19)$$

The boundary of these two mode occurs at the following load resistance:

$$R_{L,CL} = \frac{2 L_m}{T} \left(\frac{V_0}{D V_d} \right)^2. \quad (20)$$

4) *Output Filter Network*: The impedance functions of the $LC - \pi$ filter can be directly written from the circuit shown in Fig. 1 as

$$Z_{01} = \frac{R_{c1,e} C_1 s + 1}{C_1 s} \quad (21)$$

$$Z_{02} = L s + R_{L,e} \quad (22)$$

$$Z_{03} = \frac{R_L (R_{c2,e} C_2 s + 1)}{(R_L + R_{c2,e}) C_2 s + 1}. \quad (23)$$

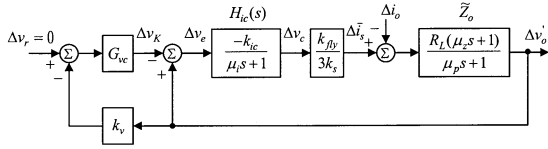


Fig. 4. Simplified control system block diagram of proposed flyback converter.

B. Simplified Configuration

Through properly selecting the block components and considering the time-scale properties of the block transfer functions, a much simplified block diagram can be built up. This will significantly facilitate the design of the voltage controller. In making the simplification, the following assumptions are made.

1) The two filter capacitances are chosen to be identical, i.e., $C_1 = C_2 \triangleq C$ and $R_{C1,e} = R_{C2,e} \triangleq R_{C,e}$.
2) Generally, the time constant μ_E is very small compared with the voltage dynamic response time, so it is negligible. 3) The series inductance L and thus its series equivalent resistance $R_{L,e}$ are very small. The governed equation of the output section of Fig. 2 can be written as

$$\Delta v_o' = \frac{Z_{01}Z_{03}}{Z_{01} + Z_{02} + Z_{03}} \Delta \bar{i}_s - \frac{(Z_{01} + Z_{02})Z_{03}}{Z_{01} + Z_{02} + Z_{03}} \Delta i_0$$

$$\triangleq \frac{Z_{01}Z_{03}}{Z_{01} + Z_{02} + Z_{03}} \Delta \bar{i}_s - Z_0 \Delta i_0 \quad (24)$$

where Z_0 denotes the output impedance of the current-mode controlled flyback converter and Δi_0 is the load current change. Based on the above assumptions, the expression of (24) can be simplified to be

$$\Delta v_o' \approx \frac{Z_{01}Z_{03}}{Z_{01} + Z_{03}} (\Delta \bar{i}_s - \Delta i_0) \triangleq \tilde{Z}_0 (\Delta \bar{i}_s - \Delta i_0) \quad (25)$$

with

$$\tilde{Z}_0 \approx \frac{R_L(\mu_z s + 1)}{(\mu_p s + 1)} \quad (26)$$

where $\mu_z = R_{C,e}C$, $\mu_p = 2R_LC$ under the assumption that $R_L \gg (R_{C,e}/2)$. Accordingly, the block diagram of Fig. 2 can then be approximately represented by that shown in Fig. 4.

1) *Observation:* Owing to the very small values of L and its series equivalent resistance $R_{L,e}$, the frequency response of Z_0 is approximated very well by \tilde{Z}_0 within the main dynamic frequency range. The effect of modeling steady-state error between Z_0 and \tilde{Z}_0 will be automatically compensated by the voltage feedback controller.

As that mentioned previously, the dynamic behavior of Z_E generally can be neglected owing to its very small value of time constant. As a result, the blocks from Δv_e to Δv_c can be combined and

expressed as:

$$H_{ic}(s) \triangleq \frac{\Delta v_c}{\Delta v_e} \approx \frac{-k_{ic}}{\mu_i s + 1} = \frac{-k_{ic}}{\mu_z s + 1}, \quad (27)$$

$$k_{ic} = H_{ct} R_E k_i / R_F$$

where $\mu_i = \mu_z$ is set for pole-zero cancellation.

C. Transfer Function Parameter Determination

1) *Physical Approach:* Within the specifications defined in Section III, a typical operating point having the following quantities is chosen:

$$V_d = 156 \text{ Vdc}, \quad V_0 = 16 \text{ Vdc}, \quad R_L = 10.7 \, \Omega,$$

$$D = 0.33 \quad (\text{continuous mode}). \quad (28)$$

Using the parameters listed in (28) and those already given previously, one can derive the following parameters of various blocks from the related equations:

$$n = 70/16, \quad H_{vi} = 1/R_F = 1/320 \, \Omega, \quad k_v = 1/6.4 \quad (29)$$

$$k_{\text{fly}} = \frac{\Delta \bar{i}_s}{\Delta \hat{i}_p} = \frac{DV_d}{2V_0} = 1.6 \quad (\text{continuous mode}) \quad (30)$$

and from (10) and (24)–(28),

$$Z_E = 470 / (4.7 \times 10^{-6} s + 1) \quad (31)$$

$$Z_{01} = \frac{5 \times 10^{-5} s + 1}{10^{-3} s},$$

$$Z_{02} = 2 \times 10^{-6} s + 5 \times 10^{-3}, \quad (32)$$

$$Z_{03} = \frac{10.7(5 \times 10^{-5} s + 1)}{1.05 \times 10^{-3} s + 1}$$

$$\tilde{Z}_0 = \frac{10.7(5 \times 10^{-5} s + 1)}{2.14 \times 10^{-2} s + 1}. \quad (33)$$

It follows from (11), (12), and (33) that G_{if} is set to be

$$G_{if} = \frac{-3.3}{5 \times 10^{-5} s + 1} \quad (34)$$

with

$$R_{ii} = 3.3 \, \text{k}\Omega, \quad R_{if} = 10 \, \text{k}\Omega, \quad C_{if} = 5 \, \text{nF}. \quad (35)$$

Until now, the only block transfer functions yet to be determined are H_{ct} and k_s . Although the former can be found from the data sheet offered by the vender ($H_{ct} = 1 \sim 3$), its accurate value is difficult to obtain, since it is quite nonlinear and variant due to the operating condition and temperature changes. As to the conversion factor k_s of the filtered current sensing circuit, its accurate value is not easy to be identified directly from the circuit configuration. In addition, the accurate transfer factor k_{fly} of the power stage is also usually rather difficult to obtain by the derivation

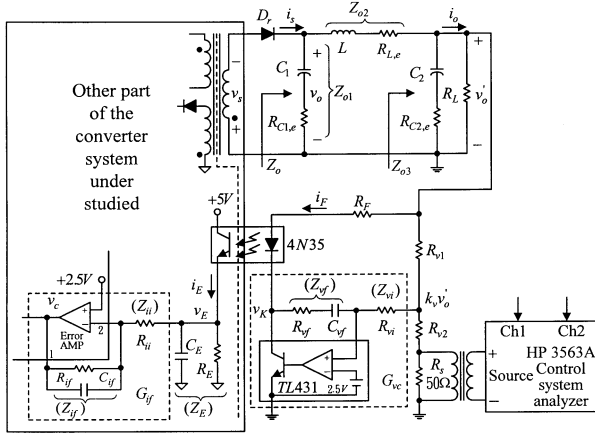


Fig. 5. Test circuit configuration for performing frequency response measurement.

described above. As a result, the estimation approach is used as an alternative to find these parameters.

2) *Estimation Approach*: For making the parameter estimation on-line, a test circuit is arranged as shown in Fig. 5. The voltage feedback controller G_{vc} is set to be integral type with $R_{vf} = 0$, $C_{vf} = 100$ nF and $R_{vi} = 10$ k Ω to let the whole converter system be normally operated at the chosen operating point. A swept-sine test signal with frequency from 30 Hz to 30 kHz generated from the control system analyzer is injected into the system with transformer isolation. The sensed two circuit variables are inputted to the analyzer and the generated frequency responses can be employed to perform the parameter estimation. The key parameters estimated in this stage are briefly described as follows:

i) The factor k_s is estimated directly from the current waveform of \hat{i}_p and its command to be $k_s = 0.45$.

ii) The voltages across $R_F (= \Delta v'_0 - \Delta v_k)$ and $R_E (= \Delta v_E)$ are sensed and inputted to the channels 1 and 2 (Ch1 and Ch2) of analyzer. The frequency responses of the transfer function from $(\Delta v'_0 - \Delta v_k)$ to Δv_E are plotted in Fig. 6(a). The magnitude response is rather constant within the main dynamic frequency range (≤ 1 kHz). Since the loading effect over this frequency range is very small, the current transfer ratio of optocoupler can be accurately estimated by

$$H_{ct} = \frac{\Delta v_E / R_E}{(\Delta v'_0 - \Delta v_k) / R_F} = 2.0. \quad (36)$$

iii) From the block diagram of Fig. 4, one can observe that the transfer factor k_{fly} of the flyback converter can be estimated to be

$$k_{fly} = 3k_s \frac{|\Delta v_0 / \Delta v_c|}{|\tilde{Z}_0|}. \quad (37)$$

Similarly, the voltages of Δv_c (see Fig. 1) and Δv_0 are sensed and inputted to the channels 1 and 2 of analyzer. Fig. 6(b) shows the measured frequency

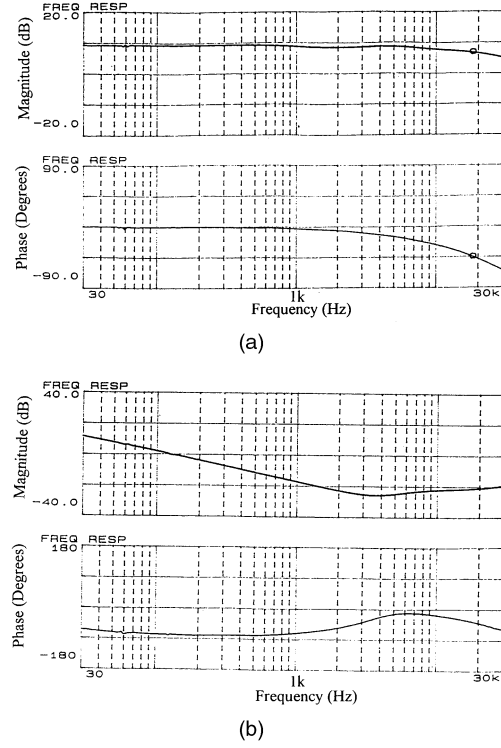


Fig. 6. Frequency responses of transfer functions. (a) $(\Delta v'_0 - \Delta v_k)$ to Δv_E . (b) Δv_c to Δv_0 .

responses of the transfer function from Δv_c to Δv_0 . The frequency response of \tilde{Z}_0 at nominal load case can be accurately calculated off-line. The estimates of (37) over the frequency range $30 \text{ Hz} < f < 1000 \text{ Hz}$ are slightly varied. An average of the estimates at six frequencies (30 Hz, 60 Hz, 120 Hz, ..., 960 Hz) is found to be $k_{fly} = 2.1$.

IV. QUANTITATIVE DESIGN OF VOLTAGE CONTROLLER

Having estimated the transfer functions of all blocks in Fig. 2 and made the model simplification for Z_0 , all the blocks in the simplified block diagram of Fig. 4 have been known at the chosen operating point. The transfer function from Δi_0 to $\Delta v'_0$ can be derived from Fig. 4 as

$$\begin{aligned} H_d(s) &\triangleq \frac{\Delta v'_0}{\Delta i_0} \bigg|_{\Delta v_r=0} = \frac{-\tilde{Z}_0}{1 - (1 + k_v G_{vc}) k_{fly} \tilde{Z}_0 H_{ic}(s) / 3k_s} \\ &= \frac{-sR_L(\mu_z s + 1)}{\mu_p s^2 + [1 + (1 + k_v K_P) R_L k_{fly} k_{ic} / 3k_s] s + K_I k_v R_L k_{fly} k_{ic} / 3k_s} \\ &= \frac{s(cs + d)}{s^2 + as + b} = \frac{h_1 s}{s + \mu_1} + \frac{h_2 s}{s + \mu_2} \end{aligned} \quad (38)$$

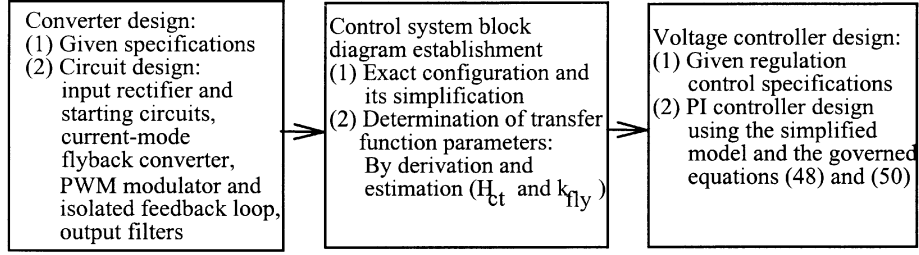
where

$$a = [1 + (1 + k_v K_P) k_{ic} k_{fly} R_L / 3k_s] / \mu_p \quad (39)$$

$$b = k_v K_I k_{ic} k_{fly} R_L / 3k_s \mu_p \quad (40)$$

$$c = -R_L \mu_z / \mu_p \quad (41)$$

TABLE I



$$d = -R_L / \mu_p \quad (42)$$

$$h_1 = \frac{-d + c\mu_1}{\mu_1 - \mu_2} \quad (43)$$

$$h_2 = \frac{d - c\mu_2}{\mu_1 - \mu_2} \quad (44)$$

$$\mu_1 + \mu_2 = a \quad (45)$$

$$\mu_1 \mu_2 = b. \quad (46)$$

The voltage response due to unit-step load current change can be derived from (38) to (46):

$$\Delta v'_0(t) = \frac{1}{\mu_1 - \mu_2} [(-d + c\mu_1)e^{-\mu_1 t} + (d - c\mu_2)e^{-\mu_2 t}]. \quad (47)$$

The general requirements of unit-step load regulation response can be specified as: 1) maximum dip $= \Delta v_{dm}$; 2) restore time $= t_{re}$, which is defined as the time at which the response $\Delta v'_0(t)$ restores to 5% of Δv_{dm} ; 3) overshoot $= 0$; and 4) steady-state error $= 0$. Some governed equations related to these key specifications are derived as followed. The maximum voltage dip Δv_{dm} and the time t_{dm} at which it occurred can be derived from (47) to be

$$\Delta v_{dm} = \frac{1}{\mu_1 - \mu_2} \left[(-d + c\mu_1) \left(\frac{\mu_1(-d + c\mu_1)}{\mu_2(-d + c\mu_2)} \right)^{-\mu_1/\mu_1 - \mu_2} + (d - c\mu_2) \left(\frac{\mu_1(-d + c\mu_1)}{\mu_2(-d + c\mu_2)} \right)^{-\mu_2/\mu_1 - \mu_2} \right] \quad (48)$$

and

$$t_{dm} = \frac{1}{\mu_1 - \mu_2} \ln \left(\frac{\mu_1(-d + c\mu_1)}{\mu_2(-d + c\mu_2)} \right). \quad (49)$$

According to the above definition, the relationship between the restore time t_{re} and the maximum dip Δv_{dm} can be found from (47) and (48) as

$$\begin{aligned} \Delta v'_0(t_{re}) &= \frac{\Delta v_{dm}}{20} \\ &= \frac{1}{\mu_1 - \mu_2} [(-d + c\mu_1)e^{-\mu_1 t_{re}} + (d - c\mu_2)e^{-\mu_2 t_{re}}]. \end{aligned} \quad (50)$$

Obviously, if the controller can be properly designed to let the closed-loop poles be all negative real, then the overshoot will not exist. In addition,

the steady-state error is also zero for the PI-controlled system. It follows that by specifying the desired Δv_{dm} and t_{re} , the negative real poles $-\mu_1$ and $-\mu_2$ can be solved from (48) and (50). And the parameters of the PI controller can be found from (39)–(46).

1) *Design Example:* Suppose that the desired output voltage regulation response characteristics due to step load current change of $\Delta i_0 = 1$ A at nominal load $R_L = 10.7 \Omega$ are

$$t_{re} = 4 \text{ ms}, \quad \Delta v_{dm} = -50 \text{ mV}. \quad (51)$$

Following the procedure described above, the parameters of the controller are found to be

$$K_p = 0.7, \quad K_I = 5300. \quad (52)$$

And the realized circuit components can be found from (7):

$$R_{vi} = 3.3 \text{ k}\Omega, \quad R_{vf} = 2.3 \text{ k}\Omega, \quad C_{vf} = 57 \text{ nF}. \quad (53)$$

The unit-step response of $\Delta v'_0$ simulated using the simplified model of Fig. 4 by Matlab is shown in Fig. 7(a); it indicates that the prescribed specifications listed in (51) are completely satisfied. The simulated $\Delta v'_0$ using the accurate model of Fig. 2 and the same designed controller is also plotted in Fig. 7(b). The comparison between the results of Figs. 7(a) and 7(b) shows that they are very close. This confirms the validity of the proposed simplified model.

2) *Summary of Design Procedure:* For wholly understanding the design of the proposed converter, the design procedure described in Sections II to IV is briefly summarized in Table I.

V. SIMULATION AND EXPERIMENTAL RESULTS

For confirming the effectiveness of the developed dynamic model, the dynamic response by Pspice simulation is further made. Fig. 8(a) plotted the simulated waveform of $\Delta v'_0$ due to the step load change $i_0 = 1.5 \text{ A} \leftrightarrow 2.5 \text{ A}$ ($R_L = 10.7 \Omega \leftrightarrow 6.4 \Omega$) at nominal load ($R_L = 10.7 \Omega$). The result shows that it is very close to the simulated result shown in Fig. 7(b). As a result, the dynamic behavior of the converter can be accurately represented by the proposed control system block diagram with the

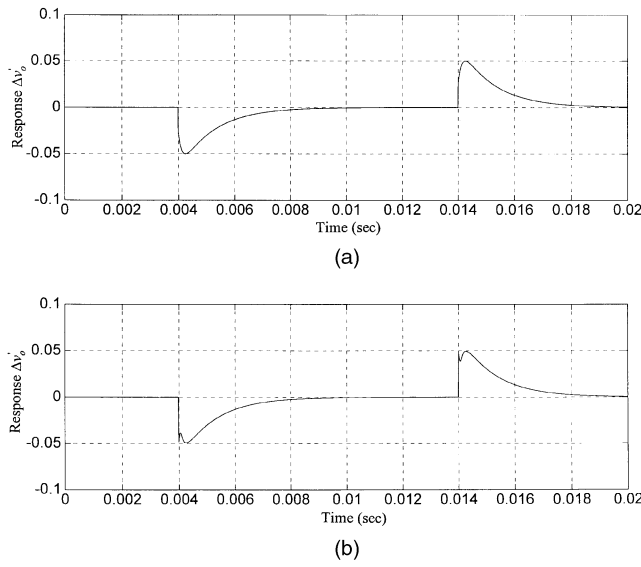


Fig. 7. Matlab simulated $\Delta v'_0$ due to unit-step load current change. (a) Using simplified model. (b) Using accurate model.

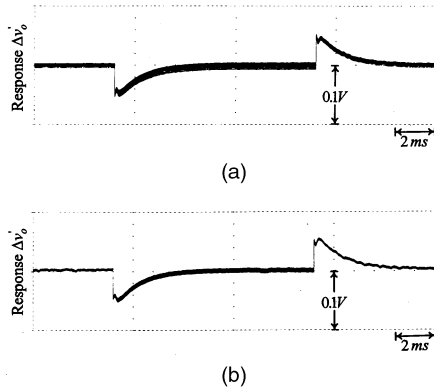


Fig. 8. Pspice simulated $\Delta v'_0$ due to step load change.
(a) $i_0 = 1 \text{ A} \leftrightarrow 2.5 \text{ A}$ ($R_L = 10.7 \Omega \leftrightarrow 6.4 \Omega$).
(b) $i_0 = 0.5 \text{ A} \leftrightarrow 1.5 \text{ A}$ ($R_L = 32 \Omega \leftrightarrow 10.7 \Omega$).

proposed estimated parameters. If the load is reduced to light load with $R_L = 32 \Omega$, the Pspice simulated unit-step load regulation response of $\Delta v'_0$ is shown in Fig. 8(b), the result indicates that very good response is also obtained by the designed controller.

Having confirmed the effectiveness of the proposed controller by simulations, hardware implementation of the designed PI controller is carried out. Some waveforms of key circuit variables are first observed. Figs. 9(a) and 9(b) plot the measured waveforms of v_s , v_{Rs} , v_{DS} and v_{GS} at two loads. For further observing the current-mode control behavior of the flyback converter, the measured waveforms of v_{Rs} and \tilde{v}_c ($\tilde{v}_c \triangleq (v_c - 1.4)/3$) at two loads are shown in Figs. 9(c) and 9(d). The correct operation of the designed converter can be seen from the results shown in Figs. 9(a)–9(d).

As to the voltage regulation responses, the measured output voltage $\Delta v'_0$ due to step load current change $\Delta i_0 = 1 \text{ A}$ at $R_L = 10.7 \Omega$ and 32Ω are shown

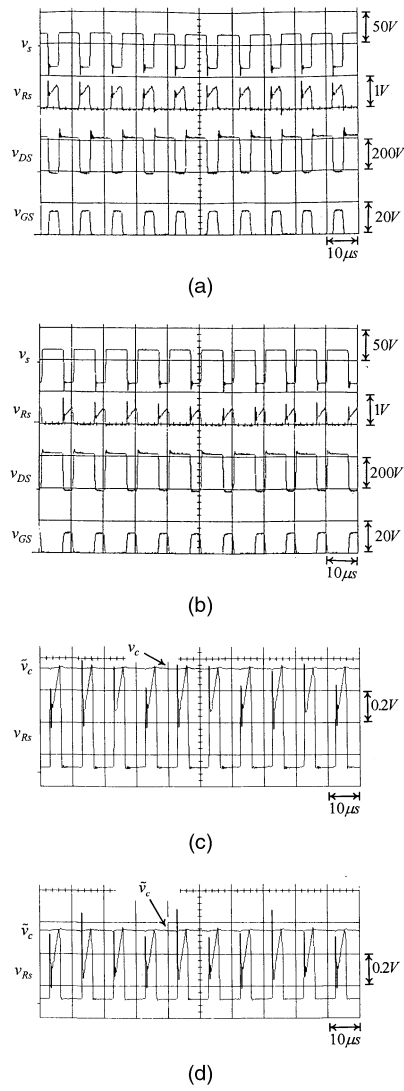


Fig. 9. Measured waveforms. (a) v_s , v_{Rs} , v_{DS} , v_{GS} at $R_L = 6.4 \Omega$.
(b) v_s , v_{Rs} , v_{DS} , v_{GS} at $R_L = 10.7 \Omega$. (c) v_{Rs} and \tilde{v}_c at $R_L = 6.4 \Omega$.
(d) v_{Rs} and \tilde{v}_c at $R_L = 10.7 \Omega$.

in Figs. 10(a) and 10(b). The results clearly show that they are very close to the simulation results shown in Fig. 7 and Fig. 8. So, the validity of the developed dynamic model and the designed controller is further confirmed.

VI. CONCLUSIONS

The dynamic modeling and quantitative controller design of an optocoupler isolated current-mode controlled flyback converter have been presented in this paper. First, the circuit elements of the converter are designed according to the given system specifications. The current-mode control has simplified the inner-loop dynamic behavior. Then the development of the detailed control system block diagram for correctly representing the dynamic behavior of the converter system is described. The estimation approach is applied to find the parameters

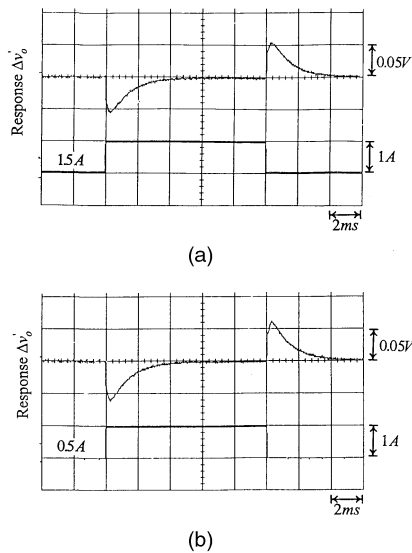
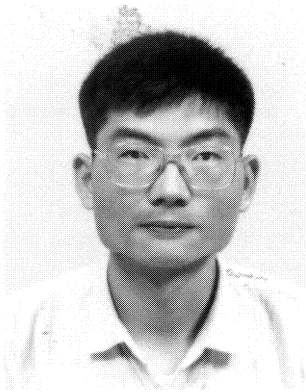


Fig. 10. Measured $\Delta v'_0$ due to step load change.
 (a) $i_0 = 1.5 \text{ A} \leftrightarrow 2.5 \text{ A}$ ($R_L = 10.7 \Omega \leftrightarrow 6.4 \Omega$).
 (b) $i_0 = 0.5 \text{ A} \leftrightarrow 1.5 \text{ A}$ ($R_L = 32 \Omega \leftrightarrow 10.7 \Omega$).

of some critical blocks, which is either nonlinear or difficult to be modeled accurately by derivation. Furthermore, in order to facilitate the quantitative design of the voltage controller, the compensation and model simplification are made. According to the simplified structure of control system block diagram, the governed equations corresponding to the key regulation control specifications are formulated, and the parameters of the PI voltage controller are found quantitatively and systematically. Some simulation results by Matlab and Pspice are provided to confirm the effectiveness of the proposed dynamic modeling and controller design techniques. Finally, the performance of the designed flyback converter is further demonstrated experimentally.

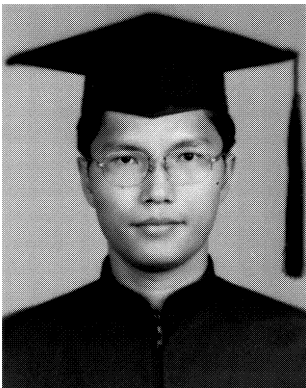
REFERENCES

- [1] Mohan, N., Undeland, T. M., and Robbins, W. P. (1995) *Power Electronics: Converters, Applications and Design*. New York: Wiley, 1995.
- [2] Czarkowski, D., and Kazimierczuk, M. K. (1992) Linear circuit models of PWM flyback and buck/boost converters. *IEEE Transactions on Circuits and System—I: Fundamental Theory and Applications*, **39**, 8 (Aug. 1992), 688–693.
- [3] Kazimierczuk, M. K., and Nquyen, S. T. (1995) Small-signal analysis of open-loop PWM flyback DC–DC converter for CCM. In *Proceedings of the IEEE 1995 National Aerospace and Electronics Conference*, 1995, 69–76.
- [4] Kazimierczuk, M. K., and Nquyen, S. T. (1995) Closed-loop voltage-mode-controlled PWM flyback DC–DC converter for CCM with integral-lead controller. In *Proceedings of the IEEE 1995 National Aerospace and Electronics Conference*, 1995, 61–68.
- [5] Ma, K. W., and Lee, Y. S. (1996) Integrated flyback converter for DC uninterruptible power supply. *IEEE Transaction on Power Electronics*, **11**, 2 (Mar. 1996), 318–327.
- [6] Mammano, B. (1990) Isolating the control loop. *Unitrode Power Supply Design Seminar SEM-700*, 1990, 2-1 to 2-15.
- [7] Middlebrook, R. D., and Cuk, S. (1976) A general unified approach to modelling switching-converter power stages. In *IEEE Power Electronics Specialists Conference Record*, 1976, 18–34.
- [8] Chetty, P. R. K. (1981) Current injected equivalent circuit approach (CIECA) to modeling of switching dc-dc converter in continuous inductor conduction mode. *IEEE Transactions on Aerospace and Electronic System*, **AES-17**, (Nov. 1981), 802–808.
- [9] Lee, Y. S. (1985) A systematic and unified approach to modeling switches in switch-mode power supplies. *IEEE Transactions on Industrial Electronics*, **IE-32**, 4 (Nov. 1985), 445–448.
- [10] Liaw, C. M., Chiang, S. J., Lai, C. Y., Pan, K. H., Leu, G. C., and Hsu, G. S. (1994) Modeling and controller design of a current-mode controlled converter. *IEEE Transactions on Industrial Electronics*, **41**, 2 (Apr. 1994), 231–240.
- [11] Chrysis, G. C. (1989) *High-Frequency Switching Power Supplies*. New York: McGraw-Hill, 1989.
- [12] Liaw, C. M. (1996) Research on integration of switch mode power supplies. Project Report of National Science Council, NSC 85-2622-E-007-011, Taiwan, ROC.



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