00A0 $\exists$ $\forall$ $\subseteq$ 2713x 27FA$\Longleftrightarrow$ $\surd$ $\sqrt[3]{}$ $\oplus$ $\otimes$

Ego1 Documentation

2.2

e-elements

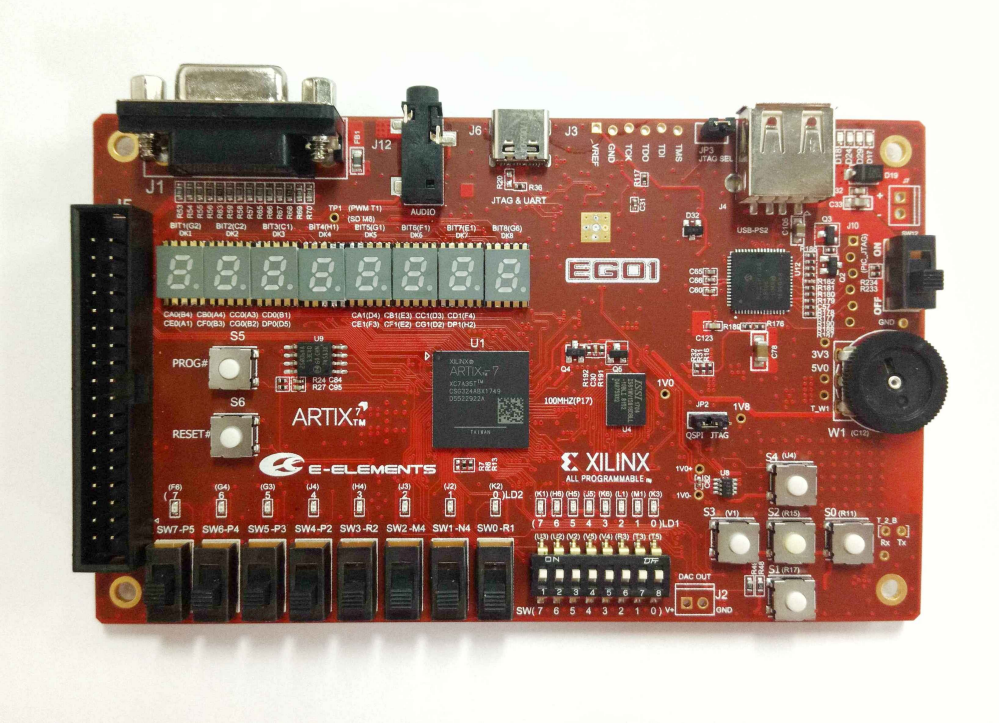
2020 07 22

Contents

CHAPTER 1

1.1

EGo1 Xilinx Artix-7 FPGA EGo1 FPGA (XC7A35T-1CSG324C) FPGA MicroBlaze



1	VGA	10	1
2		11	1 DAC
3	USB UART/JTAG	12	SRAM
4	USB PS2	13	SPI FLASH
5	2 4	14	
6	16 LED	15	
7	8		
8	1 8 DIP		
9	5		

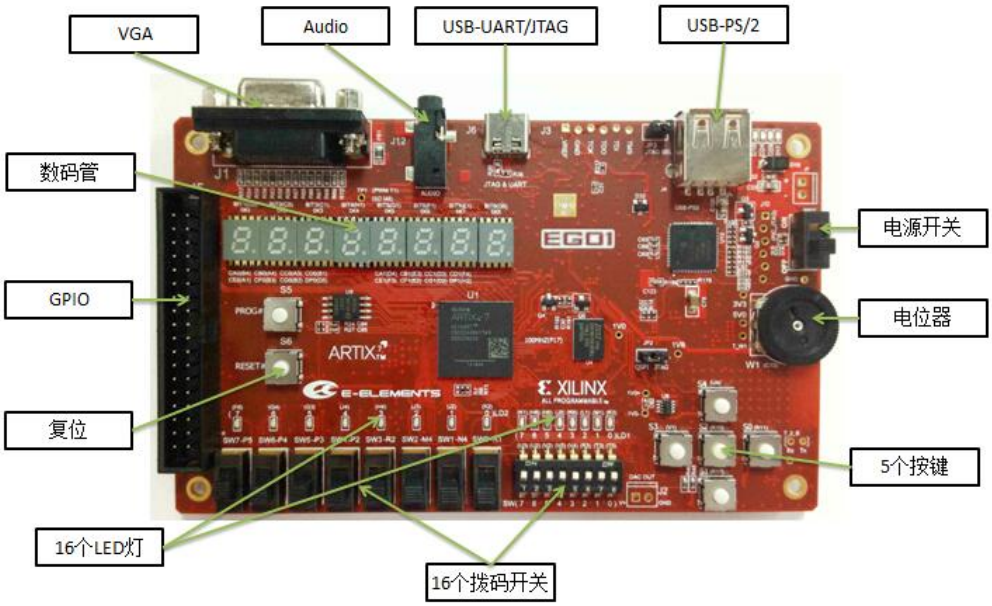
1.2 Getting start

1.2.1 1 EGo1

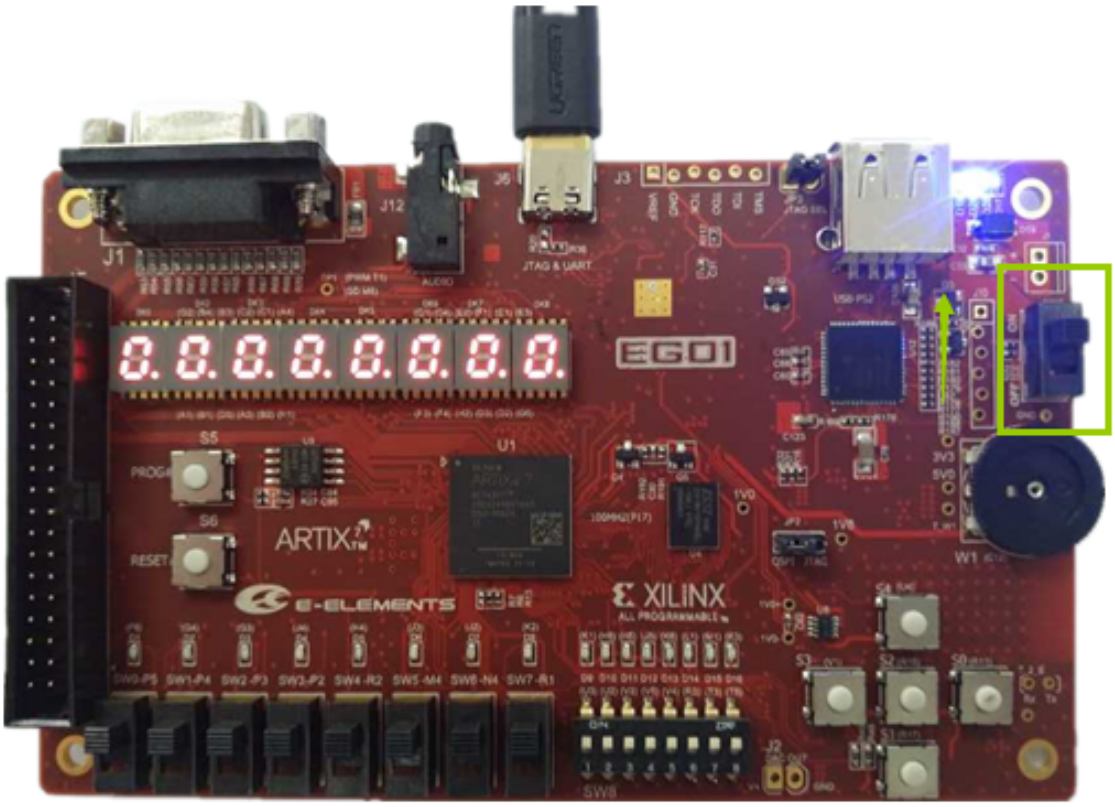
EGo1

EGo1 ( )

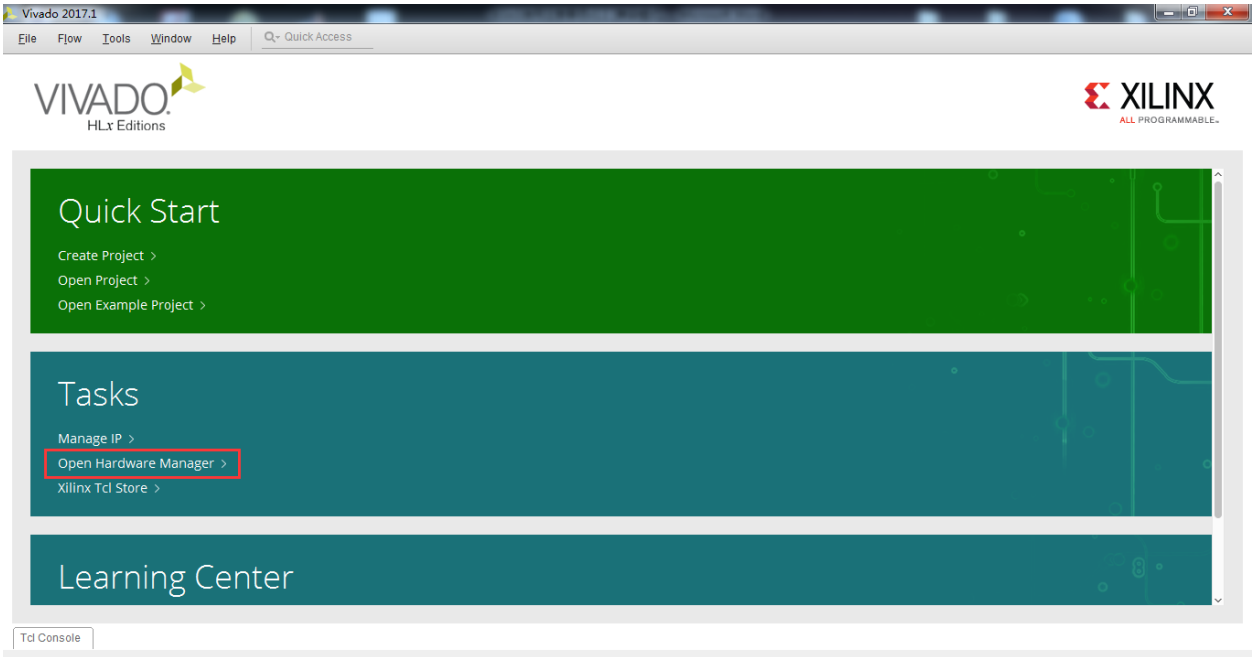
EGo1


VGA
Audio
USB-UART/JTAG
USB-PS/2
数码管
电源开关
GPIO
电位器
复位
5个按键
16个LED灯
16个拨码开关

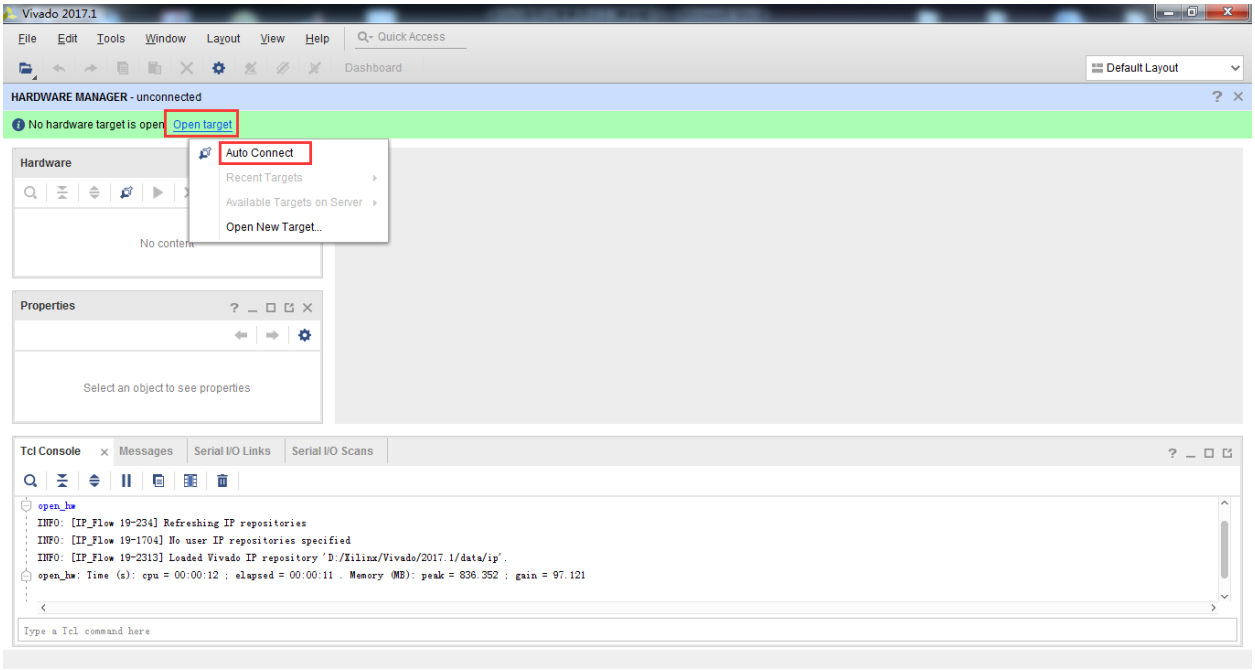
1 usb EGo1 USB-UART/JTAG Usb usb



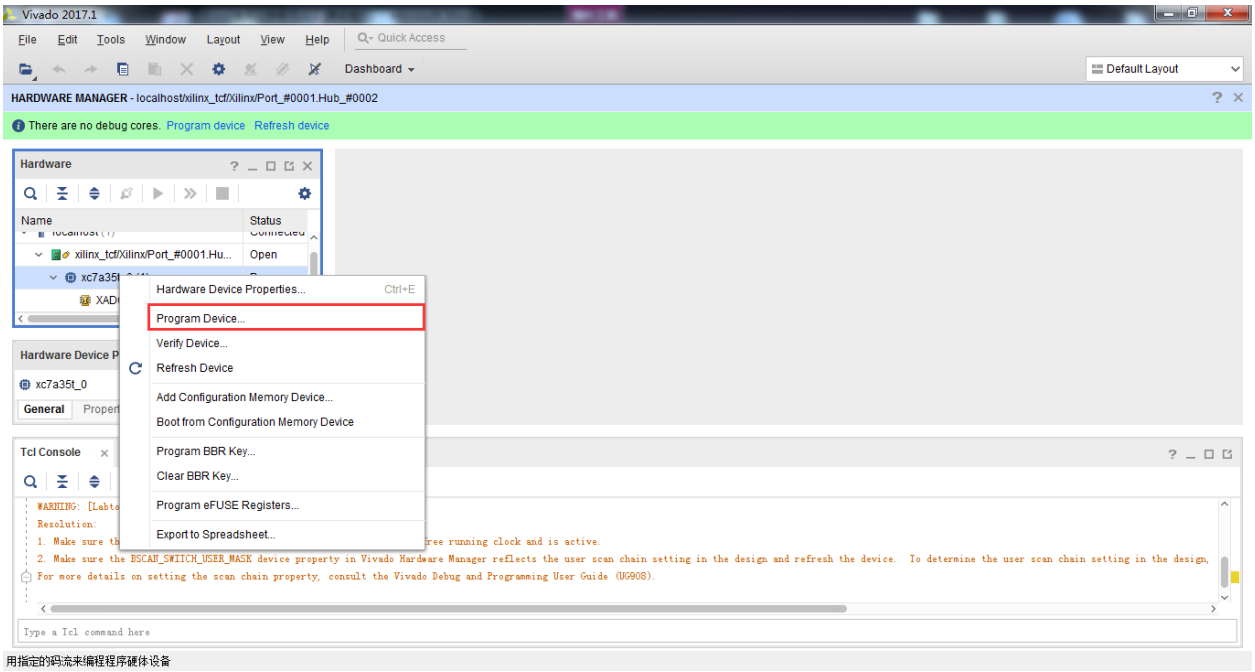
2 vivado Open Hardware Manager



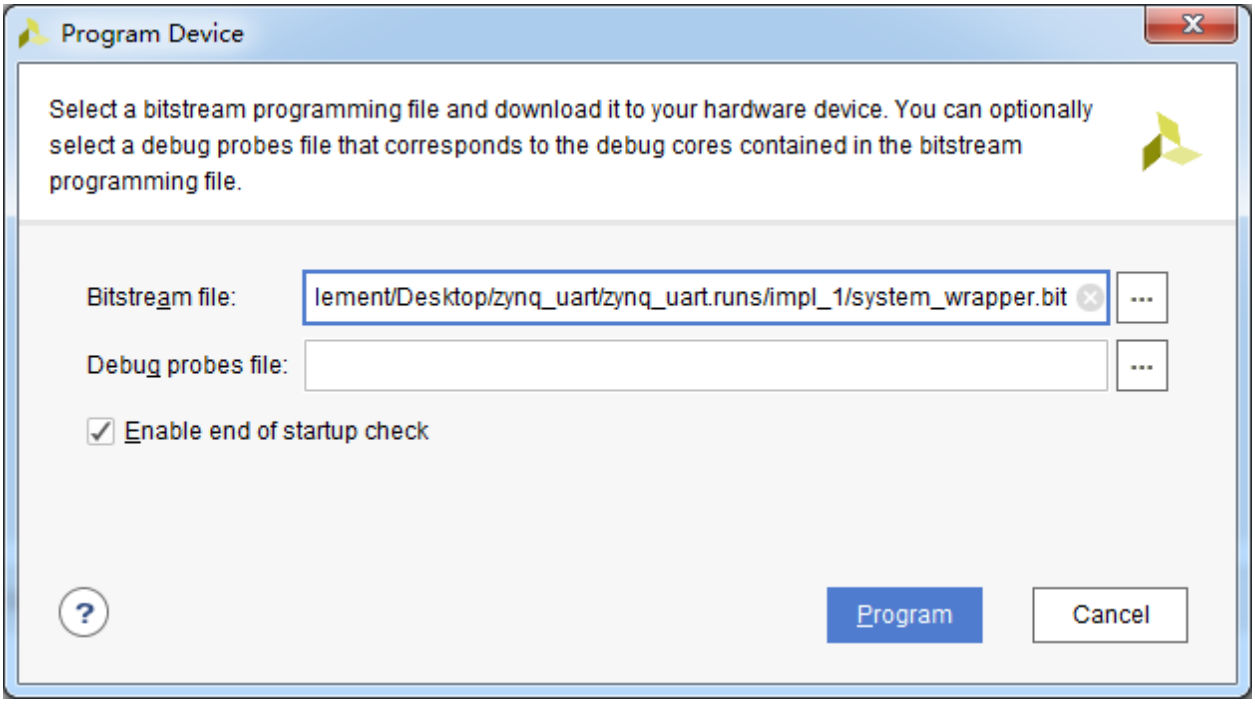
3 “Hardware Manager” “Open target”, “Auto Connect”



4 “Program Device”



5 “Bitstream File” bitstream “Program” FPGA



1.2.2 2 EGo1

- USB-Type C
- VGA USB
- 16 2*16
- PC Putty TeraTerm Vivado2015.4
- Android BLE

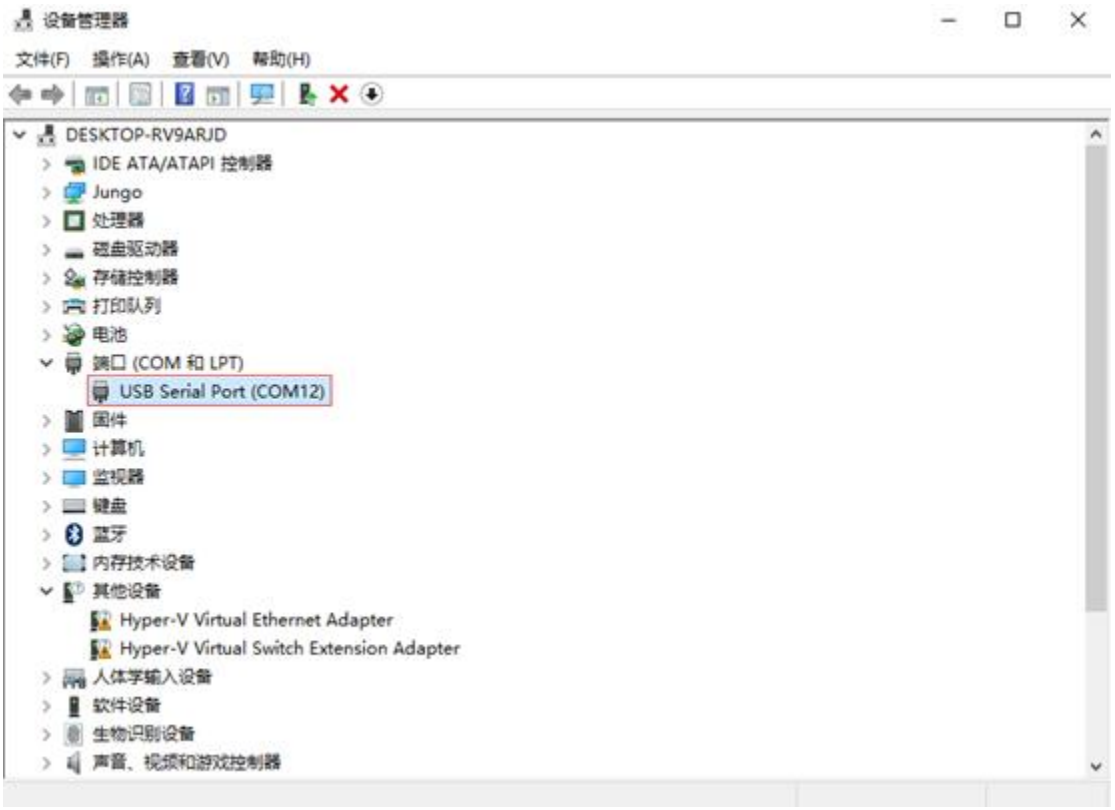
bin https://pan.baidu.com/s/1nWZ40Vq58ZvD7wrieJfgiQ l271

1.

a) OFF

b) USB PC

2. D18 D30 LED

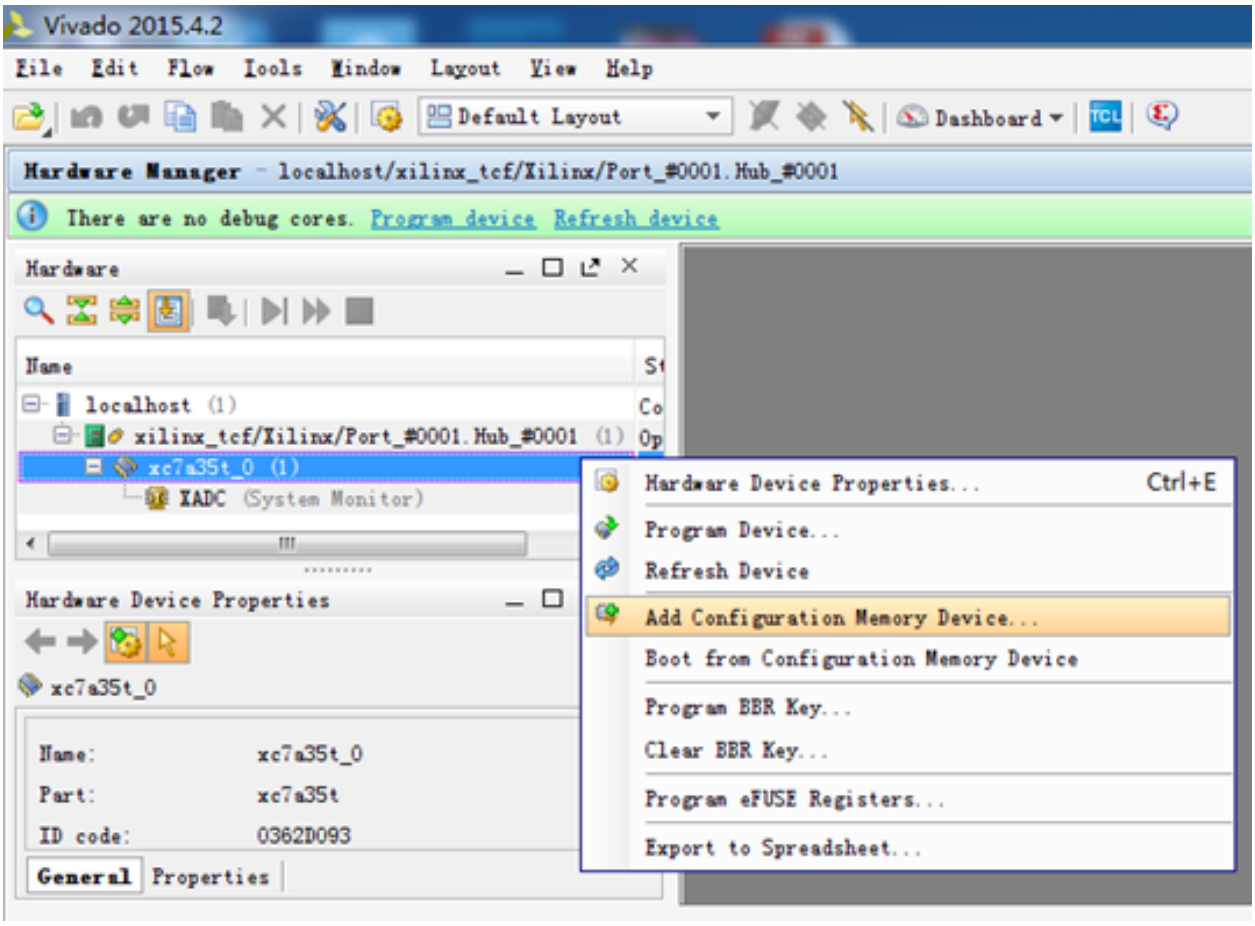


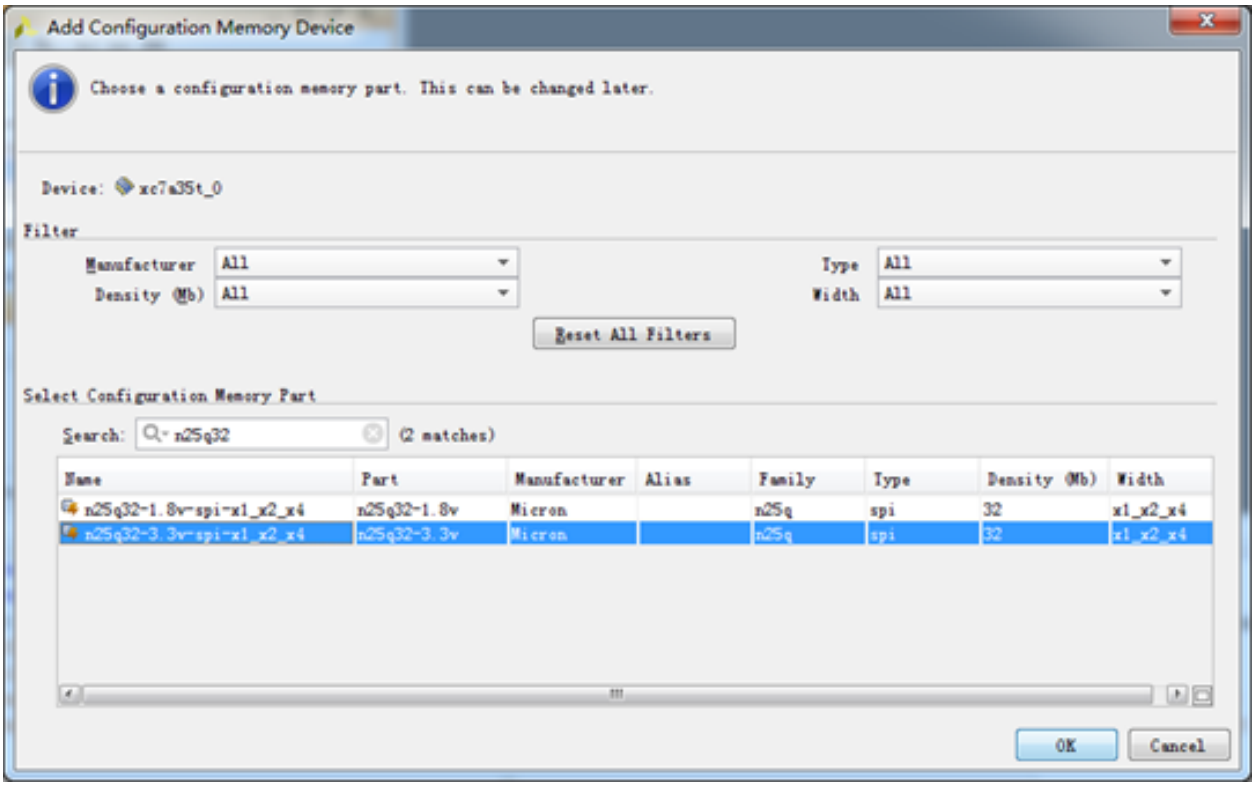
3. Flash EGO1

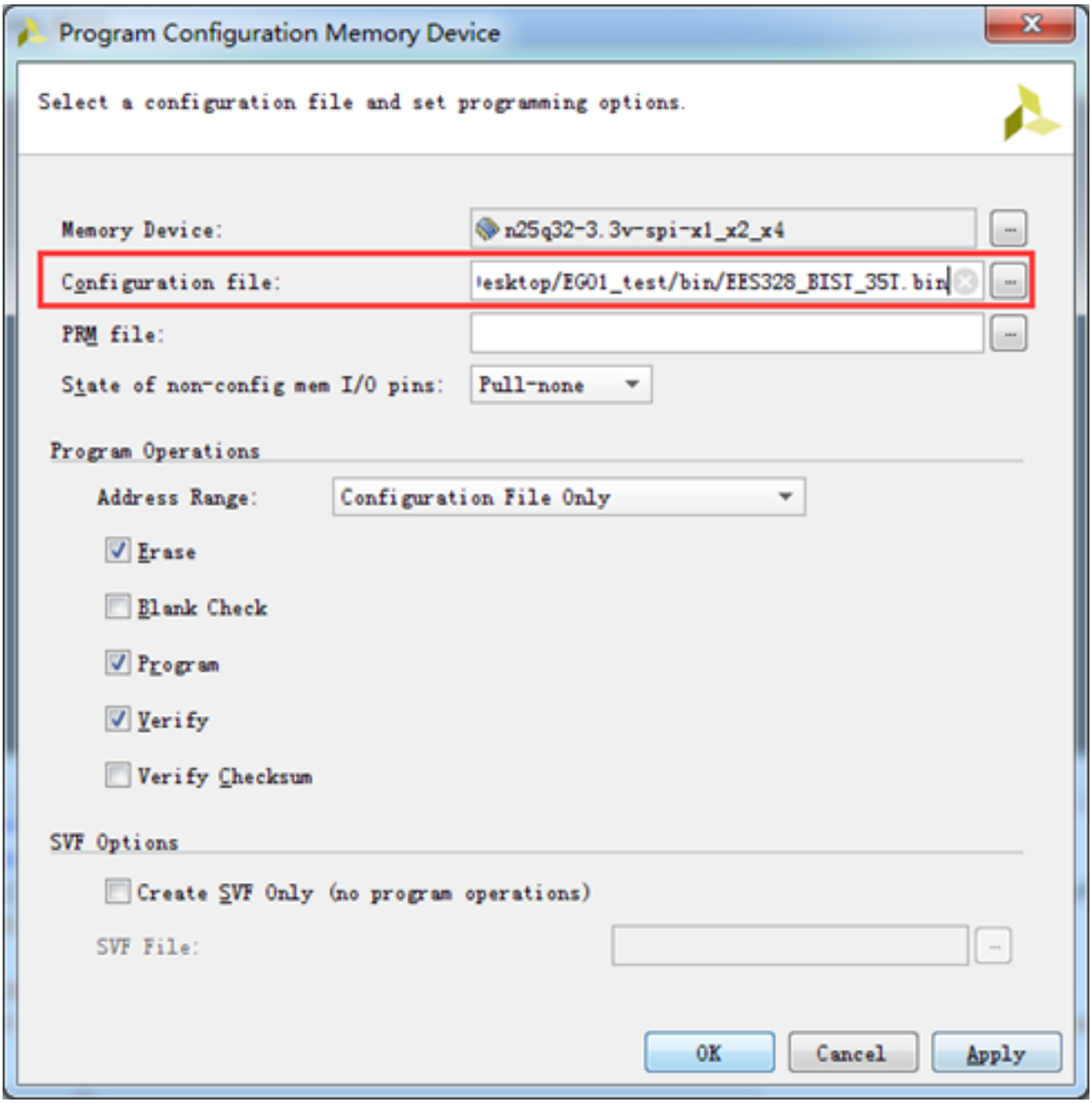
a) Vivado→Open Hardware Manager→Open Target→Auto Connect

b) Add Configuration Memory Device→ Flash N25Q64-3.3V→OK “OK”

c) “Program Configuration Memory Device” BIN Configuration File BIN ..EGO1_testbinEGO1_BIST_35T.bin “OK”

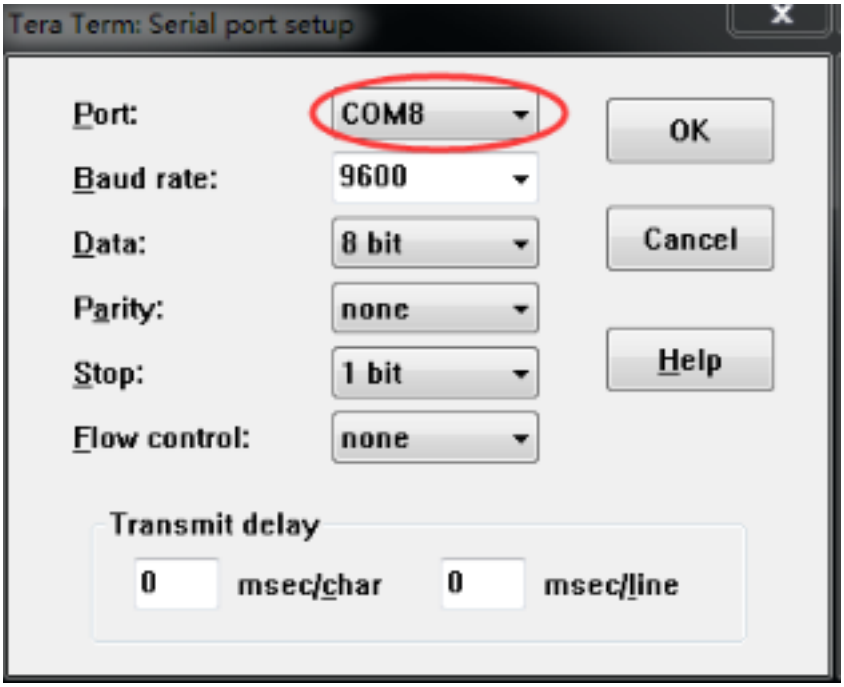

Vivado 2015.4.2
File Edit Flow Tools Window Layout View Help
Default Layout
Dashboard
Hardware Manager - localhost/xilinx_tcf/Xilinx/Port_#0001.Hub_#0001
There are no debug cores. Program device Refresh device
Hardware
Name
localhost (1)
xilinx_tcf/Xilinx/Port_#0001.Hub_#0001 (1)
xc7a35t_0 (1)
XADC (System Monitor)
Hardware Device Properties
xc7a35t_0
Name: xc7a35t_0
Part: xc7a35t
ID code: 0362D093
General Properties
Hardware Device Properties... Ctrl+E
Program Device...
Refresh Device
Add Configuration Memory Device...
Boot from Configuration Memory Device
Program BBR Key...
Clear BBR Key...
Program eFUSE Registers...
Export to Spreadsheet...


Add Configuration Memory Device
Choose a configuration memory part. This can be changed later.
Device: xc7a35t_0
Filter
Manufacturer All
Density (Mb) All
Type All
Width All
Reset All Filters
Select Configuration Memory Part
Search: n25q32
(2 matches)
Name Part Manufacturer Alias Family Type Density (Mb) Width
n25q32-1.8v-spi-x1_x2_x4 n25q32-1.8v Micron n25q spi 32 x1_x2_x4
n25q32-3.3v-spi-x1_x2_x4 n25q32-3.3v Micron n25q spi 32 x1_x2_x4
OK
Cancel

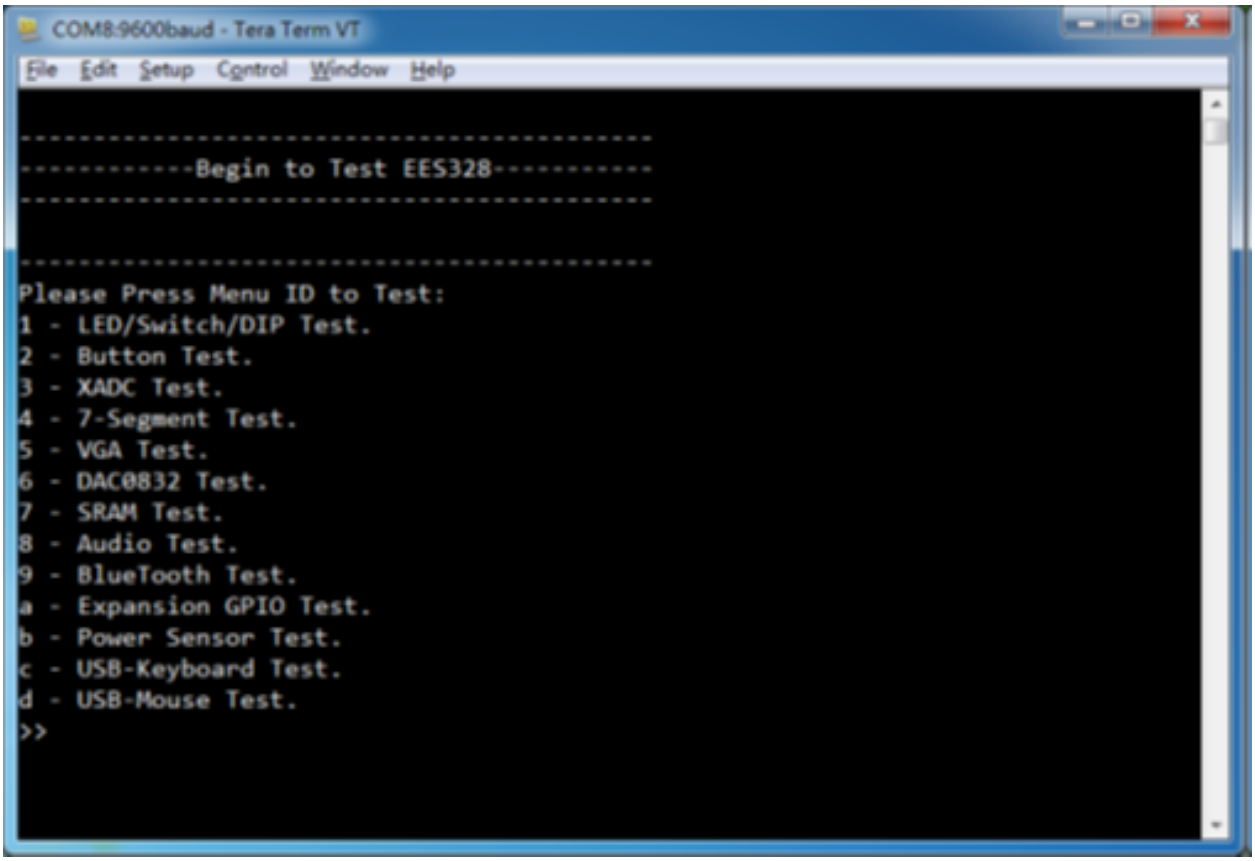


4. Flash a) JP2 QSPI b) LED D24

5. 9600 8-Bit 1-Bit



6. S5_PROG# FPGA ;



1.3 EGo1

1.3.1 1 FPGA

EGo1 Xilinx Artix-7 XC7A35T-1CSG324C FPGA

	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280
	Slices	2,000	2,600	3,650	5,200
	CLB Flip-Flops	16,000	20,800	29,200	41,600
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50
	Total Block RAM (Kb)	720	900	1,620	1,800
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5
I/O Resources	Maximum Single-Ended I/O	150	250	150	250
	Maximum Differential I/O Pairs	72	120	72	120
Embedded Hard IP Resources	DSP Slices	40	45	80	90
	PCIe® Gen2[1]	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	4	4	4
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L

1.3.2 2

EGo1 Type-C EGo1 Type-C UART JTAG Type-C 5V LED D18

1.3.3 3

EGo1 100MHz FPGA P17 FPGA MMCM

		FPGA IO PIN
	SYS_CLK	P17

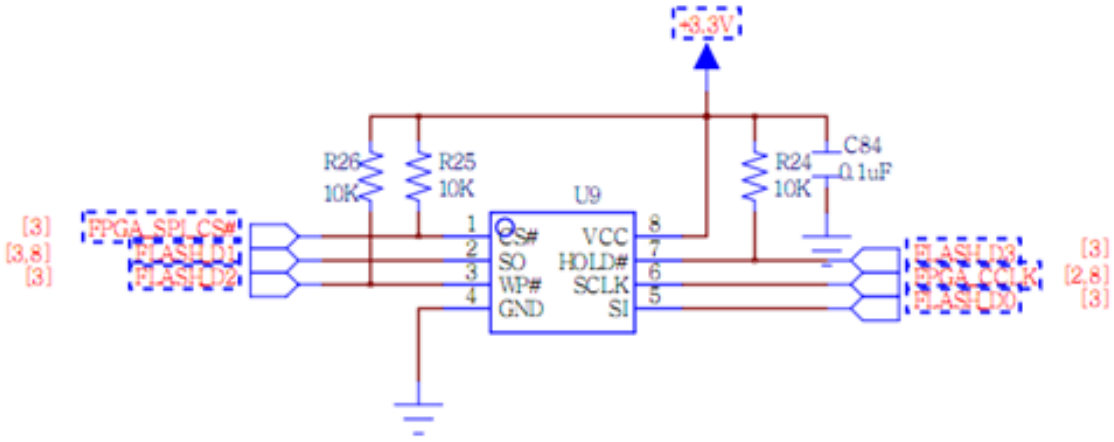
1.3.4 4 FPGA

EGo1 FPGA FPGA

- USB JTAG J6
- 6-pin JTAG J3
- SPI Flash

FPGA .bit bit FPGA Vivado BIT

SPI Flash FPGA Flash Xilinx Vivado Flash SPI Flash N25Q32 3.3V FPGA D24

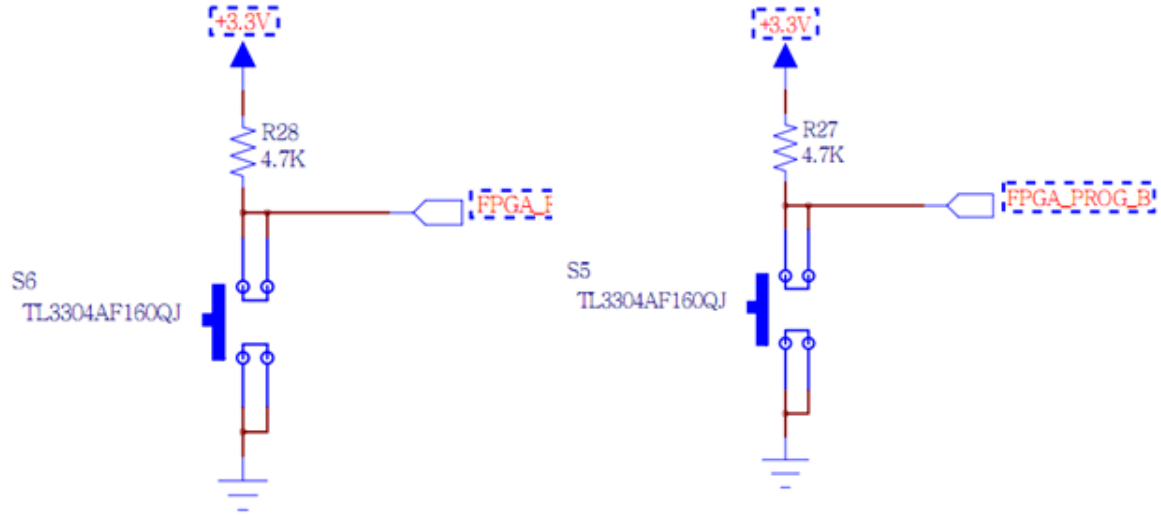


1.3.5 5 I/O

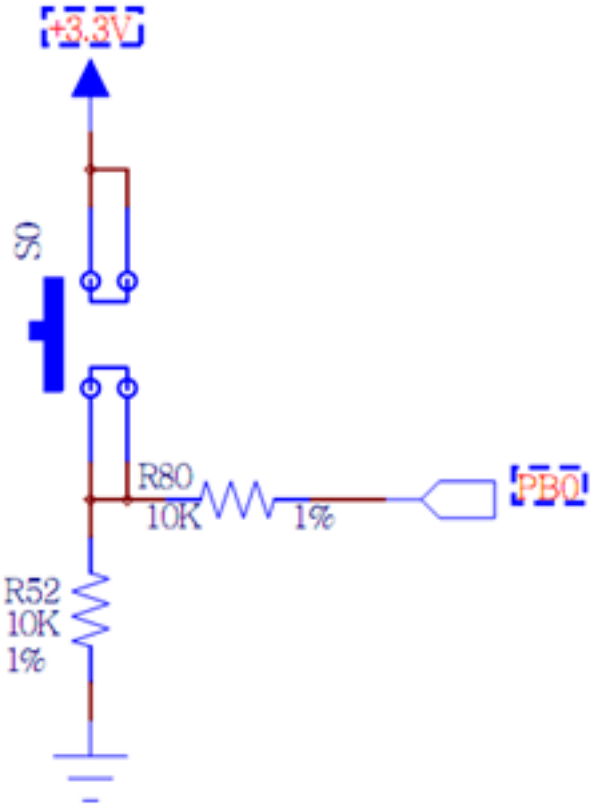
I/O 2 5 8 1 8 DIP 16 LED 8

5.1

RST S6 FPGA PROG S5 RST



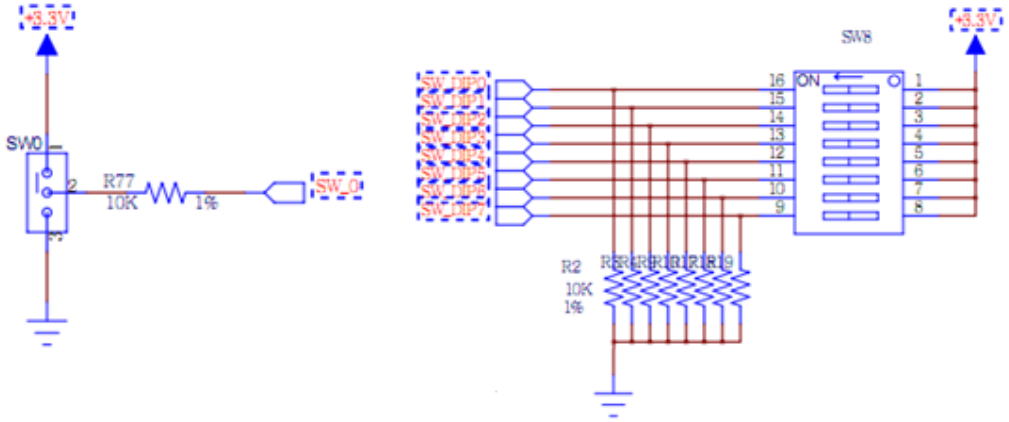
		FPGA IO PIN
	FPGA_RESET	P15



		FPGA IO PIN
S0	PB0	R11
S1	PB1	R17
S2	PB2	R15
S3	PB3	V1
S4	PB4	U4

5.2

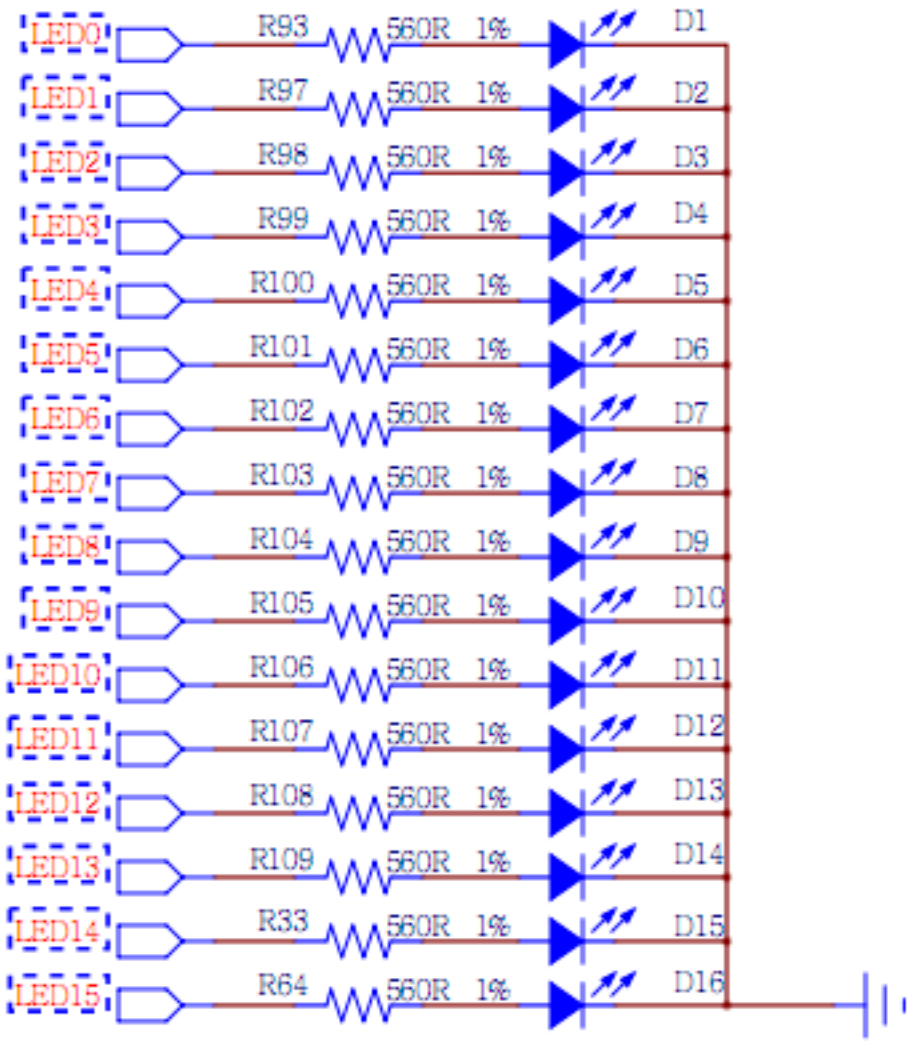
8 8 DIP



		FPGA IO PIN
SW0	SW_0	R1
SW1	SW_1	N4
SW2	SW_2	M4
SW3	SW_3	R2
SW4	SW_4	P2
SW5	SW_5	P3
SW6	SW_6	P4
SW7	SW_7	P5
SW8	SW_DIP0	T5
	SW_DIP1	T3
	SW_DIP2	R3
	SW_DIP3	V4
	SW_DIP4	V5
	SW_DIP5	V2
	SW_DIP6	U2
	SW_DIP7	U3

5.3 LED

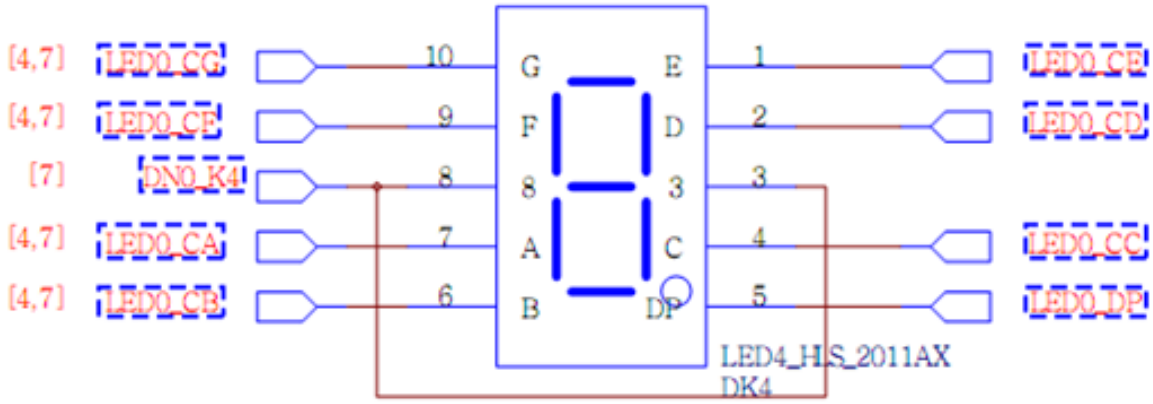
LED FPGA

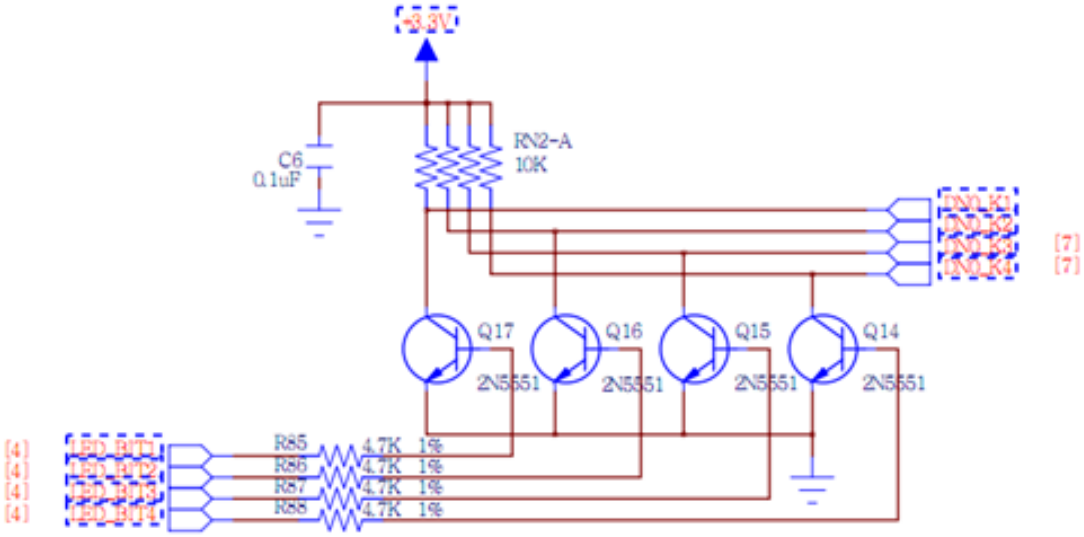

LED0
R93
560R 1%
D1
LED1
R97
560R 1%
D2
LED2
R98
560R 1%
D3
LED3
R99
560R 1%
D4
LED4
R100
560R 1%
D5
LED5
R101
560R 1%
D6
LED6
R102
560R 1%
D7
LED7
R103
560R 1%
D8
LED8
R104
560R 1%
D9
LED9
R105
560R 1%
D10
LED10
R106
560R 1%
D11
LED11
R107
560R 1%
D12
LED12
R108
560R 1%
D13
LED13
R109
560R 1%
D14
LED14
R33
560R 1%
D15
LED15
R64
560R 1%
D16

		FPGA IO PIN	
D1_0	LED1_0	K3	Green
D1_1	LED1_1	M1	Green
D1_2	LED1_2	L1	Green
D1_3	LED1_3	K6	Green
D1_4	LED1_4	J5	Green
D1_5	LED1_5	H5	Green
D1_6	LED1_6	H6	Green
D1_7	LED1_7	K1	Green
D2_0	LED2_0	K2	Green
D2_1	LED2_1	J2	Green
D2_2	LED2_2	J3	Green
D2_3	LED2_3	H4	Green
D2_4	LED2_4	J4	Green
D2_5	LED2_5	G3	Green
D2_6	LED2_6	G4	Green
D2_7	LED2_7	F6	Green

5.4

FPGA FPGA

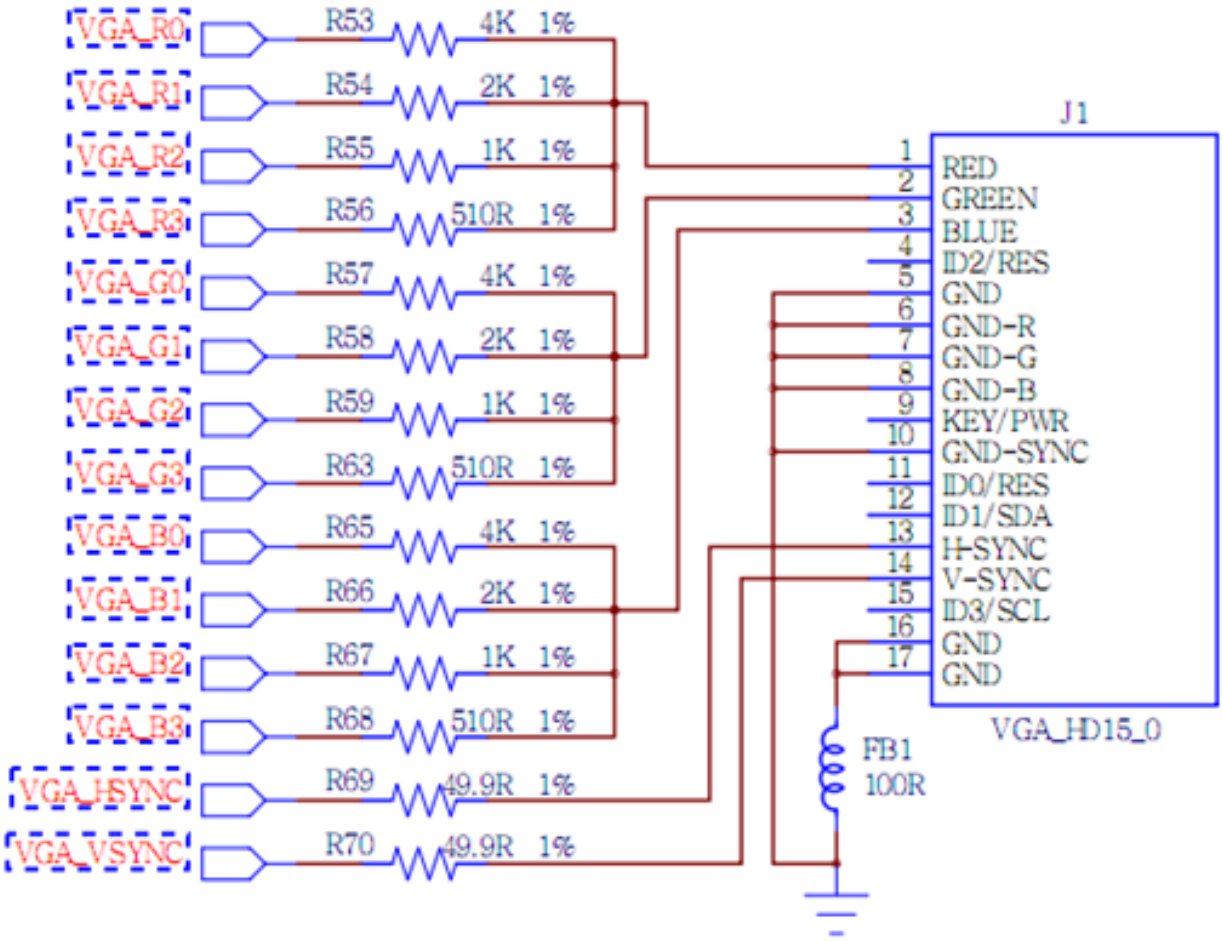




		FPGA IO PIN
A0	LED0_CA	B4
B0	LED0_CB	A4
C0	LED0_CC	A3
D0	LED0_CD	B1
E0	LED0_CE	A1
F0	LED0_CF	B3
G0	LED0_CG	B2
DP0	LED0_DP	D5
A1	LED1_CA	D4
B1	LED1_CB	E3
C1	LED1_CC	D3
D1	LED1_CD	F4
E1	LED1_CE	F3
F1	LED1_CF	E2
G1	LED1_CG	D2
DP1	LED1_DP	H2
DN0_K1	LED_BIT1	G2
DN0_K2	LED_BIT2	C2
DN0_K3	LED_BIT3	C1
DN0_K4	LED_BIT4	H1
DN1_K1	LED_BIT5	G1
DN1_K2	LED_BIT6	F1
DN1_K3	LED_BIT7	E1
DN1_K4	LED_BIT8	G6

1.3.6 6 VGA

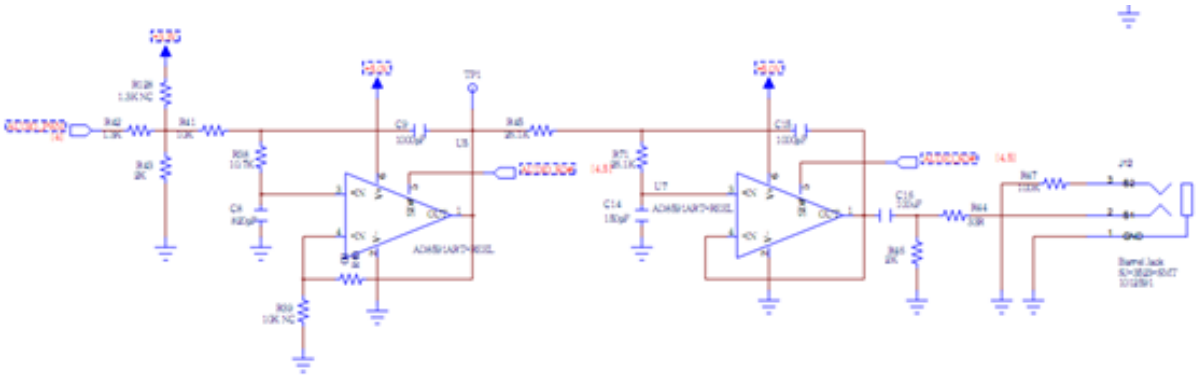
EGo1 VGA J1 14 FPGA 4



		FPGA IO PIN
RED	VGA_RO	F5
	VGA_R1	C6
	VGA_R2	C5
	VGA_R3	B7
GREEN	VGA_G0	B6
	VGA_G1	A6
	VGA_G2	A5
	VGA_G3	D8
BLUE	VGA_B0	C7
	VGA_B1	E6
	VGA_B2	E5
	VGA_B3	E7
H-SYNC	VGA_HSYNC	D7
V-SYNC	VGA_VSYNC	C4

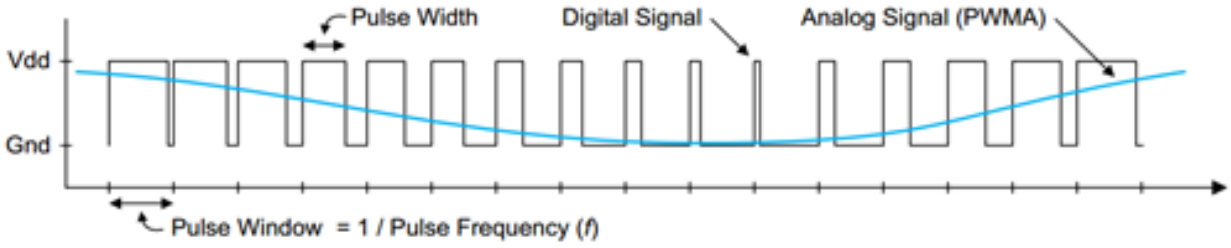
1.3.7 7

EGo1 J12 AUDIO_PWM FPGA PWM PDM

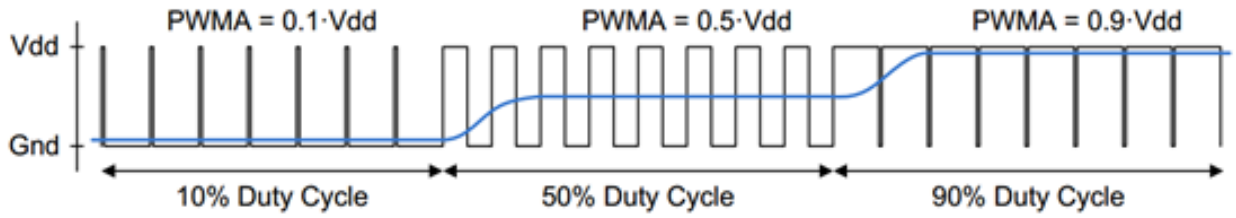


3dB 10% Vdd

PWM



3dB PWM PWM 5KHz PWM 50KHz PWM PWM



		FPGA IO PIN
AUDIO PWM	AUDIO_PWM	T1
AUDIO SD	SUDIO_SD#	M6

1.3.8 8 USB-UART/JTAG

UART/JTAG USB USB PC USB Xilinx Vivado

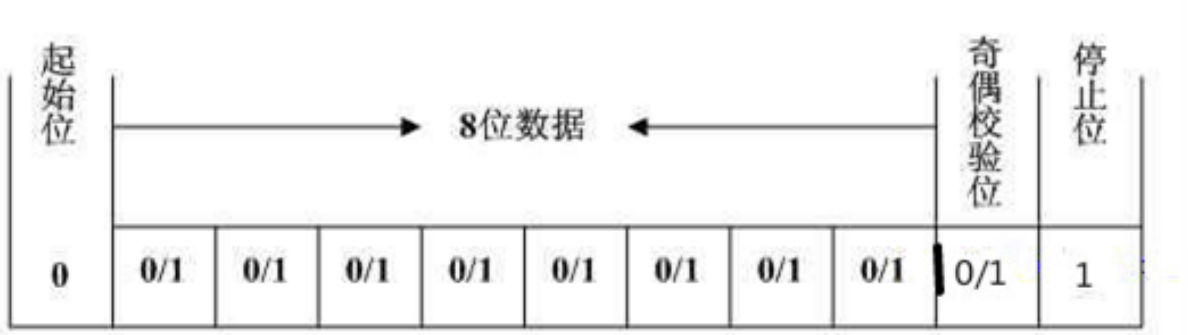
:

		FPGA IO PIN
UART RX	UART_RX	T4 FPGA
UART TX	UART_TX	N5 FPGA

UATR “ ” RXD TXD

1 8

UART



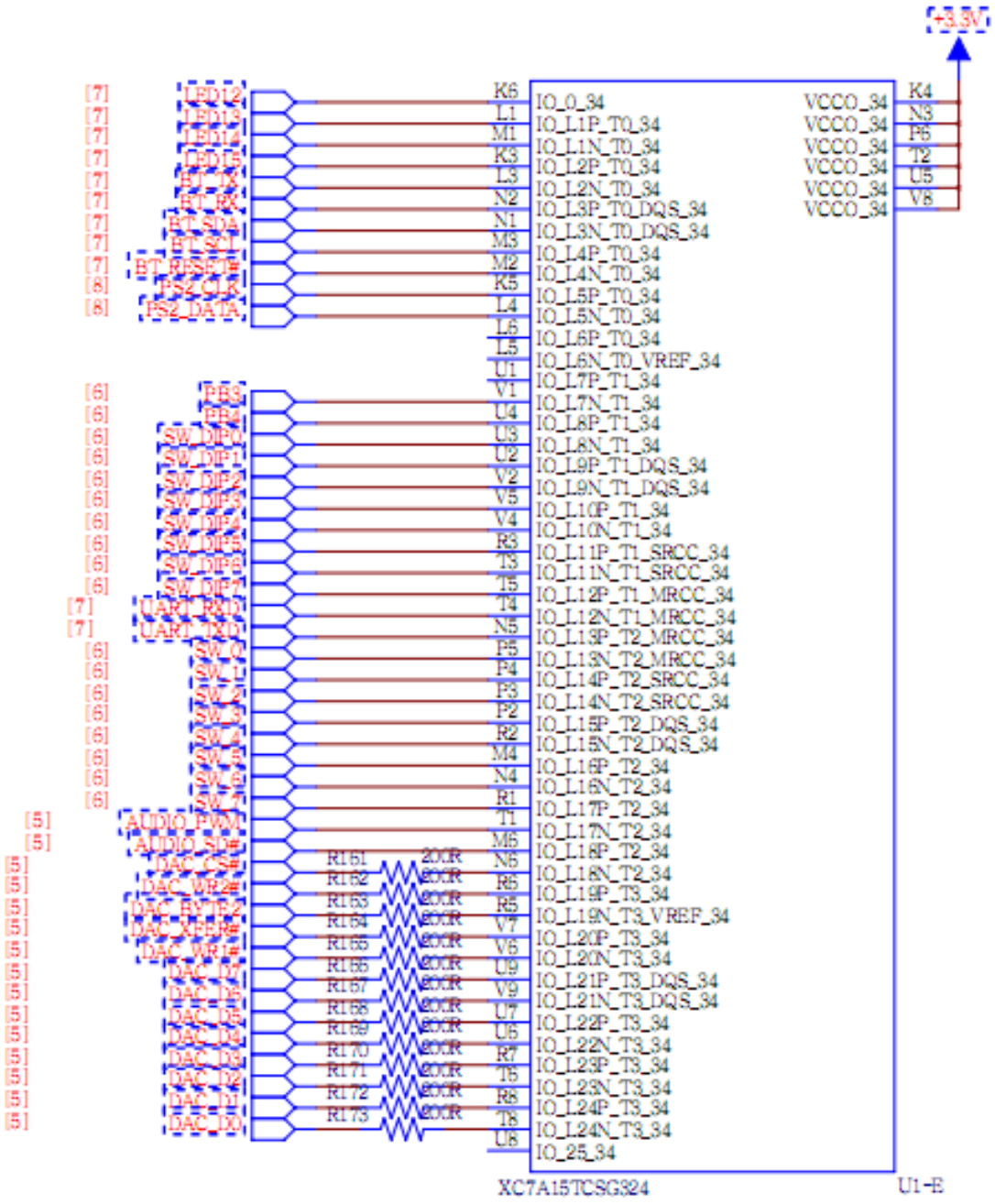
1.3.9 9 USB PS2

EGo1 USB USB J4 USB PIC24FJ128 PS/2 USB PS/2 FPGA

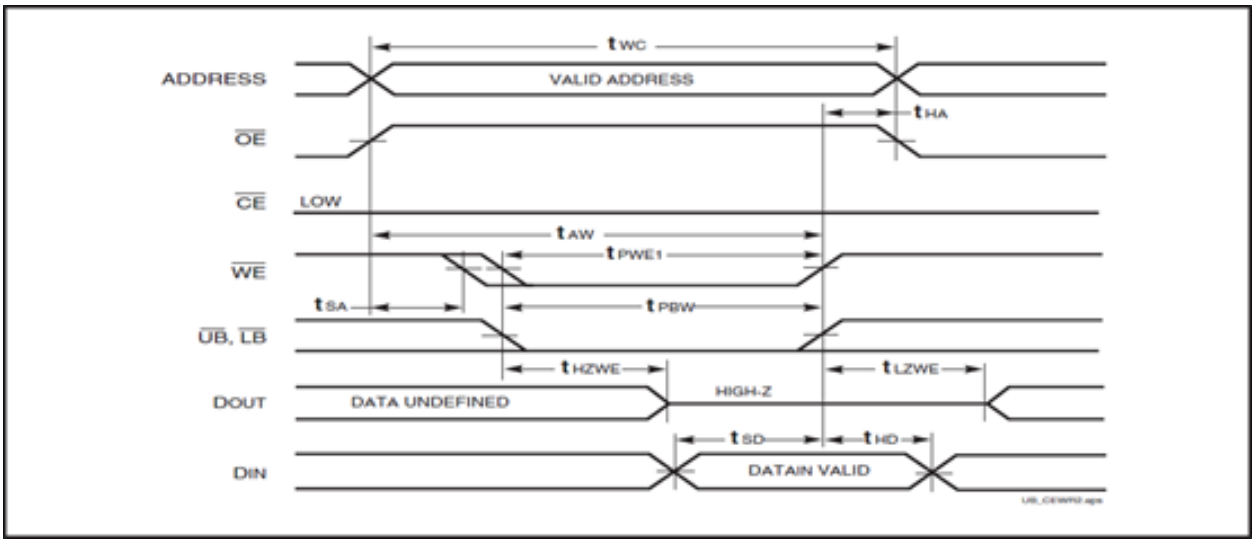
PIC24J128		FPGA IO PIN
15	PS2_CLK	K5
12	PS2_DATA	L4

1.3.10 10 SRAM

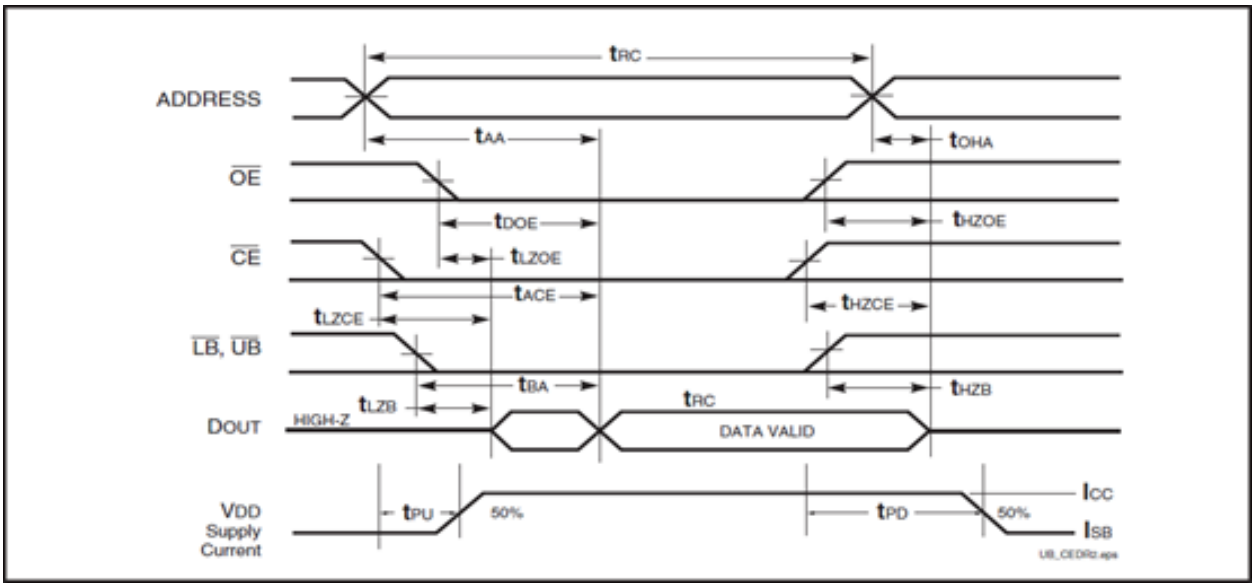
IS61WV12816BLL SRAM 2Mbit SRAM SRAM 8ns



SRAM SRAM



SRAM SRAM



SRAM		FPGA IO PIN
I/O0	MEM_D0	U17
I/O1	MEM_D1	U18
I/O2	MEM_D2	U16
I/O3	MEM_D3	V17
I/O4	MEM_D4	T11
I/O5	MEM_D5	U11
I/O6	MEM_D6	U12
I/O7	MEM_D7	V12
I/O8	MEM_D8	V10
I/O9	MEM_D9	V11
I/O10	MEM_D10	U14
I/O11	MEM_D11	V14

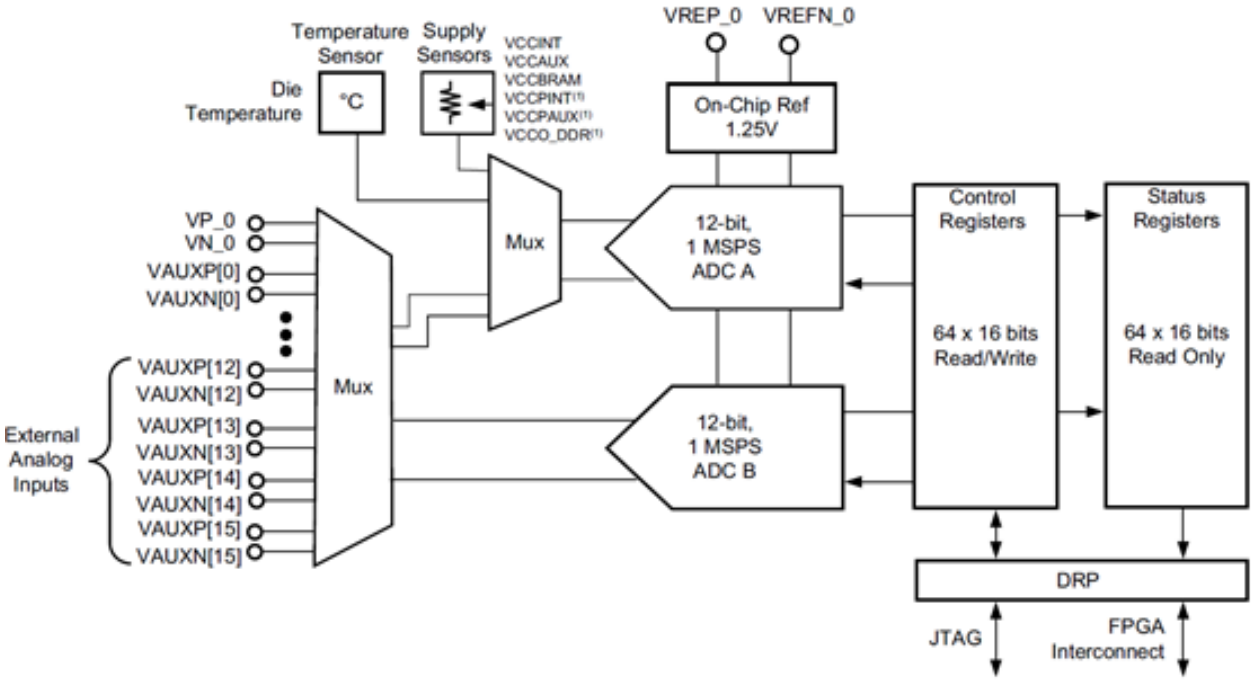
1 –

SRAM		FPGA IO PIN
I/O12	MEM_D12	T13
I/O13	MEM_D13	U13
I/O14	MEM_D14	T9
I/O15	MEM_D15	T10
A00	MEM_A00	T15
A01	MEM_A01	T14
A02	MEM_A02	N16
A03	MEM_A03	N15
A04	MEM_A04	M17
A05	MEM_A05	M16
A06	MEM_A06	P18
A07	MEM_A07	N17
A08	MEM_A08	P14
A09	MEM_A09	N14
A10	MEM_A10	T18
A11	MEM_A11	R18
A12	MEM_A12	M13
A13	MEM_A13	R13
A14	MEM_A14	R12
A15	MEM_A15	M18
A16	MEM_A16	L18
A17	MEM_A17	L16
A18	MEM_A18	L15
OE	SRAM_OE#	T16
CE	SRAM_CE#	V15
WE	SRAM_WE#	V16
UB	SRAM_UB	R16
LB	SRAM_LB	R10

1.3.11 11

Xilinx 7 FPGA 12bit 1MSPS ADC 17

XADC



XADC (VP/VN) 16 ADxP ADxN x 0 15

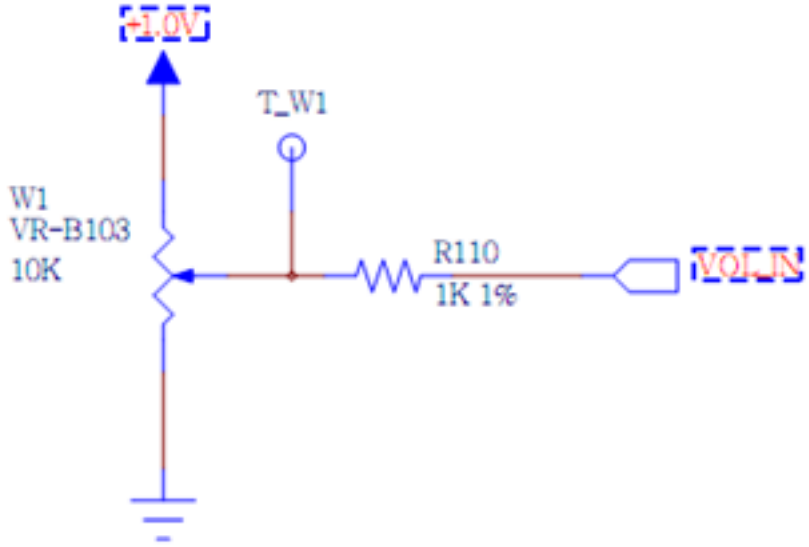
XADC status registers FPGA Dynamic Reconfiguration Port (DRP) 16 ADC JTAG TAP XADC FPGA JTAG XADC XADC XADC

XADC DRP JTAG XADC block attributes 41H SEQ3 SEQ0

SEQ3	SEQ2	SEQ1	SEQ0	Function
0	0	0	0	Default Mode
0	0	0	1	Single pass sequence
0	0	1	0	Continuous sequence mode
0	0	1	1	Single Channel mode (Sequencer Off)
0	1	X	X	Simultaneous Sampling Mode
1	0	X	X	Independent ADC Mode
1	1	X	X	Default Mode

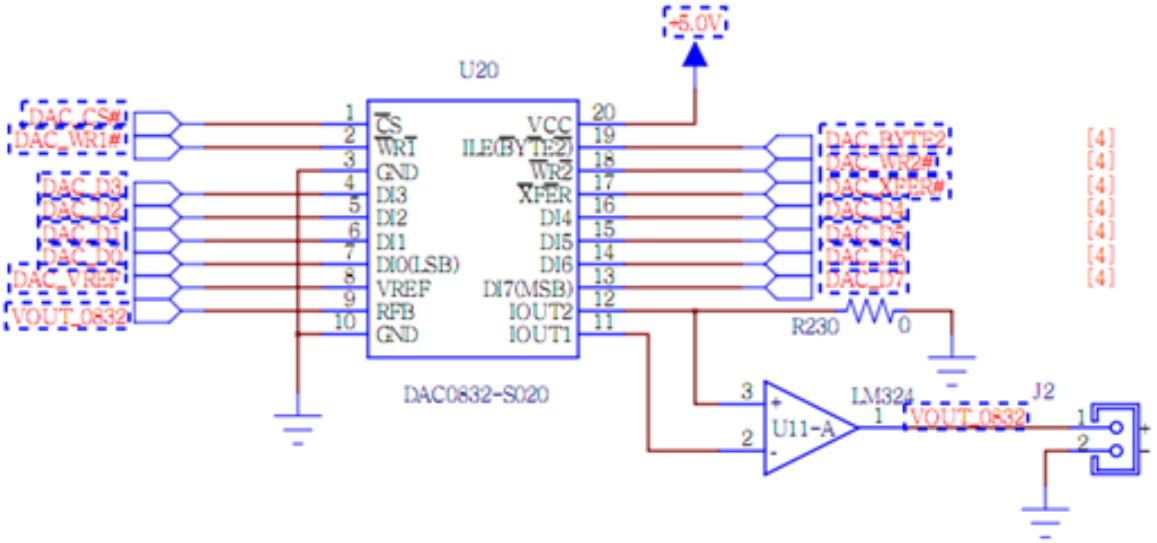
XADC FPGA JTAG XADC XADC FPGA ZYNQ PS ADC XADC ug480_7Series

EGo1 W1 FPGA 0 ~ 1V FPGA C12 1 ADC

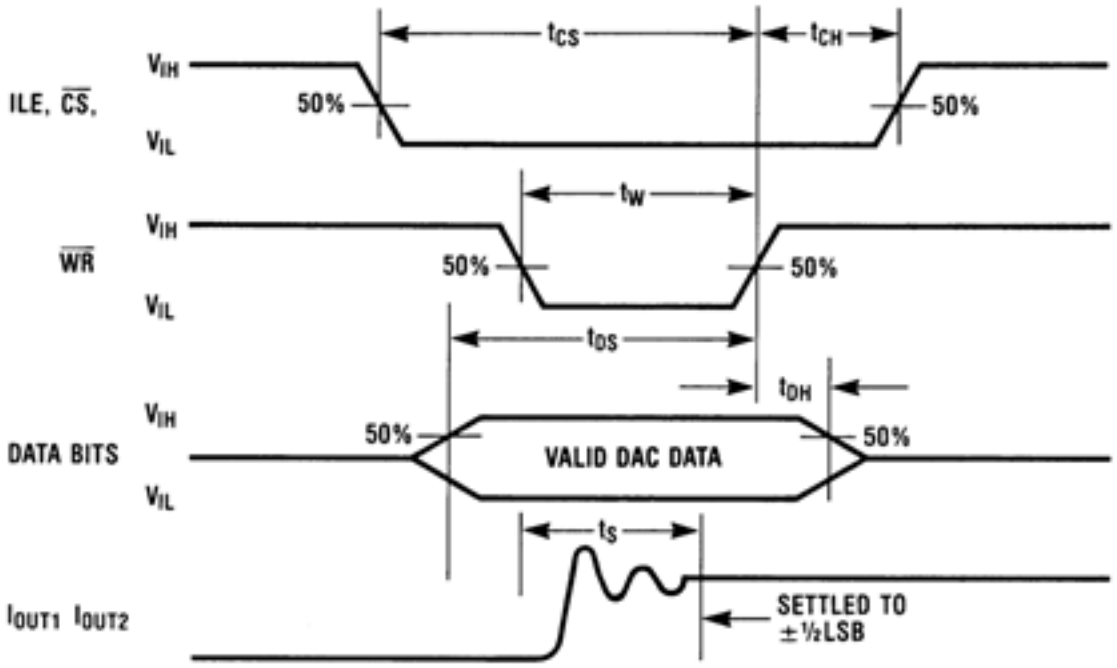


1.3.12 12 DAC

EGo1 8 DAC0832 DAC J2



DAC0832 DAC0832

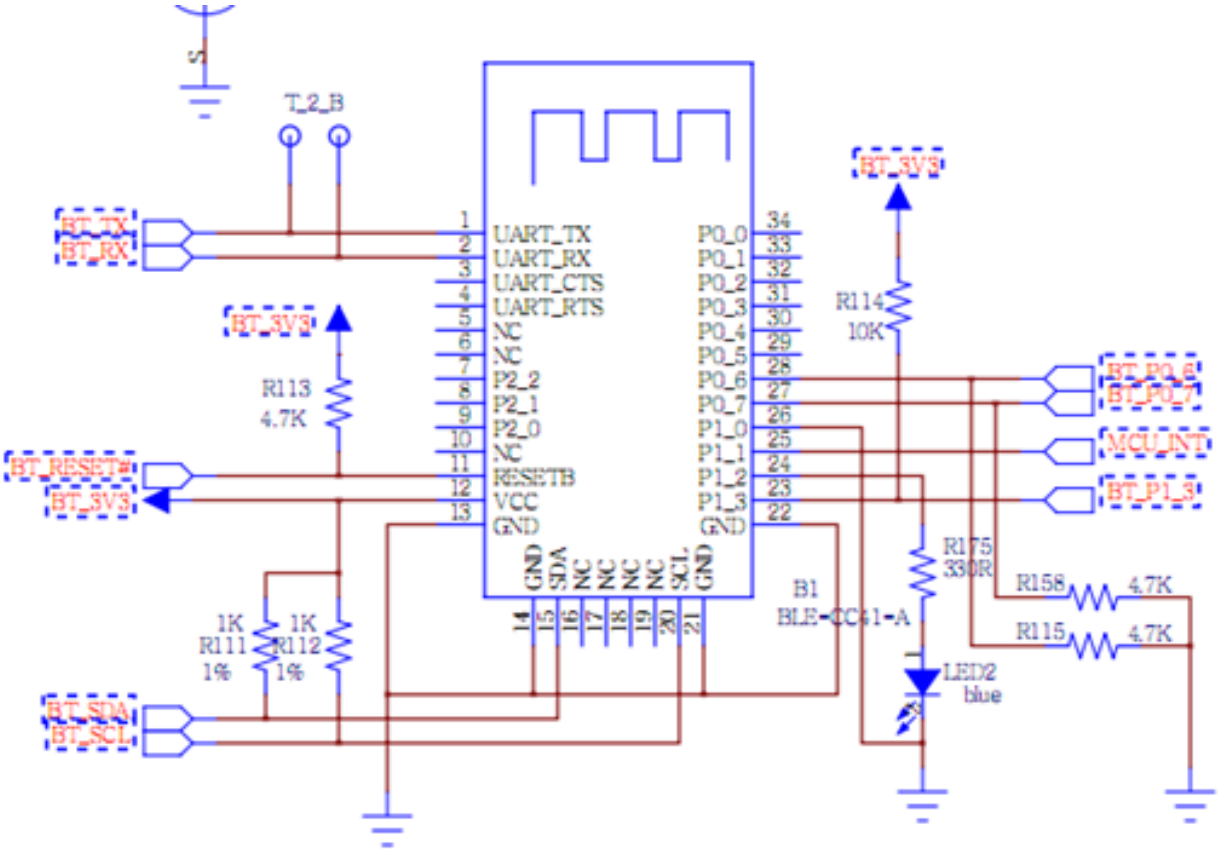


:

DAC0832		FPGA IO PIN
DI0	DAC_D0	T8
DI1	DAC_D1	R8
DI2	DAC_D2	T6
DI3	DAC_D3	R7
DI4	DAC_D4	U6
DI5	DAC_D5	U7
DI6	DAC_D6	V9
DI7	DAC_D7	U9
ILE(BYTE2)	DAC_BYTE2	R5
CS	DAC_CS#	N6
WR1	DAC_WR1#	V6
WR2	DAC_WR2#	R6
XFER	DAC_XFER#	V7

1.3.13 13

EGo1 BLE-CC41-A FPGA 1200 2400 4800 9600 14400 19200 38400 57600 115200 230400bps 9600bps

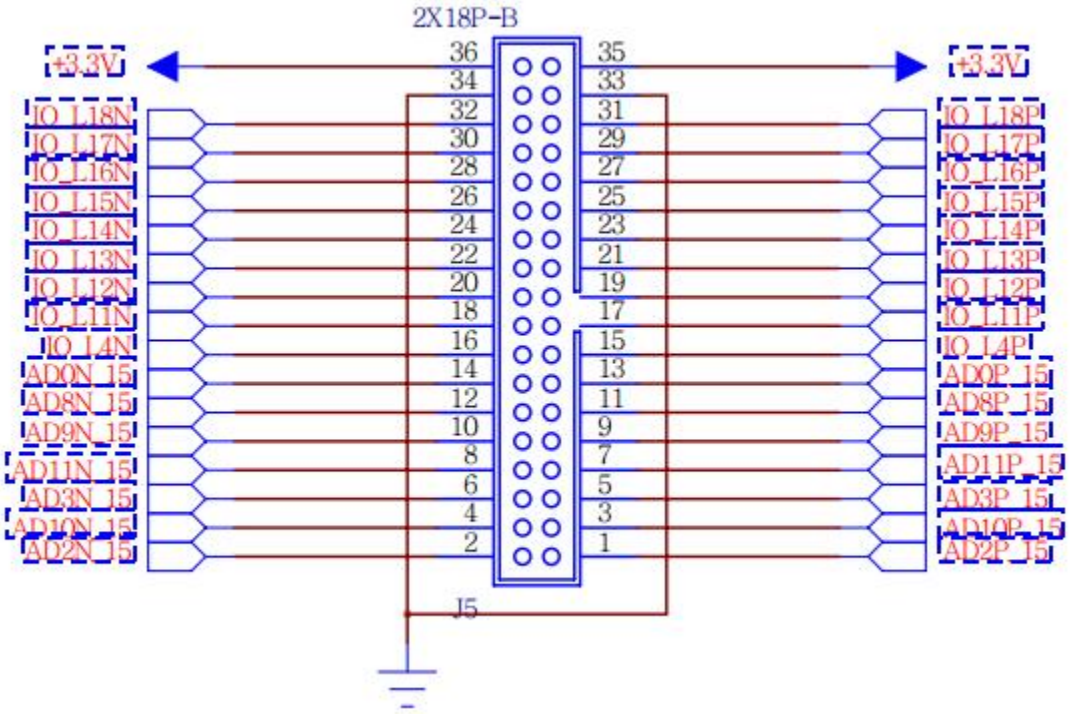


:

BLE-CC41-A		FPGA IO PIN
UART_RX	BT_RX	N2 FPGA
UART_TX	BT_TX	L3 FPGA

1.3.14 14 I/O

EGo1 J5 I/O 32 IO IO



2x18		FPGA IO PIN
1	AD2P_15	B16
2	AD2N_15	B17
3	AD10P_15	A15
4	AD10N_15	A16
5	AD3P_15	A13
6	AD3N_15	A14
7	AD11P_15	B18
8	AD11N_15	A18
9	AD9P_15	F13
10	AD9N_15	F14
11	AD8P_15	B13
12	AD8N_15	B14
13	AD0P_15	D14
14	AD0N_15	C14
15	IO_L4P	B11
16	IO_L4N	A11
17	IO_L11P	E15
18	IO_L11N	E16
19	IO_L12P	D15
20	IO_L12N	C15
21	IO_L13P	H16
22	IO_L13N	G16
23	IO_L14P	F15
24	IO_L14N	F16
25	IO_L15P	H14

2 –

2x18		FPGA IO PIN
26	IO_L15N	G14
27	IO_L16P	E17
28	IO_L16N	D17
29	IO_L17P	K13
30	IO_L17N	J13
31	IO_L18P	H17
32	IO_L18N	G17

1.4 Demo

Bit http://pan.baidu.com/s/1dF04v65

1.4.1 EGo1_demo_01

WSAD EGo1 (P15) WSAD 16

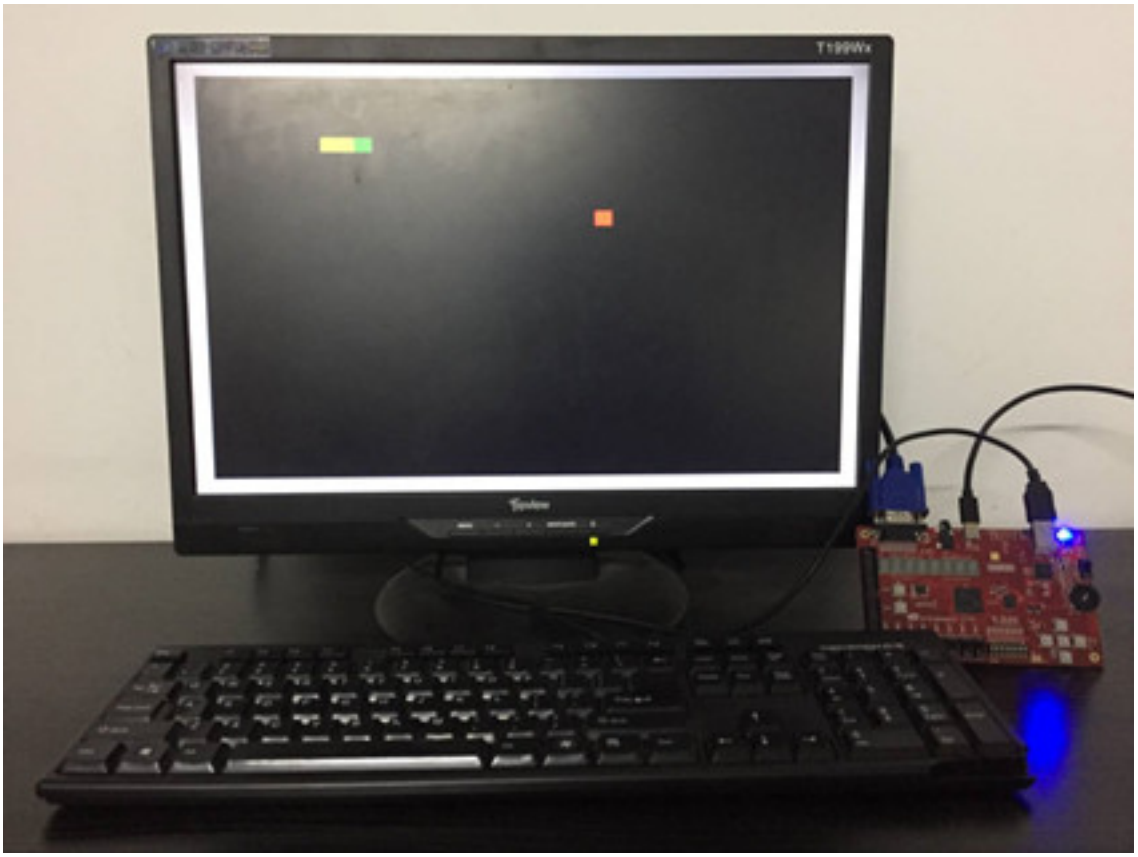
1. vivado “Open Hardware Manager”

2. Micro USB JTAG VGA USB USB-PS/2 “Hardware Manager” “Open target” “Auto Connect”

3. “Program Device”

4. “Bitstream File” bit “Program” FPGA

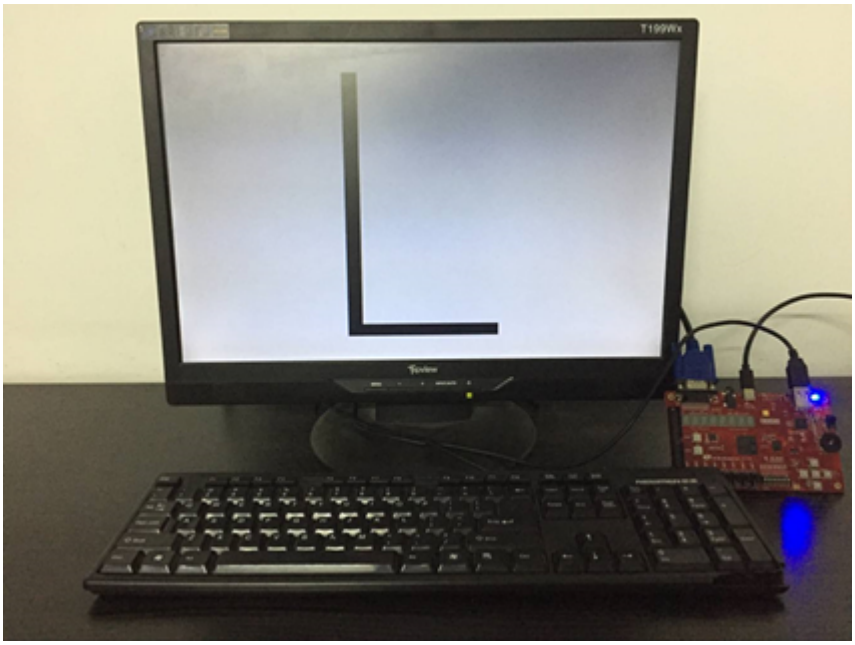
5. WSAD 16



1.4.2 EGo1_demo_02

640*480 160*10 10 20*20 WSAD L V (P15)

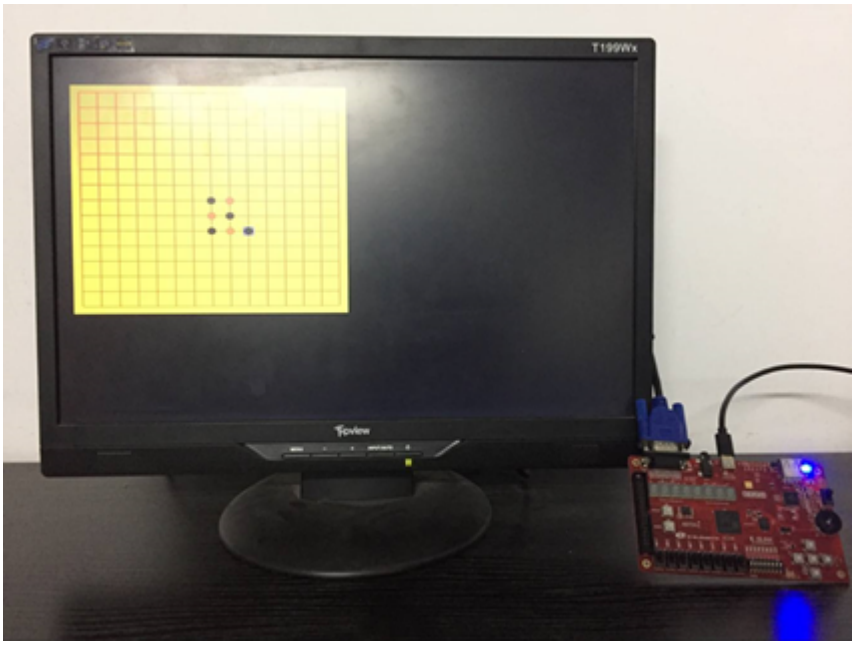
1. vivado “Open Hardware Manager”
2. Micro USB JTAG VGA USB USB-PS/2 “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5. WSAD L (P15) V



1.4.3 EGo1_demo_03

S4(U4) S1(R17) S3(V1) S0(R11) S2(R15) WIN

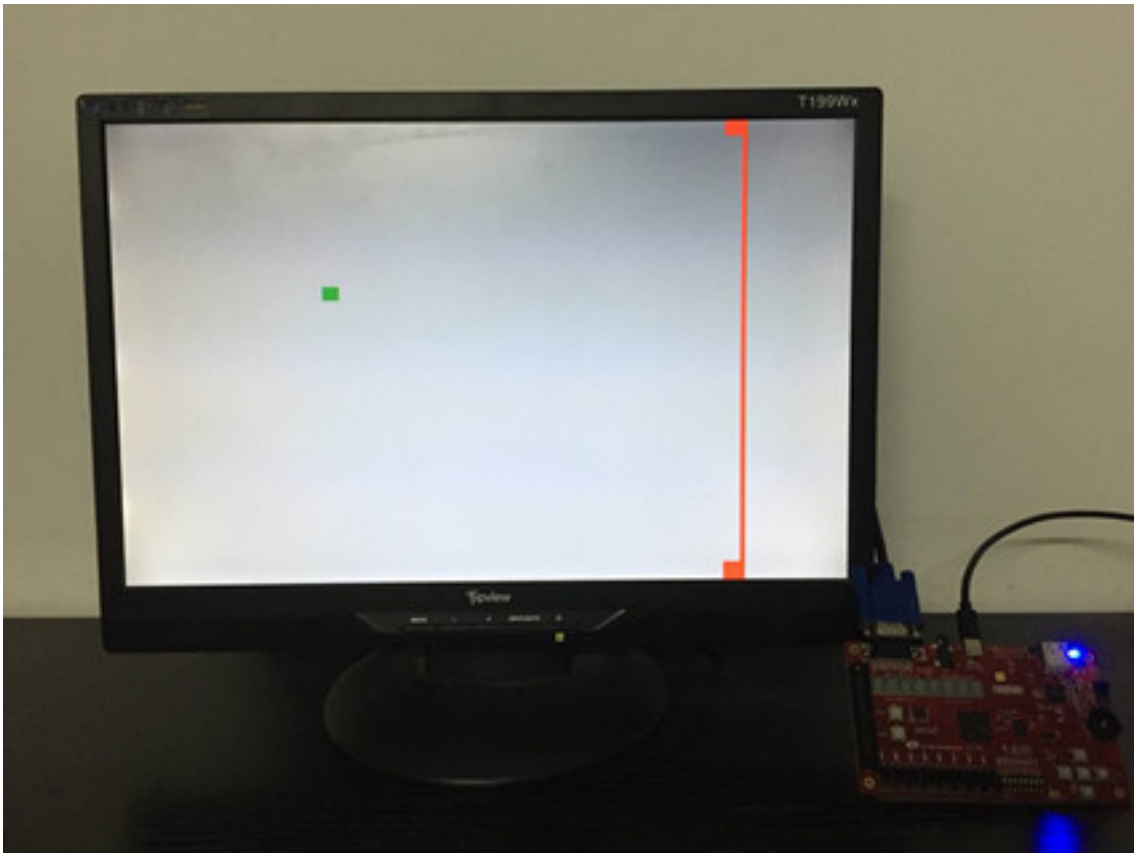
1. vivado “Open Hardware Manager”
2. Micro USB JTAG VGA “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5. S4(U4) S1(R17) S3(V1) S0(R11) S2(R15) WIN



1.4.4 EGo1_demo_04

Ego1 S2(R15) “√”

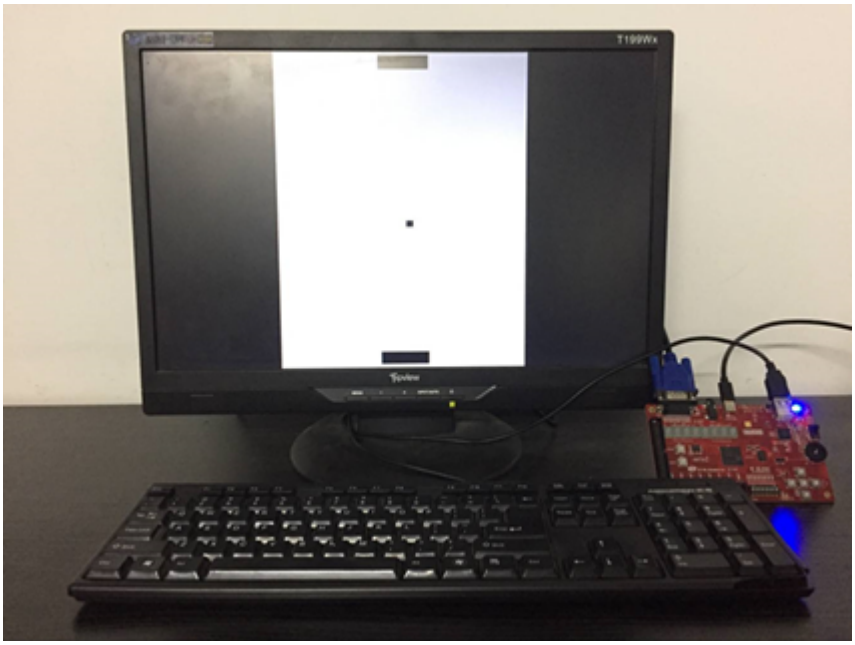
1. vivado “Open Hardware Manager”
2. Micro USB JTAG VGA “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5. S0(R11) 2(R15) “√” “ S0(R11)



1.4.5 EGo1_demo_05

Ego1 S3(V1) S0(R11) 4 6 EGo1 S2(R15),

1. vivado “Open Hardware Manager”
2. Micro USB JTAG VGA USB USB-PS/2 “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5. S2(R15) Ego1 S3(V1) S0(R11) 4 6 S2(R15)



1.4.6 EGo1_demo_06

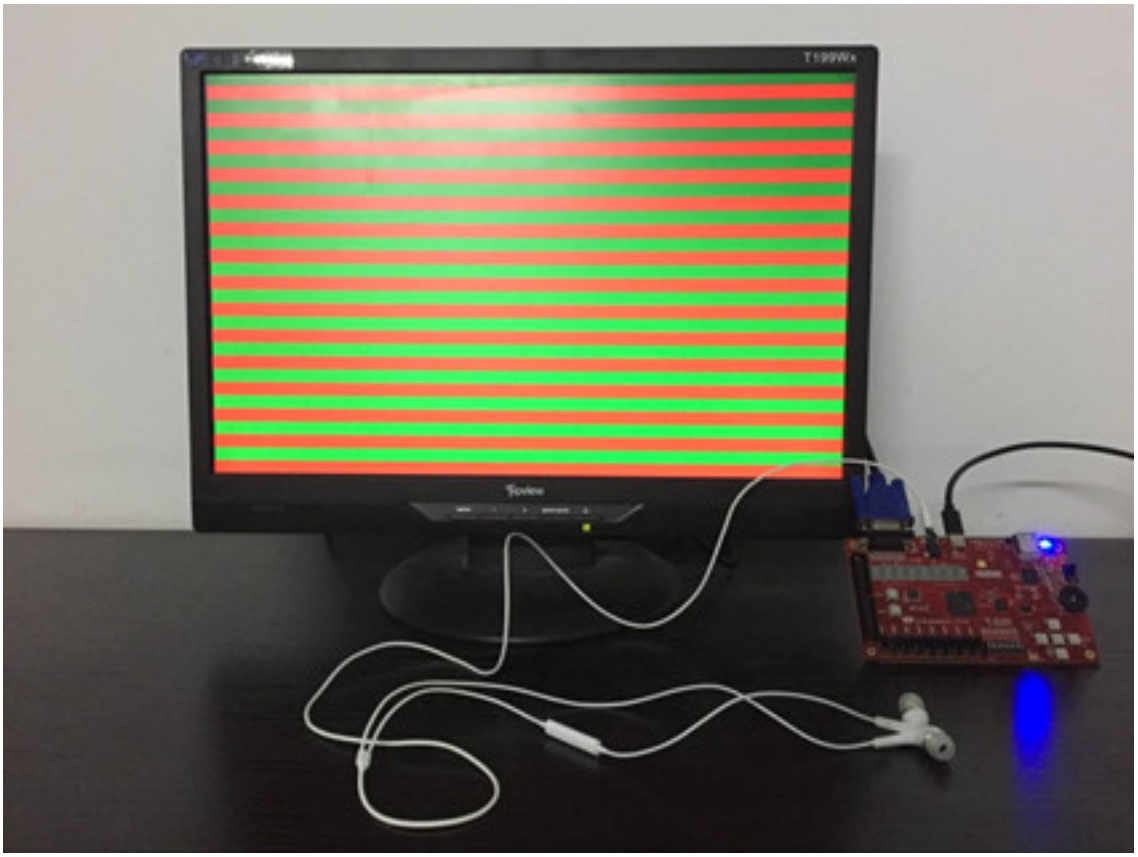
VGA EGo1 VGA VGA 64080@60Hz Logo ROM Logo

1. vivado “Open Hardware Manager”
2. Micro USB JTAG VGA “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5.logo S6(P15)

1.4.7 EGo1_demo_07

EGo1 3.5mm AD8891ART

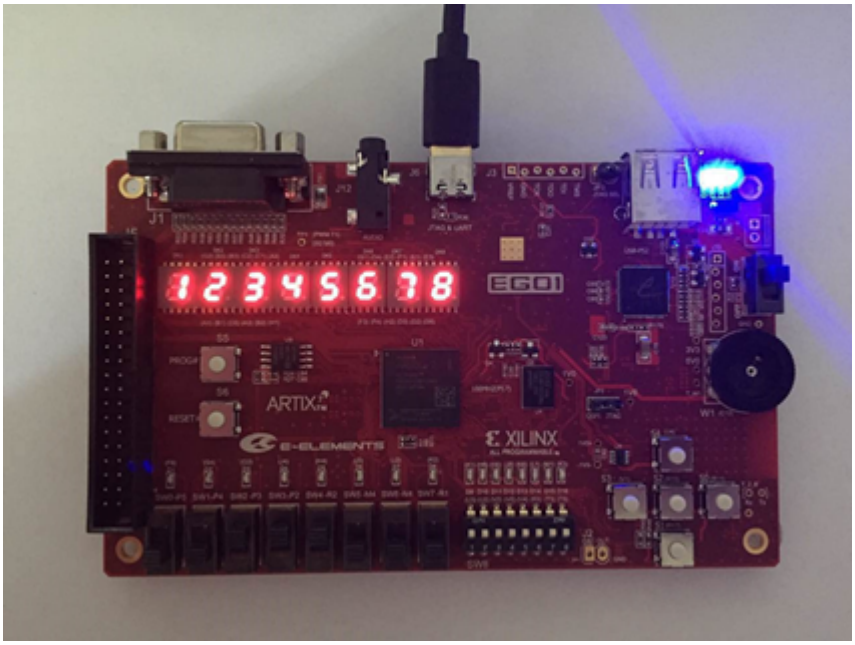
1. vivado “Open Hardware Manager”
2. Micro USB JTAG VGA “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5. SW0(P5) DIP_SW0(U3),



1.4.8 EGo1_demo_08

4.0 FPGA UART
FPGA 1 *Naaaa 2 *Waaaaaaaa
* N W a N 16bit W 32bit N LED 16bit
16 LED W 32bit 8

1. vivado “Open Hardware Manager”
2. Micro USB JTAG “Hardware Manager” “Open target” “Auto Connect”
3. “Program Device”
4. “Bitstream File” bit “Program” FPGA
5. SW6 SW7 SW3 SW4 SW5 SW5 slave LED2 BLE APP
APP LED2 APP *W12345678 “ ” 12345678



1.5 Example design

EGo1 https://pan.baidu.com/s/13jtm8jNKg6eC0QSeO25wQA x6cz