MESI state transition diagram and details

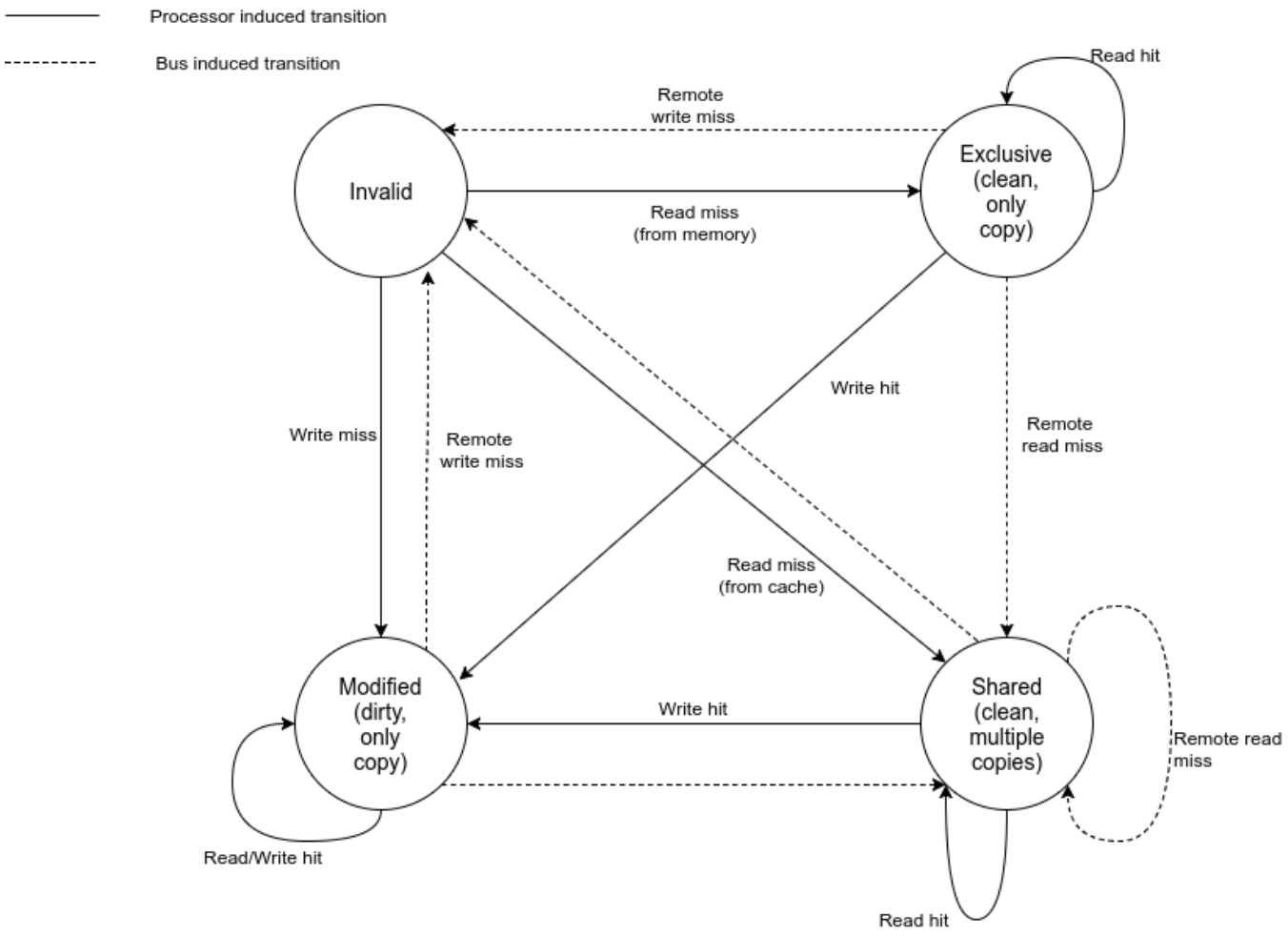

Figure 1: MESI cache coherence protocol state diagram

Actions to be performed on different memory access requests:

Read miss:

- Place read request on the bus.
- Reply from memory –> `exclusive` state.
- Reply from cache –> `shared` state.

Read hit, bus read hit:

- No state change.

Bus read miss:

- `exclusive` –> `shared`, provide copy.
- `shared` –> `shared`, provide copy.
- `modified` –> `shared`, provide copy, and writeback.

Write miss:

- Place request on the bus.
- Reply from memory –> `modified` state.
- Reply from cache –> `modified` state.

Write hit:

- `exclusive` –> `modified` state (no bus transaction).
- `modified` –> `modified` state (no bus transaction).
- `shared` –> place request on bus (to propagate 'invalidate'), go to `modified` state.

Bus write miss:

- `exclusive` –> `invalid`, provide copy.
- `shared` –> `invalid`, provide copy (any 1 core that is currently sharing the block can provide the copy).
- `modified` –> `invalid`, provide copy.

Bus write hit:

- `shared` –> invalid.
- `exclusive` (impossible).
- `modified` (impossible).