

Figure 10 is a line graph showing the scaling of the number of nodes (N) versus the number of processors (P) for different memory configurations. The x-axis represents the number of processors (P) from 0 to 50, and the y-axis represents the number of nodes (N) from 0 to 50. The graph contains ten data series, each representing a different memory configuration and its corresponding θ_{ca} value. The series are:

- DDR4-2400 4Ch $\theta_{ca}=0.31230$
- DDR4-2400 6Ch $\theta_{ca}=0.29738$
- DDR4-3200 4Ch $\theta_{ca}=0.28983$
- DDR4-3200 6Ch $\theta_{ca}=0.26682$
- DDR5-4800 4Ch $\theta_{ca}=0.22627$
- DDR5-4800 6Ch $\theta_{ca}=0.18770$
- DDR5-5600 4Ch $\theta_{ca}=0.19493$
- DDR5-5600 4Ch $\theta_{ca}=0.18911$
- DDR5-5600 6Ch $\theta_{ca}=0.14590$
- HBM2 4Ch $\theta_{ca}=0.28629$

The DDR5-5600 6Ch series shows the highest scaling, reaching N=50 at P=50. The HBM2 4Ch series shows the lowest scaling, reaching N=50 at P=50. A gray shaded region highlights the area between the DDR5-5600 4Ch ($\theta_{ca}=0.19493$) and DDR5-5600 6Ch ($\theta_{ca}=0.14590$) series.

