

28.2.2 EPT Translation Mechanism

1. Page Map Level-4 (PML4—holds PML4Es)

- A 4KB naturally aligned EPT PML4 table is located at the physical address specified in bits **51:12** (40 bits) of the EPTP, a VM-execution control field
 - An EPT PML4 table comprises 512 64-bit entries (EPT PML4Es)
 - An EPT **PML4E** is selected using the physical address defined as follows:
 - Bits **63:52** (12 bits) are all **0**
 - Bits **51:12** (40 bits) are from the **EPTP**
 - Bits **11:3** (9 bits) are bits **47:39** (9 bits) of the **guest-physical address**
 - Bits **2:0** (3 bits) are all **0**
 - Because an EPT **PML4E** is identified using bits **47:39** (9 bits) of the **guest-physical address**, it controls access to a 512GB region of the guest-physical-address space

(The format of an EPT PML4E is given in Table 28-1)

2. Page Directory Pointer Table (PDPT—holds PDPTEs)

- A 4KB naturally aligned EPT PDPT is located at the physical address specified in bits **51:12** of the EPT PML4E
 - An EPT PDPT comprises 512 64-bit entries (EPT PDPTEs)
 - An EPT **PDPTE** is selected using the physical address defined as follows:
 - Bits **63:52** (12 bits) are all **0**
 - Bits **51:12** (40 bits) are from the EPT **PML4E**
 - Bits **11:3** (9 bits) are bits **38:30** (9 bits) of the **guest-physical address**
 - Bits **2:0** (3 bits) are all **0**
 - Because an EPT **PDPTE** is identified using bits **47:30** (18 bits) of the **guest-physical address**, it controls access to a 1GB region of the guest-physical-address space
 - **Use of the PDPTE depends on the value of bit 7 in that entry**
 - If bit 7 of the EPT PDPTE is **SET**:
 - The EPT **PDPTE** maps a **1GB page**
 - The **FINAL physical address** [of the 1GB page] is computed as follows:
 - Bits **63:52** (12 bits) are all **0**
 - Bits **51:30** (22 bits) are from the EPT **PDPTE**
 - Bits **29:0** (30 bits) are from the original **guest-physical address**

(The format of an EPT PDPTE that maps a 1GB page is given in Table 28-2)

28.2.2 EPT Translation Mechanism (Cont.)

- If **bit 7** of the EPT PDPTE is **UNSET**:
 - The EPT **PDPTE** maps a **4KB naturally aligned EPT page directory (PD)** at the **physical address** specified in bits **51:12** (40 bits) of the EPT **PDPTE**
(The format of an EPT PDPTE that references an EPT page directory is given in Table 28-3)

3. Page Directory (PD—holds PDEs)

- A **4KB naturally aligned EPT PD** is located at the **physical address** specified in bits **51:12** of the EPT **PDPTE**
- An EPT PD comprises 512 64-bit entries (PDEs)
- An EPT **PDE** is **selected using the physical address** defined as follows:
 - Bits **63:52 (12 bits)** are all **0**
 - Bits **51:12 (40 bits)** are from the EPT **PDPTE**
 - Bits **11:3 (9 bits)** are bits **29:21** of the **guest-physical address**
 - Bits **2:0 (3 bits)** are all **0**
 - Because an EPT **PDE** is identified using bits **47:21** of the **guest-physical address**, it controls access to a 2MB region of the guest-physical-address space
 - **Use of the EPT PDE depends on** the value of **bit 7** in that entry:
 - If **bit 7** of the EPT PDE is **SET**:
 - The EPT **PDE** maps a **2MB page**
 - The final physical address is computed as follows:
 - Bits **63:52 (12 bits)** are all **0**
 - Bits **51:21 (31 bits)** are from the EPT **PDE**
 - Bits **20:0 (21 bits)** are from the **original guest-physical address**

(The format of an EPT PDE that maps a 2-MByte page is given in Table 28-4)
 - If **bit 7** of the EPT PDE is **UNSET**:
 - A **4KB naturally aligned EPT page table** is located at the **physical address** specified in bits **51:12** (31 bits) of the EPT **PDE**.
(The format of an EPT PDE that references an EPT page table is given in Table 28-5)

28.2.2 EPT Translation Mechanism (Cont.)

4. Page Table (PT—holds PTEs)

- A 4KB naturally aligned EPT page table is located at the physical address specified in bits 51:12 of the EPT PDE
- An EPT page table comprises 512 64-bit entries (PTEs).
- An EPT PTE is selected using a physical address defined as follows:
 - Bits 63:52 (12 bits) are all 0
 - Bits 51:12 (40 bits) are from the EPT PDE
 - Bits 11:3 (9 bits) are bits 20:12 (9 bits) of the guest-physical address
 - Bits 2:0 (3 bits) are all 0
- Because an EPT PTE is identified using bits 47:12 (36 bits) of the guest-physical address, every EPT PTE maps a 4KB page
- The FINAL physical address is computed as follows:
 - Bits 63:52 (12 bits) are all 0
 - Bits 51:12 (40 bits) are from the EPT PTE
 - Bits 11:0 (12 bits) are from the original guest-physical address

(The format of an EPT PTE is given in Table 28-6)