Analog Electronics

FET Amplifiers

Tutorial 4

The Common-Source Amplifier

1. Determine I_D and V_{GS} at the Q point for the JFET amplifier in Figure 1. The typical I_{DSS} for this particular JFET is 4.3 mA and $V_{GS(off)}$ is -7.7 V. [5 marks]

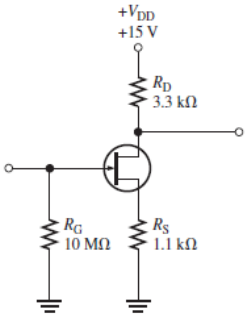

Figure 1

2. Calculate the dc voltages from each terminal to ground for the FETs in Figure 2. [5 marks]

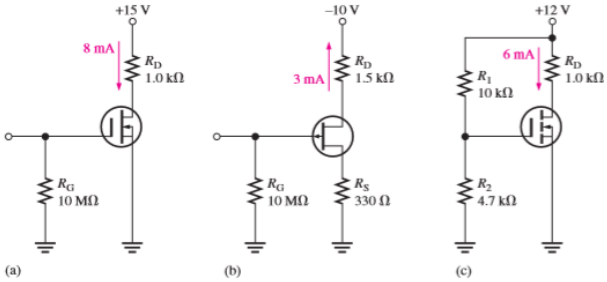

Figure 2

3. Given that I_D=2.83 mA in Figure 3, find V_{DS} and V_{GS}. $V_{GS(off)}$ = -7 V and I_{DSS} = 8 mA. [4 marks]

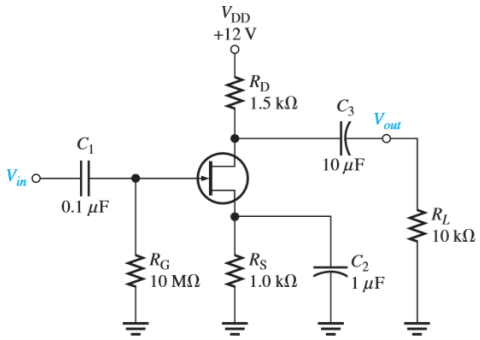

Figure 3

4. If a 50 mV rms input signal is applied to the amplifier in Figure 3, what is the peak to peak output voltage? g_m = 5000 µS. [5 marks]

5. Determine the voltage gain of each common-source amplifier in Figure 4. [8 marks]

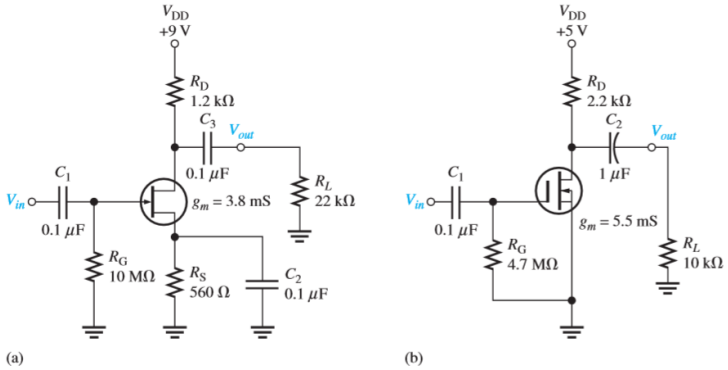

Figure 4

6. Draw the dc and ac equivalent circuits for the amplifier in Figure 5. [4 marks]

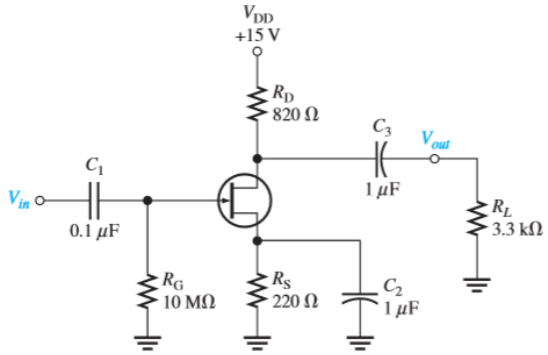

Figure 5

7. A resistor 4.7 kOhm is connected in parallel with R_L in Figure 5. What is the voltage gain? g_m=4.41 mS [5 marks]

8. What input resistance is seen by the signal source? I_{GSS} = 25 nA, V_{GS} = -15 V. [8 marks]

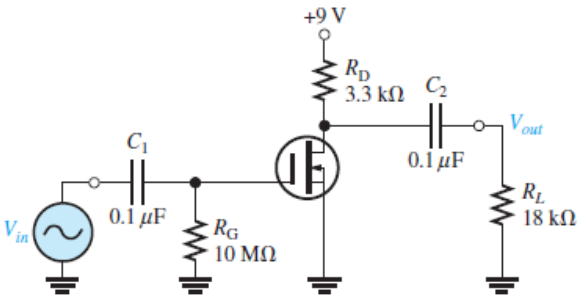

Figure 6

The Common Drain Amplifier

9. For the source follower in Figure 7, determine the voltage gain and input resistance, I_{GSS} = 50 pA at V_{GS} = -15 V and g_m = 5500 µS. [15 marks]

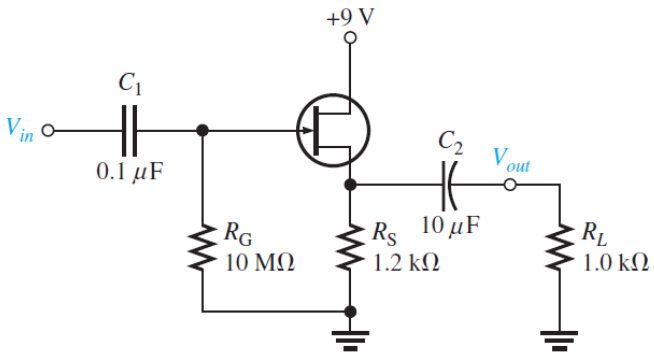

Figure 7

The Common Gate Amplifier

10. Determine the voltage gain and input resistance of the common-gate amplifier in Figure 8. [8 marks]

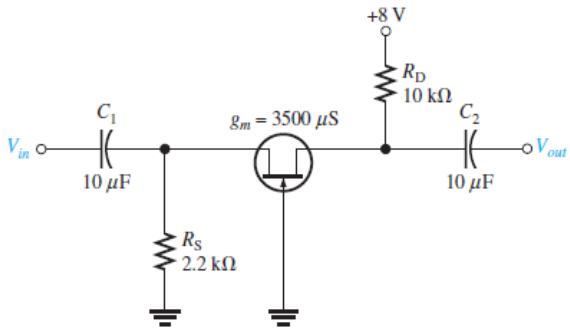

Figure 8

11. Common gate amplifier [12 marks]

- Determine the minimum voltage gain and input resistance of amplifier in Figure 9, given that g_m=2000 uS, I_{GSS} = 5 nA, V_{GS} = 20 V.
- Why V_{DD} is negative?
- What is the type of given semiconductor device?

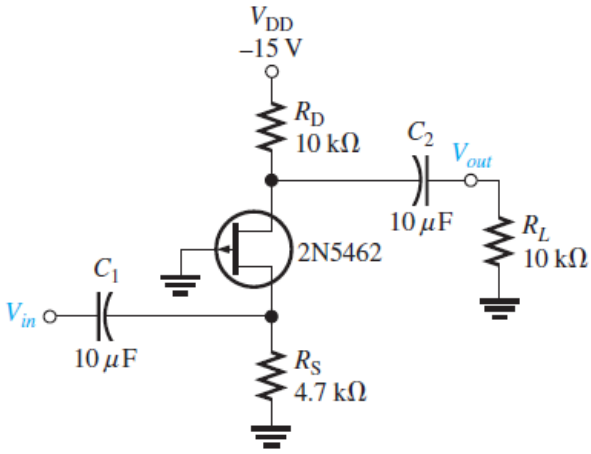

Figure 9

12. NAND gate is created by using MOSFETs. Gate consists of 2 inputs and an output. According to the Figure 10, fill the given table. [8 marks]

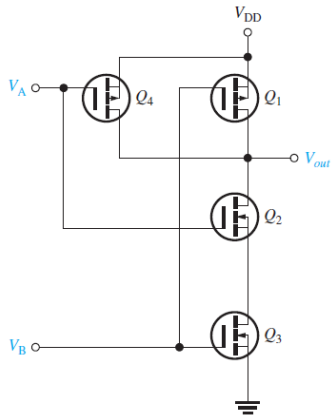

Figure 10

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0					
0	V_{DD}					
V_{DD}	0					
V_{DD}	V_{DD}					

13. Fill the table, in case, previous gate is replaced with NOR gate. [8 marks]

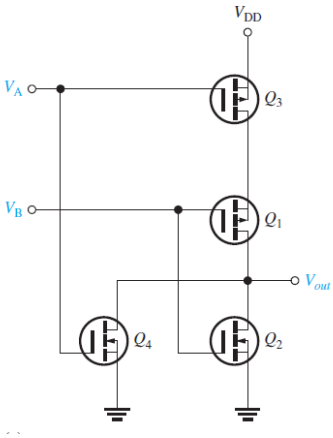

Figure 11

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0					
0	V_{DD}					
V_{DD}	0					
V_{DD}	V_{DD}					

14. A pulse waveform is applied to a CMOS inverter as shown in Figure 12. Determine the output waveform and explain the operation. [5 marks]

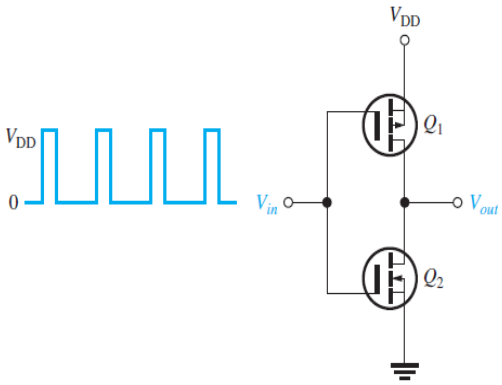

Figure 12