# Yixin Luo

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## EDUCATION

### CARNEGIE MELLON UNIVERSITY
PhD in Computer Science
Dec 2017 | Pittsburgh, PA

### UNIVERSITY OF MICHIGAN
BS in Computer Science
May 2012 | Ann Arbor, MI
Dean's List 2010, 2011, EECS Scholar 2010

### SHANGHAI JIAO TONG UNIVERSITY
BS in Electrical Engineering
May 2012 | Shanghai, China
Dean's List 2009

## LINKS

Github:// **camellyx**
LinkedIn:// **luoyixin**

## COURSEWORK

### GRADUATE
Deep Learning
Advanced Database Systems
Deep Reinforcement Learning
Machine Learning
Optimizing Compilers
Operating Systems and Distributed Systems
Advanced Cloud Computing
Graduate Algorithms
Computer Architecture
Computer Networks
*(Teaching Assistant)*
Parallel Computer Arch. and Programming
Parallel Computer Architecture

### UNDERGRADUATE
Computer Architecture + Major Design Proj.
VLSI Design + Major Design Proj.
Microprocessor-Based Systems
Operating Systems
Artificial Intelligence
Honors Mathematics

## SKILLS

### PROGRAMMING
Over 10,000 lines:
C++ • Python • Matlab • Shell • Verilog • LaTeX
Familiar:
Perl • HTML • Windows Batch • TensorFlow • PyTorch
Simulator & Tools:
Intel Pin • HSPICE • Cadence tools • gem5 • Multi2Sim • MySQL/PostgreSQL

## EXPERIENCE

### SEAGATE TECHNOLOGY | Engineering Intern
May 2015 – Oct. 2015; May 2016 – Aug 2016 | Lakeview, CA
- Developed new tool to automatically test and analyze seven types of SSD errors
- Collected and analyzed 700 GB of SSD error data from real devices using data mining and statistical modeling techniques
- Developed four new models and ten new techniques to improve SSD lifetime

### MICROSOFT RESEARCH | Research Intern
May 2014 – Aug. 2014 | Redmond, WA
- Developed new server architecture that can reduce datacenter TCO by 2.7%.
- Characterized memory error vulnerability of three important data-intensive applications running in datacenters

## RESEARCH

### CARNEGIE MELLON UNIVERSITY | Graduate Research Assistant
Sep. 2012 – Present | Pittsburgh, PA
Worked with Prof. **Onur Mutlu** on improving storage and memory reliability, published 10 academic papers in Proceedings of the IEEE, MICRO, HPCA, DSN, JSAC, MSST, etc.

### UNIVERSITY OF MICHIGAN | Research Assistant
May 2011 – May 2012 | Ann Arbor, MI
Worded with Prof. **Marios C. Papaefthymiou** and Prof. **Thomas F. Wenisch** on **Computational Sprinting** of manycore processors on mobile devices that improves the responsiveness of interactive applications by 10×. Worked with Prof. **Todd M. Austin** and Dr. **Joseph L. Greathouse** on architecture support for **Unlimited Watchpoints** that accelerates dynamic software analysis by 9×.

## AWARDS

2017 DFRWS EU Best Paper Award
2015 HPCA Best Paper Runner Up
2012 HPCA Best Paper Award

## SELECTED PUBLICATIONS

*(Full publication list is available on my website.)*

[1] Y. Cai, S. Ghose, E. F. Haratsch, Y. Luo, and O. Mutlu. Error Characterization, Mitigation, and Recovery in Flash-Memory-Based Solid-State Drives. *Proc. IEEE*, Sep. 2017.
[2] Y. Luo, S. Ghose, Y. Cai, E. F. Haratsch, and O. Mutlu. Enabling Accurate and Practical Online Flash Channel Modeling for Modern MLC NAND Flash Memory. *IEEE JSAC*, Sep. 2016.
[3] Y. Cai, Y. Luo, E. F. Haratsch, K. Mai, and O. Mutlu. Data Retention in MLC NAND Flash Memory: Characterization, Optimization, and Recovery. In *HPCA*, 2015.
[4] Y. Luo, Y. Cai, S. Ghose, J. Choi, and O. Mutlu. WARM: Improving NAND Flash Memory Lifetime With Write-Hotness Aware Retention Management. In *MSST*, 2015.
[5] Y. Luo, S. Govindan, B. Sharma, M. Santaniello, J. Meza, A. Kansal, J. Liu, B. Khessib, K. Vaid, and O. Mutlu. Characterizing Application Memory Error Vulnerability to Optimize Datacenter Cost via Heterogeneous-Reliability Memory. In *DSN*, 2014.
[6] A. Raghavan, Y. Luo, A. Chandawalla, M. Papaefthymiou, K. P. Pipe, T. F. Wenisch, and M. MK. Martin. Computational sprinting. In *HPCA*, 2012.