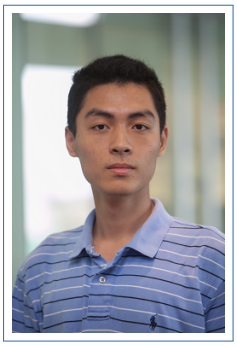
Yixin Luo

Curriculum Vitae

(734) 546 7629
camellyx@gmail.com
cs.cmu.edu/~yixinluo
Google Scholar: Yixin Luo
GitHub: github.com/camellyx
LinkedIn: linkedin.com/in/luoyixin



Education

2012.9–2018.3 **Ph.D. in Computer Science**, *Carnegie Mellon University*, Pittsburgh, PA.
PhD Thesis: "Architectural Techniques for Improving NAND Flash Memory Reliability", advised by Prof. **Onur Mutlu.**

2010.9–2012.5 **B.S. in Computer Engineering**, *University of Michigan*, Ann Arbor, MI.
GPA: 3.9/4.0. Dean's List 2010, 2011, EECS Scholar 2010.

2008.9–2012.8 **B.S. in Electrical and Computer Engineering**, *Shanghai Jiao Tong University*, China.
GPA: 3.8/4.0. Dean's List 2009.

Experience

2018.8–present **Software Engineer**, *Google Inc.*, Sunnyvale, CA.
Improving performance of storage and analytics frameworks, including columnar storage format, vectorized SQL expression library, and Flume.

2018.4–2018.8 **Postdoctoral Researcher in ECE**, *Carnegie Mellon University*, Pittsburgh, PA.
Worked with Dr. **Saugata Ghose** on developing new techniques for improving SSD storage system reliability.

2015.5–2015.8, 2016.5–2016.8 **Engineering Intern**, *Seagate Technology*, Lakeview, CA.
Worked with Dr. **Erich Haratsch** on developing new SSD controller algorithms for next-generation NAND flash memories.
Detailed achievements:
- Developed 10 new techniques and 4 new models to improve SSD lifetime by up to 12.9×
- Developed new tools to automatically test and analyze seven types of SSD errors
- Collected and analyzed 700 GB of real SSD error data using machine learning and statistical modeling techniques

2013.6–2013.8 **Research Intern**, *Microsoft Research*, Redmond, WA.
Worked with Dr. **Jie Liu** on developing new server architectures to tolerate memory errors in large-scale data centers.
Detailed achievements:
- Developed a new server architecture to reduce data center TCO by 2.7%
- Characterized memory error vulnerability of 3 important production data-intensive applications running in Microsoft data centers

Awards

2017 **DFRWS EU Best Paper Award**

2015 **HPCA Best Paper Runner Up**

2012 **HPCA Best Paper Award**

Publications

[1] Yixin Luo, Saugata Ghose, Yu Cai, Erich F. Haratsch, and Onur Mutlu. Improving 3D NAND Flash Memory Lifetime by Tolerating Early Retention Loss and Process Variation. In *SIGMETRICS*, 2018.

[2] Arash Tavakkol, Mohammad Sadrosadati, Saugata Ghose, Jeremie Kim, Yixin Luo, Yaohua Wang, Nika Mansouri Ghiasi, Lois Orosa, Juan G. Luna, and Onur Mutlu. FLIN: Enabling Fairness and Enhancing Performance in Modern NVMe Solid State Drives. In *ISCA*, 2018.

[3] Yixin Luo, Saugata Ghose, Yu Cai, Erich F. Haratsch, and Onur Mutlu. HeatWatch: Improving 3D NAND Flash Memory Device Reliability by Exploiting Self-Recovery and Temperature-Awareness. In *HPCA*, 2018.

[4] Yu Cai, Saugata Ghose, Erich F Haratsch, Yixin Luo, and Onur Mutlu. Error Characterization, Mitigation, and Recovery in Flash-Memory-Based Solid-State Drives. *Proc. IEEE*, Sep. 2017.

[5] Yu Cai, Saugata Ghose, Yixin Luo, Ken Mai, Onur Mutlu, and Erich F Haratsch. Vulnerabilities in MLC NAND Flash Memory Programming: Experimental Analysis, Exploits, and Mitigation Techniques. In *HPCA*, 2017.

[6] Aya Fukami, Saugata Ghose, Yixin Luo, Yu Cai, and Onur Mutlu. Improving the Reliability of Chip-Off Forensic Analysis of NAND Flash Memory Devices. In *DFRWS EU*, 2017. **Best Paper Award**.

[7] Yixin Luo, Saugata Ghose, Tianshi Li, Sriram Govindan, Bikash Sharma, Bryan Kelly, Amirali Boroumand, and Onur Mutlu. Using ECC DRAM to Adaptively Increase Memory Capacity. *arXiv preprint arXiv:1706.08870*, 2017.

[8] Yixin Luo, Saugata Ghose, Yu Cai, Erich F Haratsch, and Onur Mutlu. Enabling Accurate and Practical Online Flash Channel Modeling for Modern MLC NAND Flash Memory. *IEEE JSAC*, 34(9):2294–2311, 2016.

[9] Yu Cai, Yixin Luo, Erich F Haratsch, Ken Mai, and Onur Mutlu. Data Retention in MLC NAND Flash Memory: Characterization, Optimization, and Recovery. In *HPCA*, 2015. **Best Paper Runner Up**.

[10] Yu Cai, Yixin Luo, Saugata Ghose, and Onur Mutlu. Read Disturb Errors in MLC NAND Flash Memory: Characterization, Mitigation, and Recovery. In *DSN*, 2015.

[11] Yixin Luo, Yu Cai, Saugata Ghose, Jongmoo Choi, and Onur Mutlu. WARM: Improving NAND Flash Memory Lifetime With Write-Hotness Aware Retention Management. In *MSST*, 2015.

[12] Yixin Luo, Sriram Govindan, Bikash Sharma, Mark Santaniello, Justin Meza, Aman Kansal, Jie Liu, Badriddine Khessib, Kushagra Vaid, and Onur Mutlu. Characterizing Application Memory Error Vulnerability to Optimize Datacenter Cost via Heterogeneous-Reliability Memory. In *DSN*, 2014.

[13] Vivek Seshadri, Yoongu Kim, Chris Fallin, Donghyuk Lee, Rachata Ausavarungnirun, Gennady Pekhi-

menko, Yixin Luo, Onur Mutlu, Phillip B Gibbons, Michael A Kozuch, et al. RowClone: Fast and Energy-Efficient In-DRAM Bulk Data Copy and Initialization. In *MICRO*, 2013.

[14] Justin Meza, Yixin Luo, Samira Khan, Jishen Zhao, Yuan Xie, and Onur Mutlu. A Case for Efficient Hardware/Software Cooperative Management of Storage and Memory. In *WEED*, 2013.

[15] Arun Raghavan, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P Pipe, Thomas F Wenisch, and Milo MK Martin. Designing for Responsiveness with Computational Sprinting. *IEEE Micro*, 33(3): 8–15, 2013.

[16] Joseph L Greathouse, Hongyi Xin, Yixin Luo, and Todd Austin. A Case for Unlimited Watchpoints. In *ASPLOS*, 2012.

[17] Arun Raghavan, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P Pipe, Thomas F Wenisch, and Milo MK Martin. Computational Sprinting. In *HPCA*, 2012. **Best Paper Award**.

Conference Talks

- **Architectural Techniques for Improving NAND Flash Memory Reliability**,
  Thesis Defense: CMU 2018,
  Job Talk: Alibaba, Baidu, Seagate, 2018,
  Seminar: Tsinghua University, CAS-ICT, SJTU, Kyushu University, NTU Taipei, NCTU, TSMC, City University of Hong Kong, Seoul National University, KAIST, Microsoft Research, 2018.
- **Improving 3D NAND Flash Memory Lifetime by Tolerating Early Retention Loss and Process Variation**, Sigmetrics 2018, PDL Retreat 2017.
- **HeatWatch: Improving 3D NAND Flash Memory Device Reliability by Exploiting Self-Recovery and Temperature Awareness**, HPCA 2018, PDL Retreat 2017. (Lightning session talk on YouTube: https://youtu.be/7ZpGozzEVpY)
- **Improving SSD Lifetime with Access Pattern and Flash Device Awareness**, Google PhD Summit 2017.
- **Online Flash Channel Modeling and Its Applications**, Flash Memory Summit, PDL Retreat, 2016.
- **Data Retention in MLC NAND Flash Memory**, Flash Memory Summit, PDL Retreat, CMU SCS Student Seminar Series, 2015.
- **WARM: Write-hotness Aware Retention Management**, MSST 2015.
- **Read Disturb Errors in MLC NAND Flash Memory**, DSN, PDL Retreat, 2015.
- **Data Retention in MLC NAND Flash Memory *(Best paper session)***, HPCA, PDL Retreat, CALCM Seminar, 2015.
- **Optimizing Data Center Cost via Heterogeneous Reliability Memory**, DSN, PDL Retreat, 2014.

Projects

Research Projects

2017.1–2018.3 **Peloton: A Self-Driving In-Memory Database**, *Open Source Project*.
Led a team of three graduate students to design and develop the database catalog for Peloton to support non-blocking schema change and to implement a concurrent lock-free skiplist index. This project is advised by Prof. **Andy Pavlo**.

2014.1–2018.7 **Architectural Techniques to Improve NAND Flash Memory Reliability**.
Started as an internship project at Seagate to improve the reliability of NAND flash memory-based SSD at low cost. Led to my PhD dissertation.
Detailed achievements:
- Published 4 first-authored papers and 6 co-authored papers, one of which won DFRWS EU best paper award, another won HPCA best paper runner up award
- Developed 10 new techniques to improve SSD lifetime by up to 12.9×
- Experimentally characterized state-of-the-art NAND flash memory chips
- Developed 4 new analytical models to accurately estimate SSD reliability

2013.6–2018.7 **Heterogeneous Reliability Memory**.
Started as an internship project at Microsoft Research to optimize data center TCO and memory reliability. Closely related to my PhD dissertation.
Detailed achievements:
- Published 2 first-authored papers
- Developed a new server architecture to reduce data center TCO by 2.7%
- Developed a new mechanism that dynamically adjusts memory capacity and reliability

2013 **Single-Level Storage**.
Characterized the performance, energy, and scalability benefit of a single-level storage system compared to a traditional two-level storage system through architectural simulations.

2011.5–2012.3 **A Case for Unlimited Watchpoints**, *Undergraduate Research Project*.
Worked with Prof. **Todd M. Austin** and Dr. **Joseph L. Greathouse** on architecture support for **Unlimited Watchpoints** that accelerates dynamic software analysis by 9×.
Detailed achievements:
- Developed a simulation framework for range cache using C++
- Performed architectural simulations to show the performance benefits of the proposed range cache design

2011.9–2012.2 **Computational Sprinting**, *Undergraduate Research Project*.
Worked with Prof. **Marios C. Papaefthymiou** and Prof. **Thomas F. Wenisch** on **Computational Sprinting** of manycore processors on mobile devices that improves the responsiveness of interactive applications by 10×.
Detailed achievements:
- Developed a SPICE power model for power gating many-core processors
- Developed a new technique to reduce the performance overhead for power gating
- Performed SPICE circuit simulations to show the performance benefit of Computational Sprinting

Academic Projects

2017.12 **Multi-Agent Deep Reinforcement Learning**, *Course Project*.
Developed DQN, DDPG, and MADDPG models for continuous multi-agent environment.

2017.4 **Symbolic Information Processing for Question Answering**, *Course Project*.
Developed an RNN model to answer questions regarding a natural language context.

2014.12 **Deep Learning with Noise**, *Course Project*.
Characterized the effect of different types of noise on different components of a neural network.

2014.5 **Compiler Support for Hardware Compression**, *Course Project*.
Developed data splitting and memory pooling compiler optimizations for cache compression algorithms.

2011.5 **CPU Architecture Design**, *Undergraduate Major Design Project*.
Led a team of three undergraduate students on designing and implementing an 150 MHz out-of-order processor using Verilog.

2011.12 **CPU Layout Design**, *Undergraduate Major Design Project*.
Led a team of five graduate and undergraduate students on designing the circuit layout for a 5-stage pipelined in-order processor and a 3-transistor eDRAM cache.

Teaching Experience

2014.8–2012.12 **Teaching Assistant**, *Carnegie Mellon University*, Pittsburgh, PA.
CMU 18–742 — **Parallel Computer Architecture**, taught by Prof. **Onur Mutlu**.
Responsibilities include holding office hours, mentoring research projects.

2014.1–2014.5 **Teaching Assistant**, *Carnegie Mellon University*, Pittsburgh, PA.
CMU 15–418/15–618 — **Parallel Computer Architecture and Programming**, taught by Prof. **Kayvon Fatahalian**.
Responsibilities include holding office hours, mentoring projects, preparing and grading homework.

Selected Coursework

Graduate

CMU 15–721 Advanced Database Systems
CMU 15–712 Advanced Operating Systems and Distributed Systems
CMU 15–719 Advanced Cloud Computing
CMU 15–744 Computer Networks
CMU 15–745 Advanced Optimizing Compilers
CMU 15–740 Computer Architecture
CMU 15–750 Graduate Algorithms
CMU 10–701 Machine Learning
CMU 10–707 Deep Learning
CMU 10–703 Deep Reinforcement Learning

Undergraduate

UM EECS570 Computer Architecture + Major Design Project
UM EECS427 VLSI Design + Major Design Project
UM EECS470 Microprocessor-Based Systems
UM EECS482 Operating Systems
UM EECS484 Database Management Systems
UM EECS492 Artificial Intelligence
SJTU Honors Mathematics

Programming Skills

Advanced	C++, Python, Matlab, Shell, Verilog, LaTeX
Intermediate	Perl, HTML, Windows Batch, TensorFlow, PyTorch
Tools	Intel Pin, HSPICE, Cadence tools, gem5, Multi2Sim, MySQL/PostgreSQL

Interests

- Basketball
- Hiking
- Ping Pong
- Traveling