Yixin Luo

Curriculum Vitae

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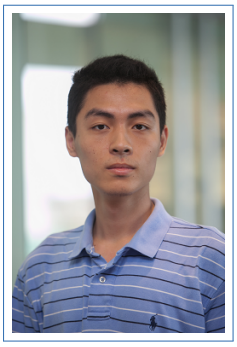

Education

2012–2017 **Ph.D of Computer Science**, *Carnegie Mellon University*, Pittsburgh, PA.
PhD Thesis (in progress): "Architectural Techniques for Improving NAND Flash Memory Reliability", advised by Prof. **Onur Mutlu.**

2010–2012 **Bachelor of Computer Engineering**, *University of Michigan*, Ann Arbor, MI.
GPA: 3.9/4.0. Dean's List 2010, 2011, EECS Scholar 2010.

2008–2012 **Bachelor of Electrical Engineering**, *Shanghai Jiao Tong University*, Shanghai, China.
GPA: 3.8/4.0. Dean's List 2009.

Experience

2015, 2016 **Engineering Intern**, *Seagate Technology*, Lakeview, CA.
Worked with Dr. **Erich Haratsch** on developing new SSD controller algorithms for next-generation NAND flash memories.
Detailed achievements:
- Developed 10 new techniques and 4 new models to improve SSD lifetime by up to 12.9×
- Developed new tools to automatically test and analyze seven types of SSD errors
- Collected and analyzed 700 GB of real SSD error data using machine learning and statistical modeling techniques

2013 **Research Intern**, *Microsoft Research*, Redmond, WA.
Worked with Dr. **Jie Liu** on developing new server architectures to tolerate memory errors in large-scale data centers.
Detailed achievements:
- Developed a new server architecture to reduce data center TCO by 2.7%
- Characterized memory error vulnerability of 3 important production data-intensive applications running in Microsoft data centers

Awards

2017 DFRWS EU Best Paper Award
2015 HPCA Best Paper Runner Up
2012 HPCA Best Paper Award

Conference Talks

2016 **Online Flash Channel Modeling and Its Applications** *Flash Memory Summit*
2015 **Data Retention in MLC NAND Flash Memory** *Flash Memory Summit*
2015 **WARM: Write-hotnes Aware Retention Management** *MSST*
2015 **Read Disturb Errors in MLC NAND Flash Memory** *DSN*
2015 **Data Retention in MLC NAND Flash Memory** *HPCA* ***(Best paper session)***
2014 **Optimizing Data Center Cost via Heterogeneous Reliability Memory** *DSN*

Publications

[1] Yu Cai, Saugata Ghose, Erich F Haratsch, Yixin Luo, and Onur Mutlu. Error Characterization, Mitigation, and Recovery in Flash-Memory-Based Solid-State Drives. *Proc. IEEE*, Sep. 2017.

[2] Yu Cai, Saugata Ghose, Yixin Luo, Ken Mai, Onur Mutlu, and Erich F Haratsch. Vulnerabilities in MLC NAND flash memory programming: experimental analysis, exploits, and mitigation techniques. In *HPCA*, 2017.

[3] Aya Fukami, Saugata Ghose, Yixin Luo, Yu Cai, and Onur Mutlu. Improving the reliability of chip-off forensic analysis of NAND flash memory devices. In *DFRWS EU*, 2017.

[4] Yixin Luo, Saugata Ghose, Tianshi Li, Sriram Govindan, Bikash Sharma, Bryan Kelly, Amirali Boroumand, and Onur Mutlu. Using ECC DRAM to adaptively increase memory capacity. *arXiv preprint arXiv:1706.08870*, 2017.

[5] Yixin Luo, Saugata Ghose, Yu Cai, Erich F Haratsch, and Onur Mutlu. Enabling Accurate and Practical Online Flash Channel Modeling for Modern MLC NAND Flash Memory. *IEEE JSAC*, 34(9):2294–2311, 2016.

[6] Yu Cai, Yixin Luo, Erich F Haratsch, Ken Mai, and Onur Mutlu. Data Retention in MLC NAND Flash Memory: Characterization, Optimization, and Recovery. In *HPCA*, 2015.

[7] Yu Cai, Yixin Luo, Saugata Ghose, and Onur Mutlu. Read disturb errors in mlc nand flash memory: Characterization, mitigation, and recovery. In *DSN*, 2015.

[8] Yixin Luo, Yu Cai, Saugata Ghose, Jongmoo Choi, and Onur Mutlu. WARM: Improving NAND Flash Memory Lifetime With Write-Hotness Aware Retention Management. In *MSST*, 2015.

[9] Yixin Luo, Sriram Govindan, Bikash Sharma, Mark Santaniello, Justin Meza, Aman Kansal, Jie Liu, Badriddine Khessib, Kushagra Vaid, and Onur Mutlu. Characterizing Application Memory Error Vulnerability to Optimize Datacenter Cost via Heterogeneous-Reliability Memory. In *DSN*, 2014.

[10] Vivek Seshadri, Yoongu Kim, Chris Fallin, Donghyuk Lee, Rachata Ausavarungnirun, Gennady Pekhimenko, Yixin Luo, Onur Mutlu, Phillip B Gibbons, Michael A Kozuch, et al. RowClone: Fast and energy-efficient in-DRAM bulk data copy and initialization. In *MICRO*, 2013.

[11] Justin Meza, Yixin Luo, Samira Khan, Jishen Zhao, Yuan Xie, and Onur Mutlu. A case for efficient hardware/software cooperative management of storage and memory. In *WEED*, 2013.

[12] Arun Raghavan, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P Pipe, Thomas F Wenisch,

and Milo MK Martin. Designing for responsiveness with computational sprinting. *IEEE Micro*, 33(3): 8–15, 2013.

[13] Joseph L Greathouse, Hongyi Xin, Yixin Luo, and Todd Austin. A case for unlimited watchpoints. In *ASPLOS*, 2012.

[14] Arun Raghavan, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P Pipe, Thomas F Wenisch, and Milo MK Martin. Computational sprinting. In *HPCA*, 2012.

Teaching Experience

2014 **Teaching Assistant**, *Carnegie Mellon University*, Pittsburgh, PA.
CMU 18–742 — **Parallel Computer Architecture**, taught by Prof. **Onur Mutlu**.
Responsibilities include holding office hours, mentoring research projects.

2014 **Teaching Assistant**, *Carnegie Mellon University*, Pittsburgh, PA.
CMU 15–418/15–618 — **Parallel Computer Architecture and Programming**, taught by Prof. **Kayvon Fatahalian**.
Responsibilities include holding office hours, mentoring projects, preparing and grading homeworks.

Projects

Research Projects

2011–2012 **A Case for Unlimited Watchpoints**, *Undergraduate Research Project*.
Worked with Prof. **Todd M. Austin** and Dr. **Joseph L. Greathouse** on architecture support for **Unlimited Watchpoints** that accelerates dynamic software analysis by 9×.
Detailed achievements:
- Developed a simulation framework for range cache using C++.
- Performed architectural simulations to show the performance benefits of the proposed range cache design.

2011–2012 **Computational Sprinting**, *Undergraduate Research Project*.
Worked with Prof. **Marios C. Papaefthymiou** and Prof. **Thomas F. Wenisch** on **Computational Sprinting** of manycore processors on mobile devices that improves the responsiveness of interactive applications by 10×.
Detailed achievements:
- Developed a SPICE power model for power gating many-core processors.
- Developed a new technique to reduce the performance overhead for power gating.
- Performed SPICE circuit simulations to show the performance benefit of Computational Sprinting.

Academic Projects

2017 **Peloton: A Self-Driving In-Memory Database**, *Open Source Project*.
Leaded a team of three graduate students to design and implement the database catalog for Peloton to support non-blocking DDL operations and to implement a concurrent lock-free skiplist index. This project is advised by Prof. **Andy Pavlo**.

2011 **CPU Architecture Design**, *Undergraduate Major Design Project*.
Leaded a team of three undergraduate students on designing and implementing an 150 MHz out-of-order processor using Verilog.

2011 **CPU Layout Design**, *Undergraduate Major Design Project*.
Leaded a team of five graduate and undergraduate students on designing the circuit layout for a 5-stage pipelined in-order processor and a 3-transistor eDRAM cache.

Selected Coursework

Graduate

CMU 10–707	Deep Learning
CMU 15–721	Advanced Database Systems
CMU 10–703	Deep Reinforcement Learning
CMU 10–701	Machine Learning
CMU 15–745	Advanced Optimizing Compilers
CMU 15–712	Advanced Operating Systems and Distributed Systems
CMU 15–719	Advanced Cloud Computing
CMU 15–750	Graduate Algorithms
CMU 15–740	Computer Architecture
CMU 15–744	Computer Networks

Undergraduate

UM EECS570	Computer Architecture + Major Design Project
UM EECS427	VLSI Design + Major Design Project
UM EECS470	Microprocessor-Based Systems
UM EECS482	Operating Systems
UM EECS484	Database Management Systems
UM EECS492	Artificial Intelligence
SJTU	Honors Mathematics

Programming Skills

Advanced	C++, Python, Matlab, Shell, Verilog, LaTeX
Intermediate	Perl, HTML, Windows Batch, TensorFlow, PyTorch
Tools	Intel Pin, HSPICE, Cadence tools, gem5, Multi2Sim, MySQL/PostgreSQL

Interests

- Basketball
- Hiking
- Ping Pong
- Traveling