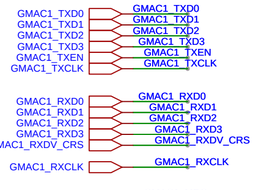
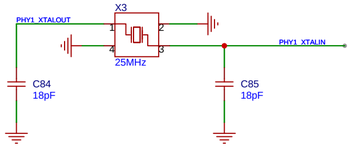
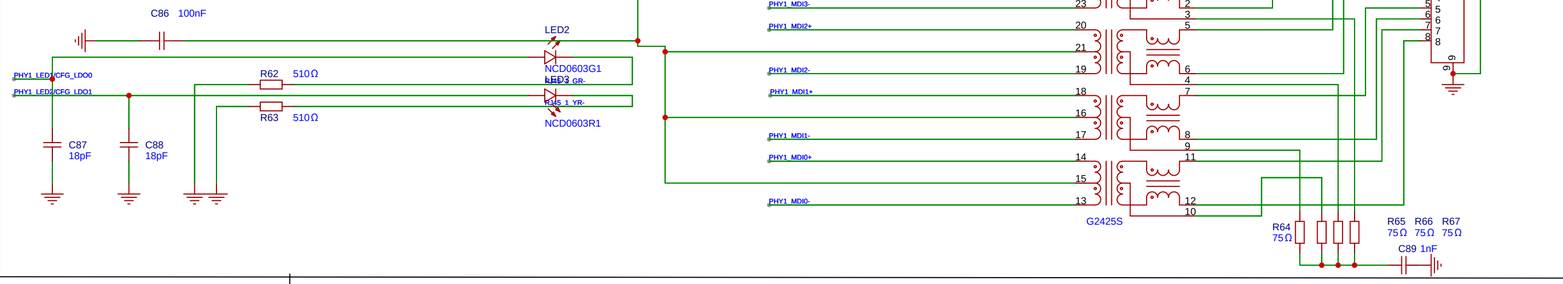
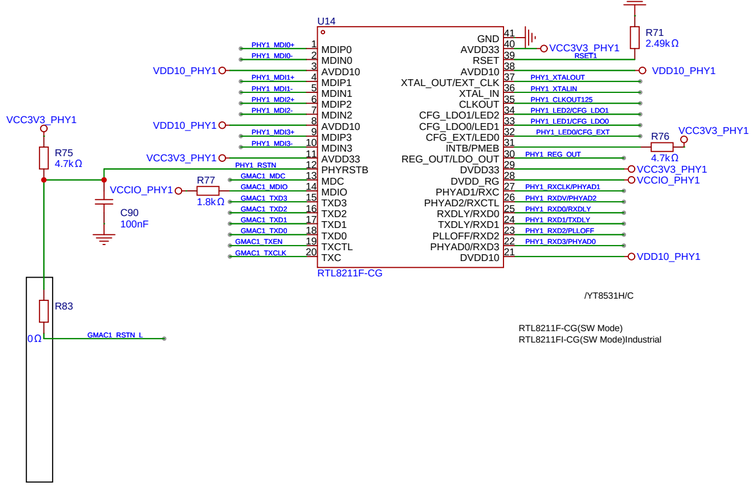
RGMII

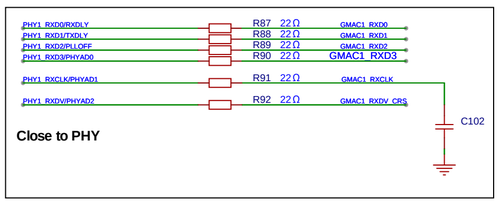




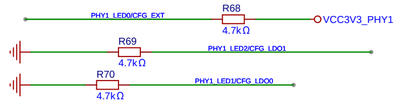


网口

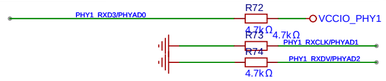




RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	



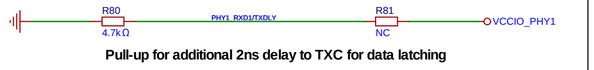
VCC_PHY0_IO Voltage Config



PHY Address Config

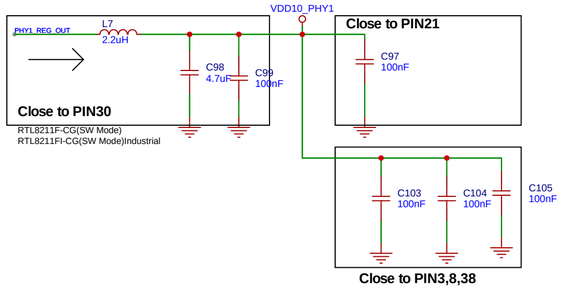
PHY Address	PHYAD[2:0]
1 (default)	3'b001

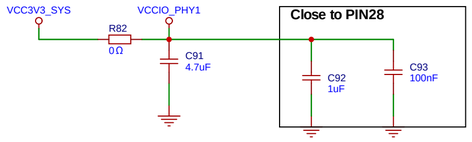
Pull-up for additional 2ns delay to RXC for data latching

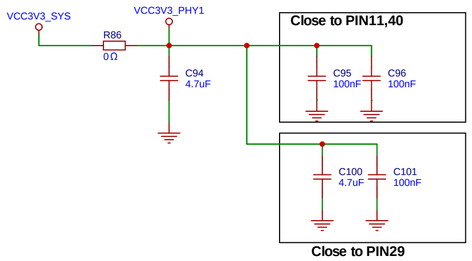


Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)







原理图	Schematic2	更新日期	2024-07-28
		创建日期	2024-06-20
图页	P3	物料编码	
绘制		CABLE_TEST	
审阅			
		版本	尺寸
		V1.0	A4
		页 3 共 4	
		嘉立创EDA	