I2C Control Register

Bit 31 (w)	Bits 25 to 19 (w)	Bits 15 to 10 (w)	Bit 3 (w)	Bit 2 (w)	Bit 1 (w)	Bit 0 (w)
Rw	Chip ID	Data Size	Read ACK	Data Load	Clear wr FIFO	Execute I2C Operation
0 – write 1 – read	**7-bit device address**	**Size of i2c data field to transmit/receive or load into write FIFO from data register**	**Acknowledge the previous data read, and load the next Data Size from the read FIFO into the data register**	**Load data from the data register into the i2c write FIFO**	**Clear the i2c write FIFO in the case of a canceled operation**	**Set to 1 along with other fields in register write to execute the i2c operation with data loaded in write FIFO**

Control register to be used alongside data and status registers. Any data that needs to be sent out along with the i2c operation should be loaded into the data FIFO before executing the i2c operation. Can check the status register to determine whether the operation was successful or not.

I2C Data Register

Bits 31 to 0 (r/w)
Data
When "Data Load" is set, the "Data Size" lowest bits from this register are loaded into the i2c write FIFO. The most significant bit is the first one to get transmitted over i2c. During a read operation, "Data Size" bits are read into this register after a successful read. Use the Read ACK bit from control register to load the next section of data from the read FIFO.

Data register interacts with internal I2C read and write FIFOs. Can be used in conjunction with the control register to read data from the read FIFO, and write data to the write FIFO.

I2C Status Register

Bit 3 (r/w)	Bit 2 (r/w)	Bit 1 (r)	Bit 0 (r)
Read FIFO overflow	Write FIFO overflow	NACK	Ready
Stick bit, must be cleared to 0 to reset. If a read overflow is detected, will get set to 1.	**Sticky bit, must be cleared to 0 to reset. If a write overflow is detected, will get set to 1.**	**0 => Previous operation was successful 1 => Previous operation resulted in a NACK**	**0 => Controller is busy with previous operation 1 => Controller is ready to start a new operation**

Status register to monitor the status of previous operations, and to determine when the i2c controller is ready to start a new operation.