CprE 381 – Computer Organization and Assembly-Level Programming

Proj-C Report

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Section / Lab Time __ Section 6 / Th: 6:10pm – 8:00pm ___

Submit a typeset pdf version of this on Canvas by the due date. Refer to the highlighted language in the Proj-C instructions for the context of the following questions.

a. [Part 0] Come up with a global list of the datapath values and control signals that are required during each pipeline stage.

   All of the control signals that were used in the Single Cycle CPU will be required during each pipeline stage. To refrain from listing them all we will instead recognize that we will need to be able track all of the control signals that we have coming from our control unit.
   Other datapath values that will be needed for control purposes is four more signals for the state registers control values in order to correctly operate the pipeline stage.

b. [Part 1 (a)] Draw a simple schematic showing how you could implement stalling and flushing operations given an ideal N-bit register.

c. [Part 1 (b)] Show that values that are stored in the initial IF/ID register are available as expected four cycles later, and that new values can be inserted into the pipeline every single cycle. *[Please include waveforms and explanations.]*

d. [Part 2] In your writeup, provide your schematic for this part, describe what challenges (if any) you faced in implementing this module.

e. [Part 3 (a)] In your writeup, show the ModelSim output for the individual instruction tests, and provide a discussion of result correctness. It may be helpful to also annotate the waveforms directly.

f. [Part 3 (b)] In your writeup, show the ModelSim output for the modified Bubblesort test, and provide a discussion of result correctness. It may be helpful to also annotate the waveforms directly.

g. [Part 4] Report the maximum frequency your software-scheduled pipelined processor can run at and determine what your critical path is (specify each module/entity/component that this path goes through).

h. [Part 5 (a)] Of the MIPS instructions supported for Project Part B, list which instructions produce values, and what signals in the pipeline these correspond to.

i. [Part 5 (b)] List which of these same instructions consume values, and what signals in the pipeline these correspond to.

j. [Part 5 (c)] Come up with a generalized list of potential data dependencies. From this generalized list, select those dependencies that will require forwarding (write down the corresponding pipeline stages that will be forwarding and receiving the data), and those dependencies that will require hazard stalls.

k. [Part 6] Write a more generalized series of data forwarding and hazard detection logic equations based on the result from part 5).

l. [Part 7] Provide a high-level schematic drawing of the interconnection between components for the MIPS Hardware-scheduled pipelined Processor.

m. [Part 8 (a)] In your writeup, show the ModelSim output for the individual instruction tests and Bubblesort test (the original from Project Part B), and provide a discussion of result correctness. It may be helpful to also annotate the waveforms directly.

n. [Part 8 (b)] In your writeup, show the ModelSim output an application that attempts to exhaustively test the forwarding and detection logic in your pipeline, and provide a discussion of result correctness. It may be helpful to also annotate the waveforms directly.

o. [Part 10] Report the maximum frequency your processor can run at and determine what your critical path is. Draw this critical path on top of your top-level schematic. In your writeup, briefly discuss your critical path results. What components would you focus on to improve the frequency?

p. [Feedback] You must complete this section for your lab to be graded. Please complete each column **separately** for each team member; I expect it to take roughly 10 minutes (do not take more than 20 minutes).

    i. How many hours did you spend on this lab?

Task	**During lab time**			**Outside of lab time**		
Team Initials						
Reading lab						
Pencil/paper design						
VHDL design						
Assembly coding						
Simulation						
Debugging						
Report writing						
Other:						
Total						

    ii. If you could change one thing about the lab experience, what would it be? Why?

    iii. What was the most interesting part of the lab?