Class Report 2: Block Memory

Cameron Anderson

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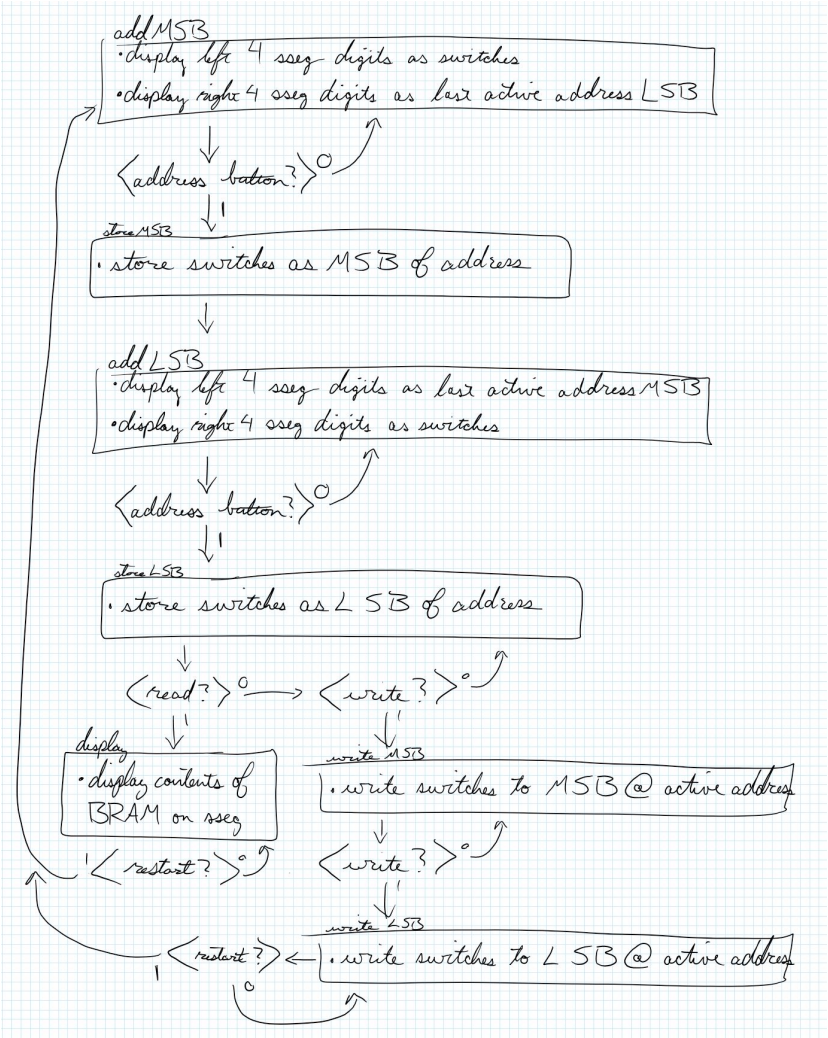
1 Introduction

The goal of this project was to use the seven-segment display and binary switches to read and write to and from the block memory within the Nexys 4 DDR prototyping board. For this project, the data and address registers are each 32 bits. The seven-segment display has 8 digits and can display the full range of hexidecimal digits at each of the 8 locations. With only 16 switches, the registers will need to be divided into MSB and LSB registers to read in the switches.

2 Experimental Plan

Figure 1 on page 2 shows the top level state machine that was used to transition between collecting the address and reading and writing to and from Block RAM. Because the registers were each 32 bits and there were only 16 switches, collecting the values through the switches had to be broken up into MSB and LSB states. This did not, however, affect the read from the BRAM because the seven segment display was able to read 8 hexidecimal digits equalling a total of 32 binary bits. The state machine transitions were completed by four buttons on the Nexys 4 DDR board. The buttons were arranged nicely in the order of the state machine. The top button was used to set first the MSB of the address and then the LSB of the address. On the next row down, the outside buttons were used to transition to the next state. The left button on the middle row was used to select the read function to display the BRAM's contents at the previously selected address. The right button on the middle row was used to select the write function. This button was used twice in succession after changing the switches to match the MSB 2 bytes of what was to be written to the previously selected address first and then similarly the LSB 2 bytes of the data. In addition to the state machine, Chu provided a module for displaying hexidecimal digits to the seven segment display but only the rightmost 4 digits. This was altered for this project to include all 8 digits of the seven segment display to read all 32 bits from an address in BRAM.

Figure 1: State Machine for using Block Memory



3 Analysis

4 Conclusion