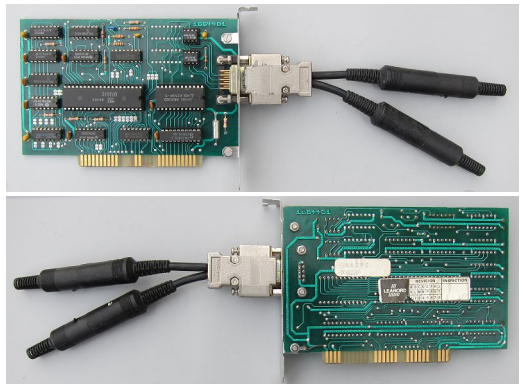

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XTBus

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alim

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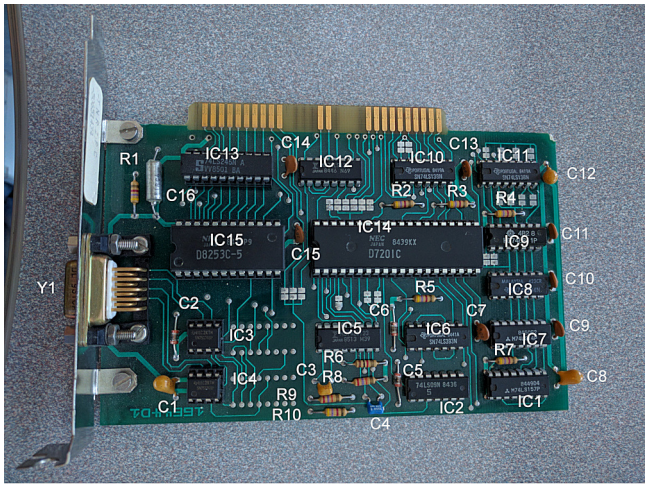

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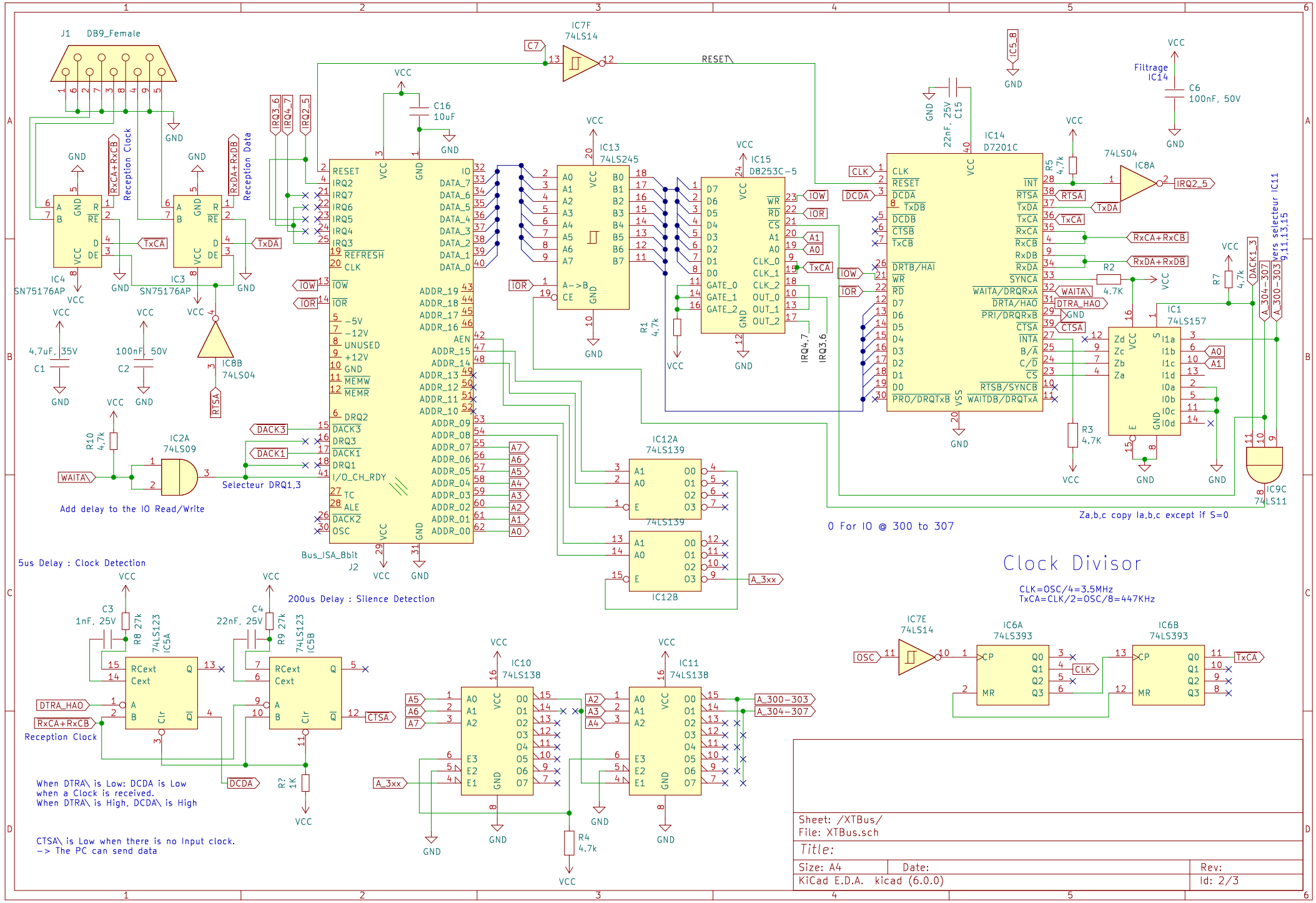
J1 DB9_Female
IC7F 74LS14
C7
RESET\
VCC
GND
C16 10uF
IC13 74LS245
IC15 D8253C-5
IC14 D7201C
C15 22nF, 25V
IC5_8
Filtrage IC14
C6 100nF, 50V
74LS04
IC8A
IRQ2_5
TxDA
RTSA
TxCA
RxCA+RxCB
RxDA+RxDB
R5 4.7k
R2 4.7K
R3 4.7K
R1 4,7k
R7 4.7k
WAITA
DTRA_HAO
CTSA
IC4 SN75176AP
IC3 SN75176AP
RxCA+RxCB Reception Clock
RxDA+RxDB Reception Data
IC8B 74LS04
C1 4,7uF, 35V
C2 100nF, 50V
IC2A 74LS09
R10 4,7k
Selecteur DRQ1,3
Add delay to the IO Read/Write
Bus_ISA_8bit J2
IRQ3_6
IRQ4_7
IRQ2_5
DACK3
DACK1
IOW
IOR
AEN
IC12A 74LS139
IC12B 74LS139
A_3xx
IRQ4.7
IRQ3.6
IC1 74LS157
A_304-307
A_300-303
IC9C 74LS11
Za,b,c copy Ia,b,c except if S=0
0 For IO @ 300 to 5
0 For IO @ 300 to 307
Clock Divisor
CLK=OSC/4=3.5MHz
TxCA=CLK/2=OSC/8=447KHz
IC7E 74LS14
IC6A 74LS393
IC6B 74LS393
5us Delay : Clock Detection
200us Delay : Silence Detection
C3 1nF, 25V
C4 22nF, 25V
R8 27k
R9 27k
74LS123 IC5A
74LS123 IC5B
DTRA_HAO
RxCA+RxCB
Reception Clock
DCDA
R? 1K
When DTRA\ is Low: DCDA is Low
when a Clock is received.
When DTRA\ is High, DCDA\ is High
CTSA\ is Low when there is no Input clock.
-> The PC can send data
IC10 74LS138
IC11 74LS138
R4 4.7k
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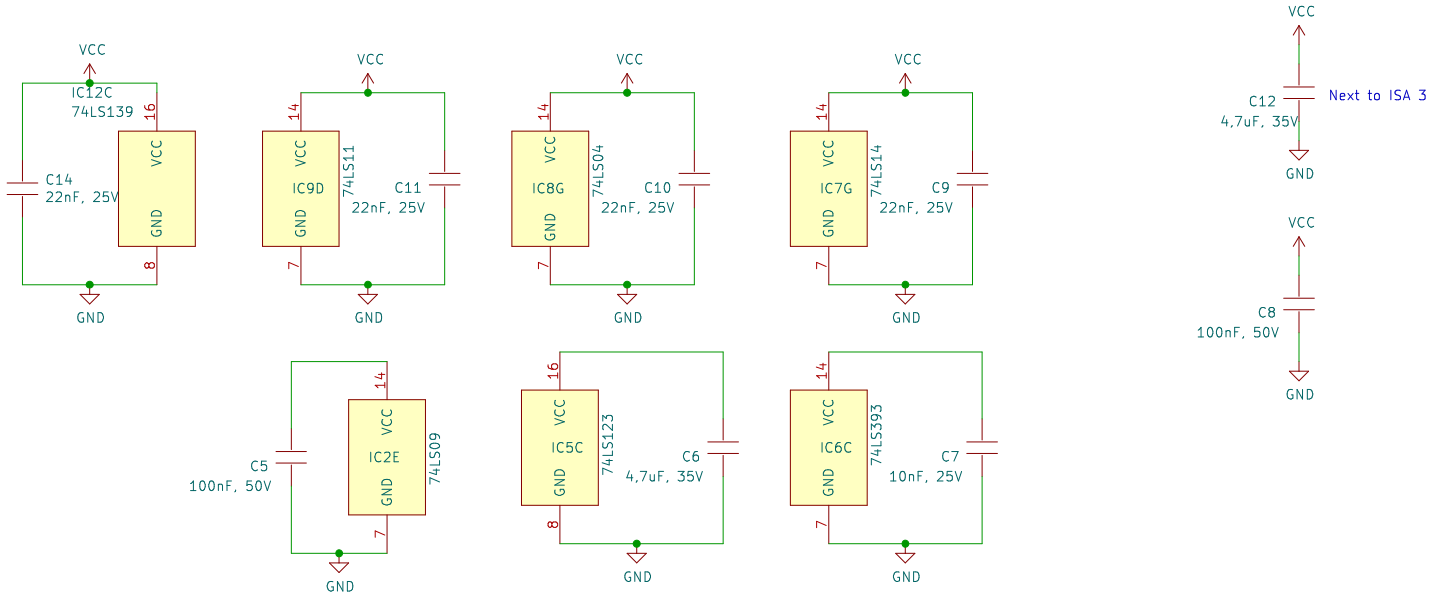

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