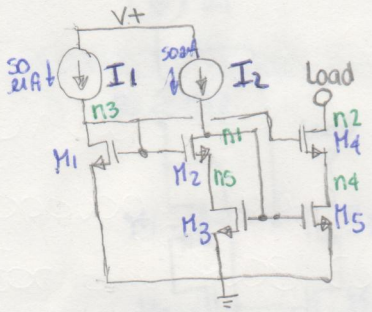
Quick hand DC analysis of Lab 3.11 circuits (just for fun.)

① Widely used mirror (@ 3V load)



node voltages (@ 1V)

$n_1 = 1.1692V$ $n_2 = 1.0V$ $n_3 = 1.1786V$ $n_4 = .4162V$ $n_5 = 0.4166$

currents (Branch)

$I_1 = 50\mu A$ $I_2 = 50\mu A$ $I_{out} = 49.9838\ \mu A$

Mosfet Operating points (@ 3V) more representative than @ 1V.

M_1: $\frac{W}{L} = \frac{4u}{2u}$ $V_{gs} = 1.1786V$ $V_{ds} = 1.1786$ $V_{th} = 0.5678V$

$V_{gs} - V_{th} = 0.6108V$ $V_{ds} > 0.6108 \rightarrow$ SAT

M_2: $\frac{W}{L} = \frac{100u}{2u}$ $V_{gs} = 0.7619V$ $V_{ds} = 0.7526V$ $V_{th} = 0.6816V$

$V_{gs} - V_{th} = 0.0803V$ $V_{ds} > 0.0803 \rightarrow$ SAT

(right at threshold)

M_3: $\frac{W}{L} = \frac{10u}{5u}$ $V_{gs} = 1.1692V$ $V_{ds} = 0.4166V$ $V_{th} = 0.5479V$

$V_{gs} - V_{th} = 0.6213$ $V_{ds} < 0.6213 \rightarrow$ Linear (non sat)

M_4: $\frac{W}{L} = \frac{100u}{2u}$ $V_{gs} = 0.7579V$ $V_{ds} = 2.5793V$ $V_{th} = 0.6824V$

Thus channel resistance and large voltage drop.

$V_{gs} - V_{th} = 0.0755V$ $V_{ds} \gg 0.0755 \rightarrow$ SAT → important for low current dependence on drain voltage

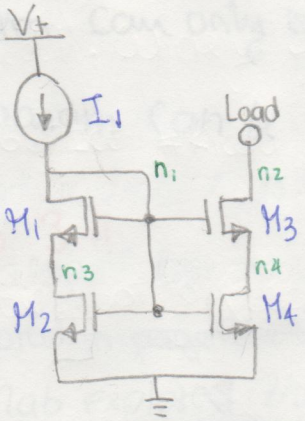
(right at threshold)

M_5: $\frac{W}{L} = \frac{10u}{5u}$ $V_{gs} = 1.1692$ $V_{ds} = 0.4207$ $V_{th} = 0.5479V$

$V_{gs} - V_{th} = 0.6213$ $V_{ds} < 0.6213 \rightarrow$ Linear (non sat) → This is ok as M_4 is our shield in saturation.

* Keep in mind that V_{sb} (source to bulk voltage) also modulates V_{th} for M_2 and M_4.

② Fewer Devices, Same Performance.



Mosfet Operating Points (@ 3V)

M1: $\frac{W}{L} = \frac{100u}{2u}$ $V_{gs} = 0.7603V$ $V_{ds} = 0.7603V$ $V_{th} = 0.6799V$

$V_{gs} - V_{th} = 0.0804V$ $V_{ds} > 0.0804V$ → Sat

M2: $\frac{W}{L} = \frac{10u}{5u}$ $V_{gs} = 1.1711V$ $V_{ds} = 0.4108V$ $V_{th} = 0.5479V$

$V_{gs} - V_{th} = 0.6232V$ $V_{ds} < 0.6232$ → Linear region

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M3: $\frac{W}{L} = \frac{100u}{2u}$ $V_{gs} = 0.7563V$ $V_{ds} = 2.58523$ $V_{th} = 0.6807V$

$V_{gs} - V_{th} = 0.0756V$ $V_{ds} >> 0.0756$ → SAT

Thus some channel resistance and large Vdrop.

right ab threshold

important for low current dependence on Voltage

M4: $\frac{W}{L} = \frac{10u}{5u}$ $V_{gs} = 1.1711V$ $V_{ds} = 0.4148V$ $V_{th} = 0.5479V$

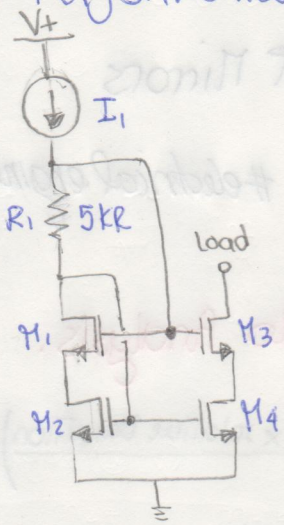
$V_{gs} - V_{th} = 0.6232V$ $V_{ds} < 0.6232$ → Linear region

→ This is ok as long as M3 is deep into Saturation

From looking at the operating points of circuits ① and ② we can see that their operating conditions are quite similar and thus the comparable performance.

* keep in mind that the threshold voltage for M1 and M3 is also dependent on the bulk to source voltage (V_{sb}).

③ Best Performance.



MOSFET Operating Points (@ 3V.)

M1: $\frac{W}{L} = \frac{100u}{2u}$ $V_{gs} = 0.7683V$ $V_{ds} = 0.5183V$ $V_{th} = 0.6873V$

$V_{gs} - V_{th} = 0.081V$ $V_{ds} > 0.081V \rightarrow$ SAT

M2: $\frac{W}{L} = \frac{20u}{5u}$ $V_{gs} = 0.9555V$ $V_{ds} = 0.4371V$ $V_{th} = 0.5440V$

$V_{gs} - V_{th} = 0.4115V$ $V_{ds} >_{\text{slightly}} 0.411S \rightarrow$ SAT ✓

M3: $\frac{W}{L} = \frac{100u}{2u}$ $V_{gs} = 0.7636V$ $V_{ds} = 2.5581V$ $V_{th} = 0.6882V$

$V_{gs} - V_{th} = 0.0754V$ $V_{ds} >> 0.0754V \rightarrow$ SAT (deep)

→ we have to keep in saturation, this is our cascode shield

M4: $\frac{W}{L} = \frac{20u}{5u}$ $V_{gs} = 0.9555V$ $V_{ds} = 0.4419V$ $V_{th} = 0.5440V$

$V_{gs} - V_{th} = 0.4115V$ $V_{ds} > 0.411S \rightarrow$ SAT

→ This device in saturation gives us even less dependence on load voltage.

Ah as we thought to really be able to reduce ~~to~~ the ~~voltage~~ current dependence on load voltage we have to try to keep the output stage devices in Saturation (not just the cascode transistor M3 which must be in deep saturation) and we have to do this while being mindful of the compliance voltage (keeping V_{th} for M_2 and M_4 low as we have more control over this: V_{GS}=0).

This topology is quite outstanding all output devices in Saturation while managing to keep V_{ds} low for M_2 & M_4!