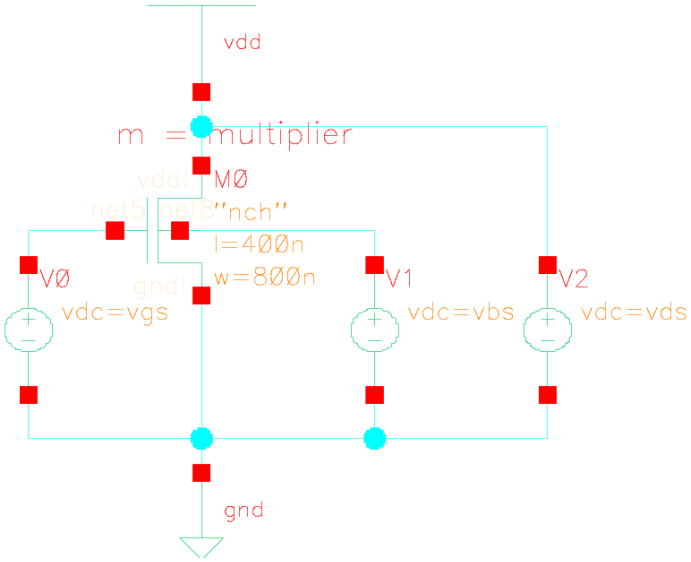
Device and circuit characterization

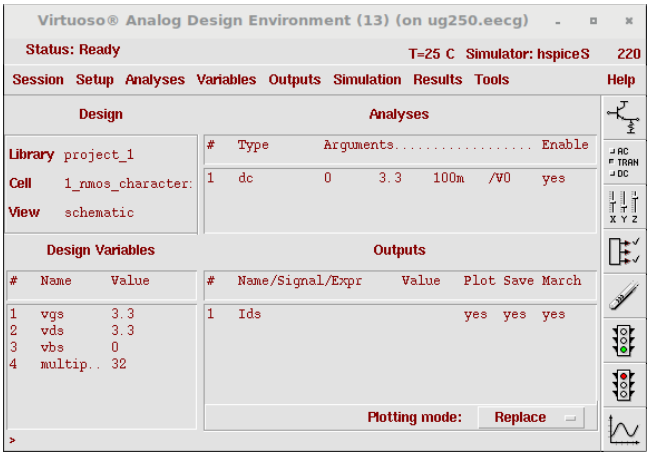
1. Device characterization (see all plots at end of section 1, all in one page)

1.1 Use Cadence Composer to generate I-V curves like those of Figures 8.16 and 8.17 (a, b, c, d) in the book for nMOS and pMOS transistors. (Unit transistor of 4λ/2λ: λ = 0.2 μm)

NMOS Device Characterization

We used the following standard schematic and analog simulation test-bench for NMOS transistor characterization.





a. Ids vs. Vds for different Vgs (Wn = 32 units)

For this question we are asked to characterize the drain to source current (Ids) response versus drain to source voltage (Vds) for a 32 units transistor (m = 32), while varying the gate to source voltage Vgs from 0 to 3.3V at linear increments. (We used a parametric analysis to simulate the response at 0.3V increments of Vgs)

b. Ids vs. Vds for different Vgs (Wn = 64 units)

As required in the project write-up, we repeat the previous device simulation albeit for a larger device (m = 64). (note the increase in current at same Vgs from previous plot)

c. Ids vs. Vgs for different Vds (Wn = 32 units)

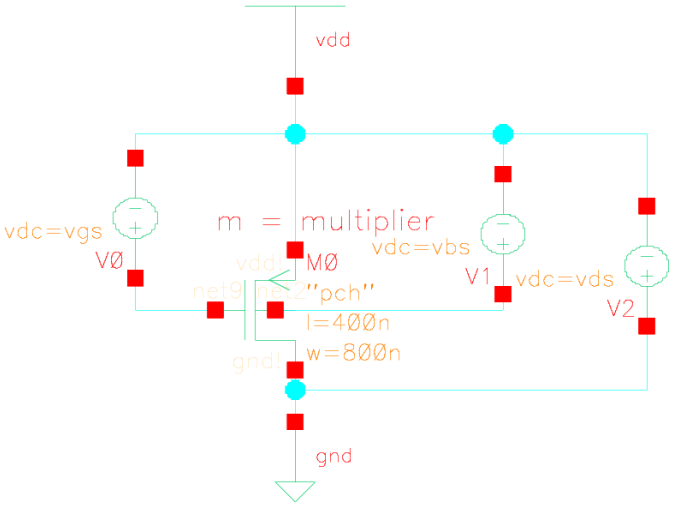
For this analysis in the book, the purpose is to measure drain to source current Ids versus gate to source Vgs voltage with drain to source voltages evaluated at both 0.1 and 3.3V

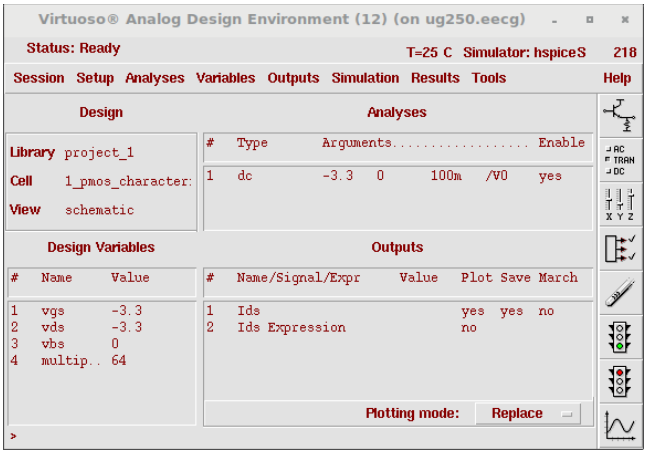
d. Ids vs. Vgs for different Vbs (Wn = 32 units)

The purpose of this plot is to see the impact of the bulk to source voltage (the back gate) on the drain to source current while sweeping the gate to source voltage of the transistor.

PMOS Device Characterization

We used the following standard schematic and analog simulation test-bench for PMOS transistor characterization.





a. Ids vs. Vds for different Vgs (Wp = 64 units)
Similarly, here we characterize the drain to source current (Ids) response versus drain to source voltage (Vds) for a 64 units transistor (m = 64), while varying the gate to source voltage Vgs from -3.3 to 0V at linear increments. (We used a parametric analysis to simulate the response at 0.3V increments of Vgs)

b. Ids vs. Vds for different Vgs (Wp = 128 units)
we repeat the previous device simulation albeit for a larger device (m = 128). (note the increase in current at same Vgs from previous plot)

c. Ids vs. Vgs for different Vds (Wp = 64 units)
The purpose here is to measure drain to source current Ids versus gate to source Vgs voltage with drain to source voltages evaluated at both -0.1 and -3.3V

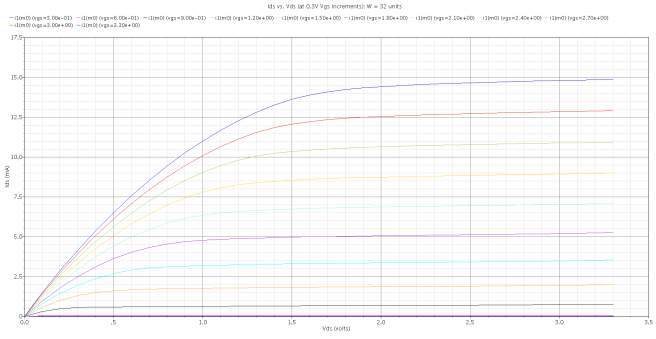
d. Ids vs. Vgs for different Vbs (Wp = 64 units)
The purpose of this plot is to see the impact of the bulk to source voltage (the back gate) on the drain to source current while sweeping the gate to source voltage of the transistor.

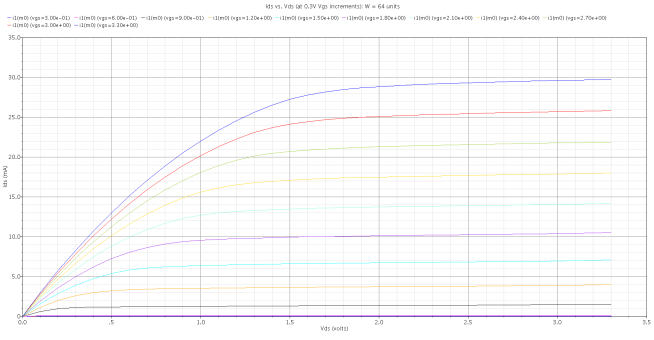
(see all plots on following page)

1.2 BONUS: Determine empirical velocity saturation models for the transistors in question 1 above for Wn,p = 32 units.

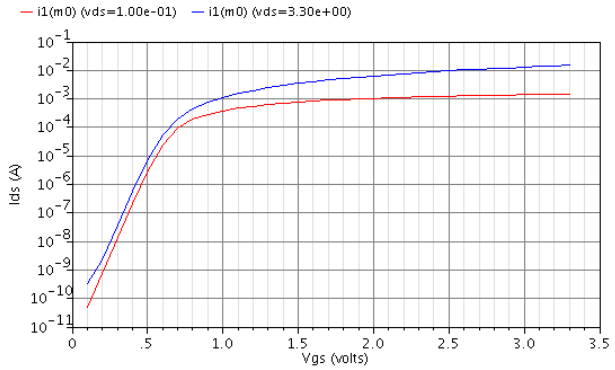
To be completed based on available time before deadline, see Appendix if applicable.

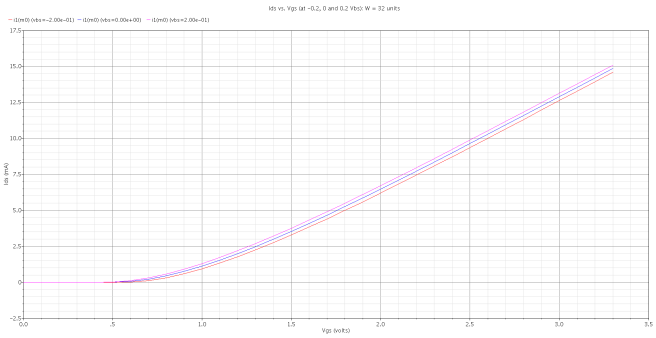
NMOS Device Characterization



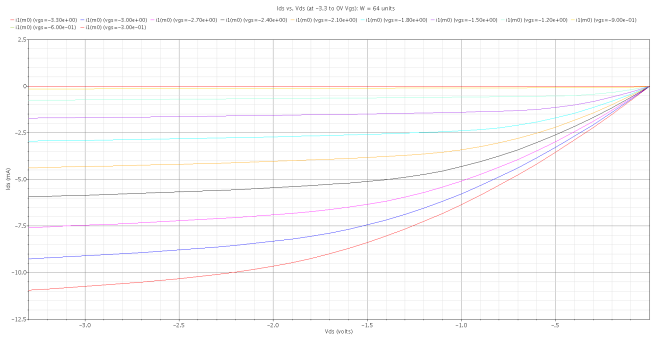


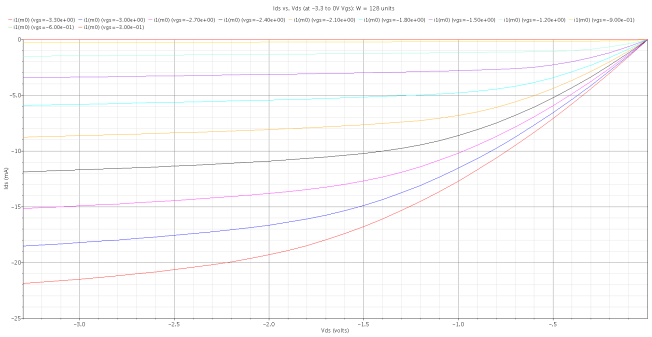
Ids vs. Vgs (at 0.1 and 3.3V Vds): W = 32 units



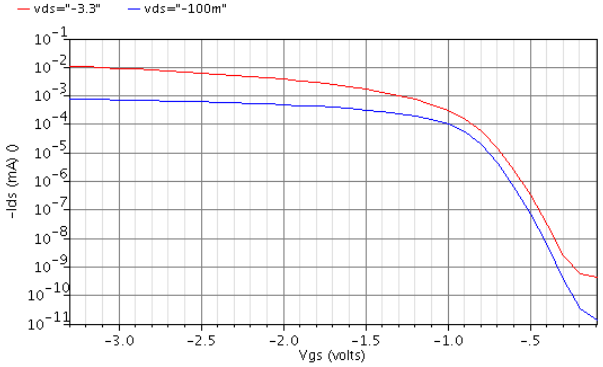


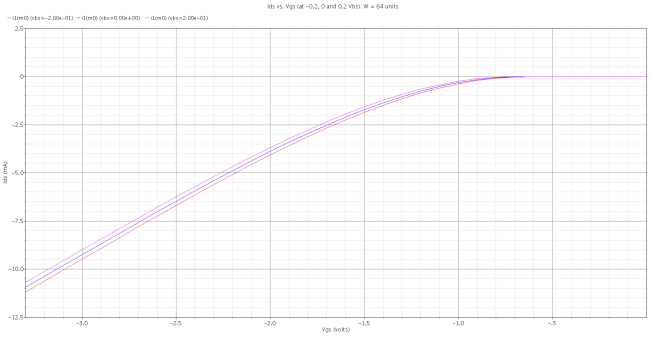
PMOS Device Characterization





Ids vs. Vgs (at -3.3 and -0.1 Vds): W = 64 units



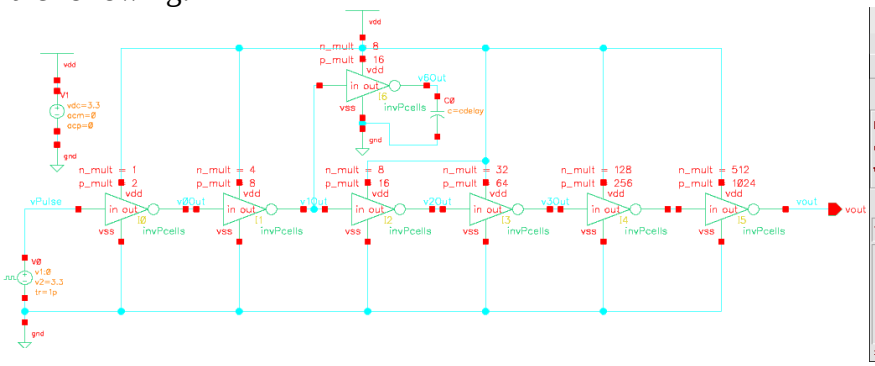


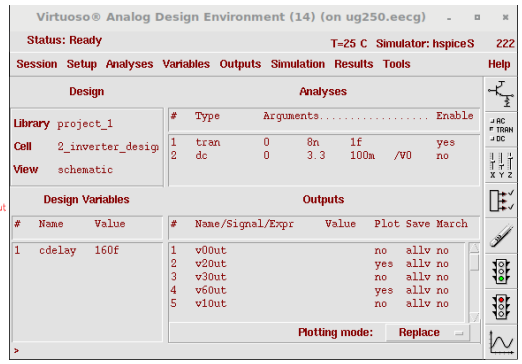
2. Circuit design and characterization with Cadence schematic entry

2.1 Determine the effective gate capacitance of a 64/32 inverter following the instructions in Section 8.4.3 with reference to Figure 8.22.

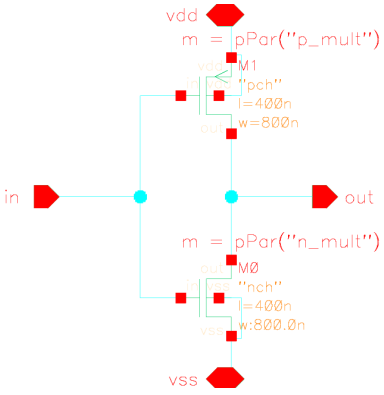
In order to calculate the gate capacitance we used the testbench outlined in figure 8.22. Here the input gate capacitance of the 64/32 inverter can be found by tunning the value of the delay capacitor Cdelay until the value of the delay from node c to g is equal to the delay from node c to g. In other words, the delay can only be equal if the capacitive load driven by inverter X6 is equal to that driven by inverter X3; the capacitance value found would then be our effective gate capacitance for inverter X4.

Our schematic testbench to find the effective gate capacitance (and for our subsequent questions) was the following:





With our parametrized inverter cell as below:



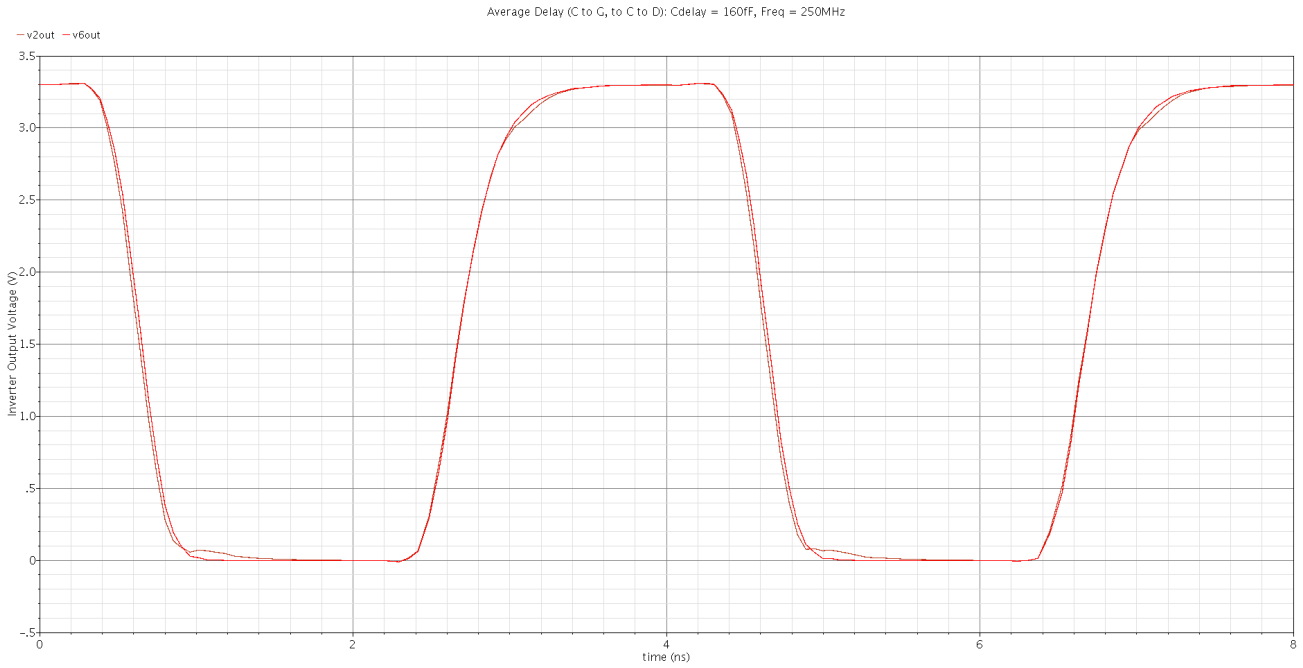
For our pulse source we reduced the frequency to 250MHz (compared to that provided in the book spice deck: this was intended to be used for 65nm technology with much lower capacitances and able to operate at much higher speeds). At 250MHz a delay is present, measurable and appropriate for our calculations.

In order to fine tune Cdelay in order to equalize the average delay for both branches, we used multiple parametric analyses to close-in on the optimal capacitance value. **The Cdelay value which minimized distance between waveform delay from c to g and from c to d is** $C_{delay} = 160\,fF$

Furthermore from the total gate width of X4 we can then obtain the capacitance per µm which allows us to compare our results from that found under Table 8.5 (for TSMC 350nm).

The capacitance per unit µm in our case is $C_g = \frac{C_{delay}}{W_{total}} = \frac{160\,fF}{(32\,x\,0.8\,\mu m) + (64\,x\,0.8\,\mu m)} = 2.083\,fF/\mu m$

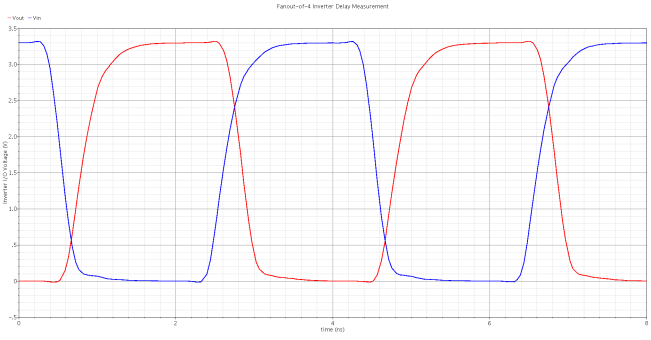
Fortunately this is very close to the value of 1.9 fF/µm found in table 8.5. Both output waveforms from inverter X3 and X6 loaded with 160fF are plotted below. (note the delays are very close as expected)

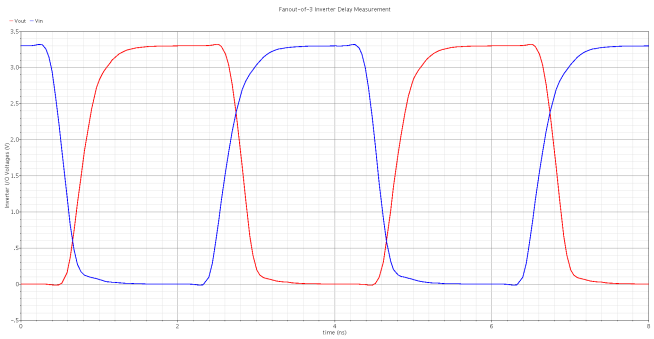


2.2 Calculate the effective resistance of single nMOS (Wn = 32 units) and pMOS (Wp = 64 units) transistors without calculating parasitic capacitances

In order to calculate the effective resistance we calculated first the inverter propagation delays at a fanout-of-3 (h=3) and subsequently at a fanout-of-4, then calculate their respective differences and use equations 8.7 accounting for total resistances (omitting factor of 3).

The fanout-of-3 testbench was similar to our standard testbench above, however both the load and load-on-load inverters we re-sized to be 3 times the size of the previous inverter. (i.e. 96/192 and 288/576 respectively). The fanout-of-4 testbench is our original testbench as the load and load-on-load inverters are already sized appropriately for this test. The propagation delays for h=4 and h=3 were measured from the following waveforms respectively. (note the differences are in the pS range)





The **64/32 inverter delays at h=4** are $t_{pdf} = 215\,pS$ $t_{pdr} = 271.3\,pS$
The **64/32 inverter delays at h=3** are $t_{pdf} = 195.1\,pS$ $t_{pdr} = 243.7\,pS$

Therefore the difference in delays at difference fan-outs are: $\Delta t_{pdf} = 19.9\,pS$ $\Delta t_{pdr} = 27.6\,pS$

Effective total PMOS resistance

Now to calculate total resistance (omitting factor of 3):

$\Delta t_{pdr} = \frac{R_p}{2}(3\,x\,4\,x\,C + 3C_d) - \frac{R_p}{2}(3\,x\,3\,x\,C + 3C_d)$ and expanding and canceling 3Cd

$\Delta t_{pdr} = \frac{4R_pC}{2} + 3C_d\frac{R_p}{2} - \frac{3R_pC}{2} - 3C_d\frac{R_p}{2} = \frac{R_pC}{2}$ and solving for Rp $R_p = \frac{2\Delta t_{pdr}}{C}$

Therefore in our case our **Effective total PMOS resistance:** $R_p = \frac{2\,x\,27.6\,pS}{160\,fF} = 345\,\Omega$

or in terms of per unit µm: $R_p(single) = R_p W_p = 345\,\Omega\,x\,64\,x\,0.8\,\mu m = 17.66\,k\Omega * \mu m$

Which intuitively agrees with our expectations and compares well with our reference value from table 8.5 $R_p(single) = 16.1\,k\Omega * \mu m$

Effective total NMOS resistance

Similarly to calculate the effective NMOS total resistance:

$\Delta t_{pdf} = R_n(3\,x\,4\,x\,C + 3C_d) - R_n(3\,x\,3\,x\,C + 3C_d)$ and expanding and canceling 3Cd

$\Delta t_{pdf} = 4R_nC + 3R_nC_d - 3R_nC - 3R_nC_d = R_nC$ and solving for Rn $R_n = \frac{\Delta t_{pdf}}{C}$

Therefore in our case our **Effective total NMOS resistance:** $R_n = \frac{19.9\,pS}{160\,fF} = 124.38\,\Omega$

or in terms of per unit µm: $R_n(single) = R_n W_n = 124.38\,\Omega\,x\,32\,x\,0.8\,\mu m = 3.184\,k\Omega * \mu m$

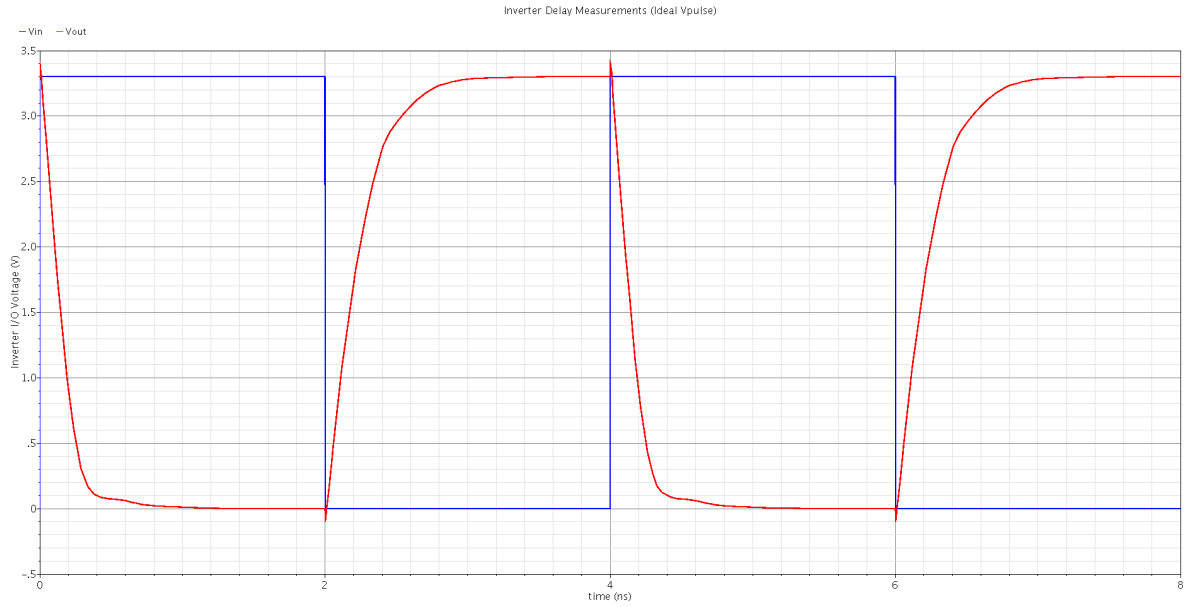
Which we can cross-check with our reference value from table 8.5 $R_n(single) = 5.73\,k\Omega * \mu m$

2.3 By what percentage does the delay of the 64/32 inverter from question 2.1 change if the input is driven by a voltage step rather than a pair of shaping inverters?

The current rise and fall propagation delays for our 32/64 inverter are from before:

Original 6s4/32 inverter delays at h=4 are $t_{pdf} = 215\,pS$ $t_{pdr} = 271.3\,pS$

Now if we remove the shaping inverters and apply an ideal voltage step to our inverter under test, our propagation delays change significantly (see waveform below) and our rising and falling propagation delays become:



With no pre-shaping inverters (ideal input pulse) at h=4: $t_{pdf} = 132.2\,pS$ $t_{pdr} = 190.2\,pS$

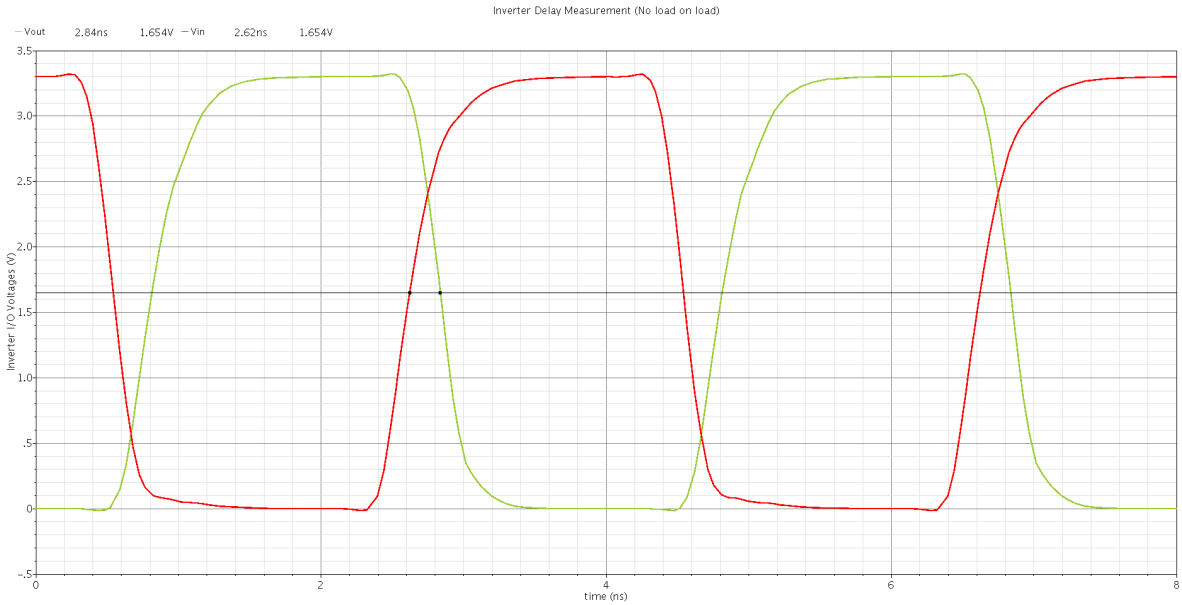
i.e. **The falling propagation delay** becomes $132.2\,pS / 215\,pS = 0.615$ 61.5% of the original falling propagation delay **(decreases by 38.5%)** and **the rising propagation delay** becomes $190.2\,pS / 271.3\,pS = 0.701$ 70.1% of the original rising propagation delay. **(decreases by 29.9%)**

2.4 Using the test bench from question 2.1 (with the X6 delay estimation inverter omitted), by what percentage does the delay of the 64/32 inverter change if the load-on-load inverter is omitted?

The current rise and fall propagation delays for our 32/64 inverter are from before:

Original 64/32 inverter delays at h=4 are $t_{pdf} = 215\,pS$ $t_{pdr} = 271.3\,pS$

Now putting the shaping inverters back in place and omitting the 1024/512 load-on-load inverter our propagation delays change very slightly (see waveform below) and our falling and rising propagation delays become:

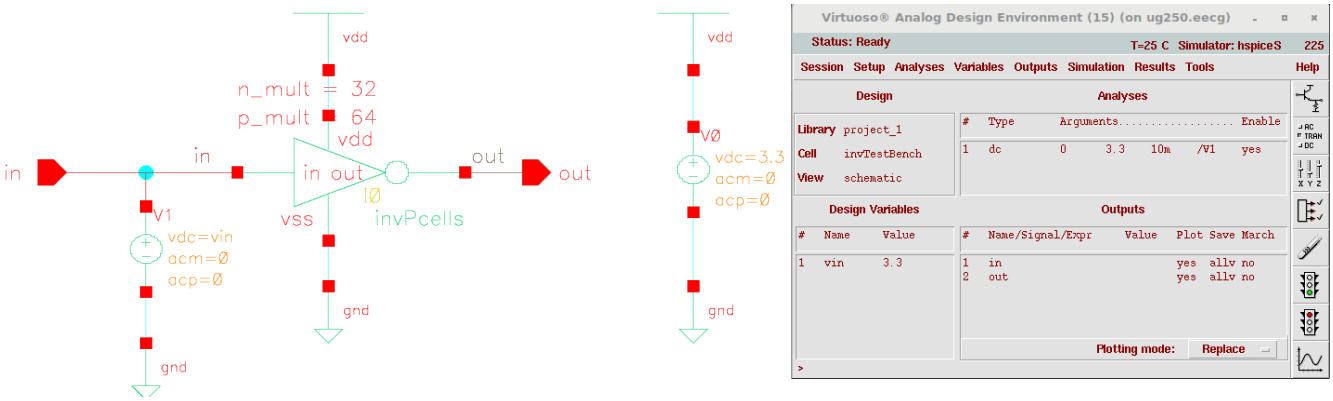


With no load-on-load inverter: $t_{pdf} = 215.6\,pS$ $t_{pdr} = 273.4\,pS$

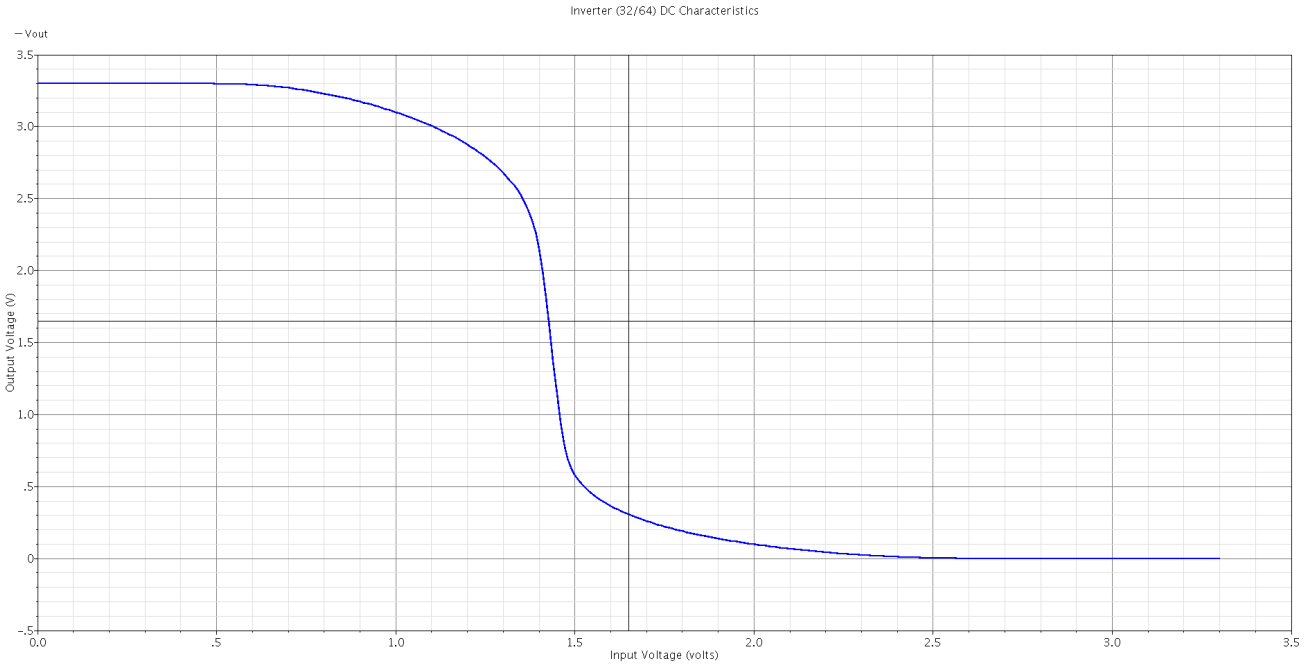
i.e. **The falling propagation delay** becomes $215.6\,pS / 215\,pS = 1.0028$ (**increases by 0.28%**) and **the rising propagation delay** becomes $273.4\,pS / 271.3\,pS = 1.077$ (**increases by 0.77%**)

2.5 Find the input and output logic levels and high and low noise margins for the 64/32 inverter in question 2.1.

Our individual inverter simulation testbench to characterize inverter noise margins is as follows:



Now from our DC simulation waveform sweeping the input voltage from low to high (0 to 3.3V respectively) we get the following inverter response (see waveform below). Note (from the vertical and horizontal markers at Vdd/2) the inverter response is skewed with $\frac{\beta_p}{\beta_n}<1$ (we would need to widen the size of our PMOS for optimal noise margin)



The noise margins for our inverter are given by (from section 2.5.3 in reference texbook):

$NM_{low}=V_{IL}-V_{OL}$ $NM_{high}=V_{OH}-V_{IH}$ where:

$V_{IL}\rightarrow V_{(Input\,Low)}$ $V_{OL}\rightarrow V_{(Output\,Low)}$ $V_{OH}\rightarrow V_{(Output\,High)}$ $V_{IH}\rightarrow V_{(Input\,High)}$

Canonically these values are identified at points along the curve where the slope is -1, in our case we used the Cadence calculator derivative function to locate these points along the curve, mainly:

$V_{OH}=3.033\,V$ $V_{IL}=1.0744\,V$ and $V_{OL}=297.3\,mV$ $V_{IH}=1.6591\,V$

Therefore **our noise margins are**:

$NM_{low} = 1.0744 - 0.2973 = 777.1 mV = 0.235 Vdd$

$NM_{high} = 3.033 - 1.6591 = 1.3739 V = 0.416 Vdd$

2.6 Use the values for extracted gate capacitance and effective resistance of single nMOS and PMOS transistors to hand-calculate propagation delays of a fanout-of-5 inverter sized 64/32.

We know from our previous questions: $C_{gate} = 160 fF$ $R_p = 345\,\Omega$ $R_n = 124.38\,\Omega$ Additionally we know the propagation delays for our fanout-of-4 (h=4) test-bench: $t_{pdf} = 215\,pS$ $t_{pdr} = 271.3\,pS$ Therefore, with these values we can calculate parasitic Cds and Cdp for our fanout-of-4 (h=4) inverter testbench. (from figure 8.26 in the reference textbook, note we are omitting the factor of 3 since we are using total quantities)

$t_{pdr} = \frac{R_p}{2}(hC + C_{dp})$ expanding and solving for Cdp for h=4: $C_{dp} = \frac{2\,t_{pdr}}{R_p} - 4C$ we find **Cdp:**

$C_{dp} = \frac{2\,x\,271.3\,pS}{345\,\Omega} - 4\,x\,160\,fF = 932.75\,fF$

Similarly, we can calculate our value for Cdn:

$t_{pdf} = R_n(hC + C_{dn})$ expanding and solving for Cdn for h=4: $C_{dn} = \frac{t_{pdf}}{R_n} - 4C$ we find **Cdn:**

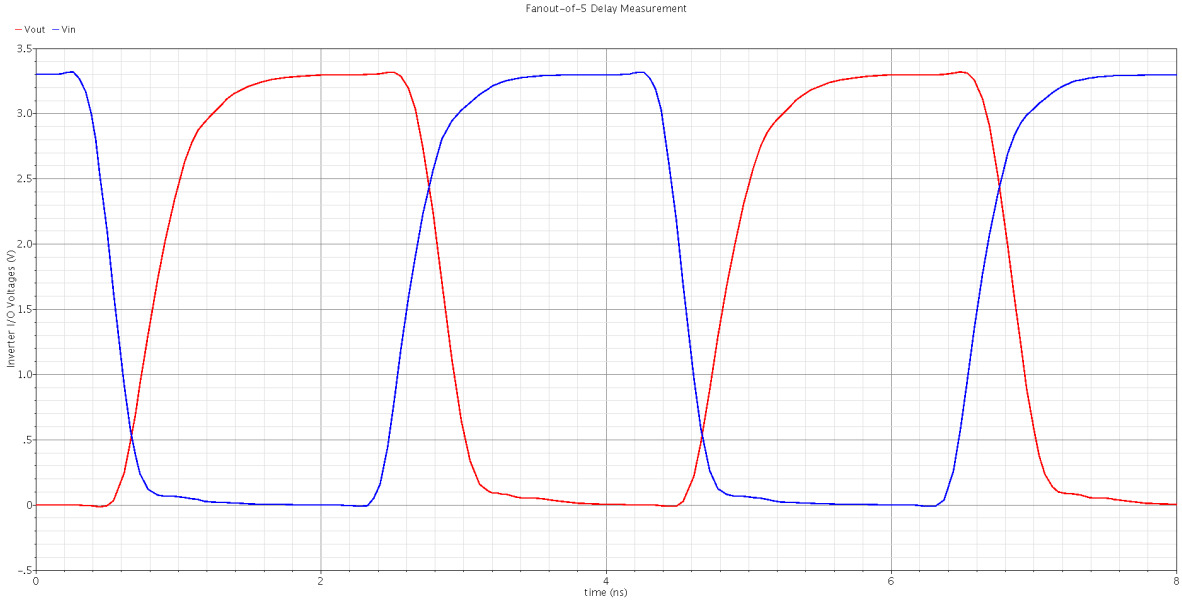
$C_{dn} = \frac{215\,pS}{124.38\,\Omega} - 4\,x\,160\,fF = 1.0886\,pF$

Subsequently we can calculate the **rise and fall propagation delays for a fanout of 5 inverter** testbench (using h = 5 in our equations above), respectively:

$t_{pdr} = \frac{R_p}{2}(hC + C_{dp}) = \frac{345\,\Omega}{2}(5\,x\,160\,fF + 932.75\,fF) = 289.9\,pS$

$t_{pdf} = R_n(hC + C_{dn}) = 124.38\,\Omega(5\,x\,160\,fF + 1.0886\,pF) = 234.9\,pS$

Now, we can modify our previous testbench to calculate the propagation delays for a fanout-of-5 inverter (h =5), i.e. resizing the subsequent stages (load and load-on-load) to be 5 times the previous stage respectively. From our simulation waveform:



we can extract, 64/32 inverter delays at a fanout-of-5 (h=5): $t_{pdr} = 296.6\,pS$ $t_{pdf} = 243\,pS$

Therefore, the percentage of difference in hand calculated results from that obtained during simulation is: for **rising propagation delay** $298.9\,pS / 296.6\,pS = 1.078$ (**0.78% difference**) and for **falling propagation delay** $234.9\,pS / 234\,pS = 1.0038$ (**0.38% difference**)

2.7 BONUS: Determine effective resistance of nMOS and pMOS transistors when two devices of each type (same size as in question 2.1) are connected in series in a fanout-of-h inverter (See Figure 8.27).

To be completed based on available time before deadline, see Appendix if applicable.

3. Layout design with Cadence Virtuoso layout editor (Inverter).

3.1 What P/N ratio maximizes the smaller of the two noise margins for the 64/32 inverter in question 2.1?

In order to maximize the smaller noise margin (Nmlow in our case) so as to optimize the noise margins such that our inverter has equal noise immunity at both logic levels: $NM_{low} = NM_{high}$ We need to attempt to make $\beta_p / \beta_n = 1$ for this inverter. In our case, after increasing the PMOS transistor size over small linear increments using parametric analyses over many runs, **we found a ratio of 128/32 (P/N = 4/1) to be optimal in achieving equal noise margins for this inverter.**

For our 128/32 noise inverter :
$V_{OH} = 2.9671\,V$ $V_{IL} = 1.3734\,V$ and $V_{OL} = 265.38\,mV$ $V_{IH} = 1.9354\,V$

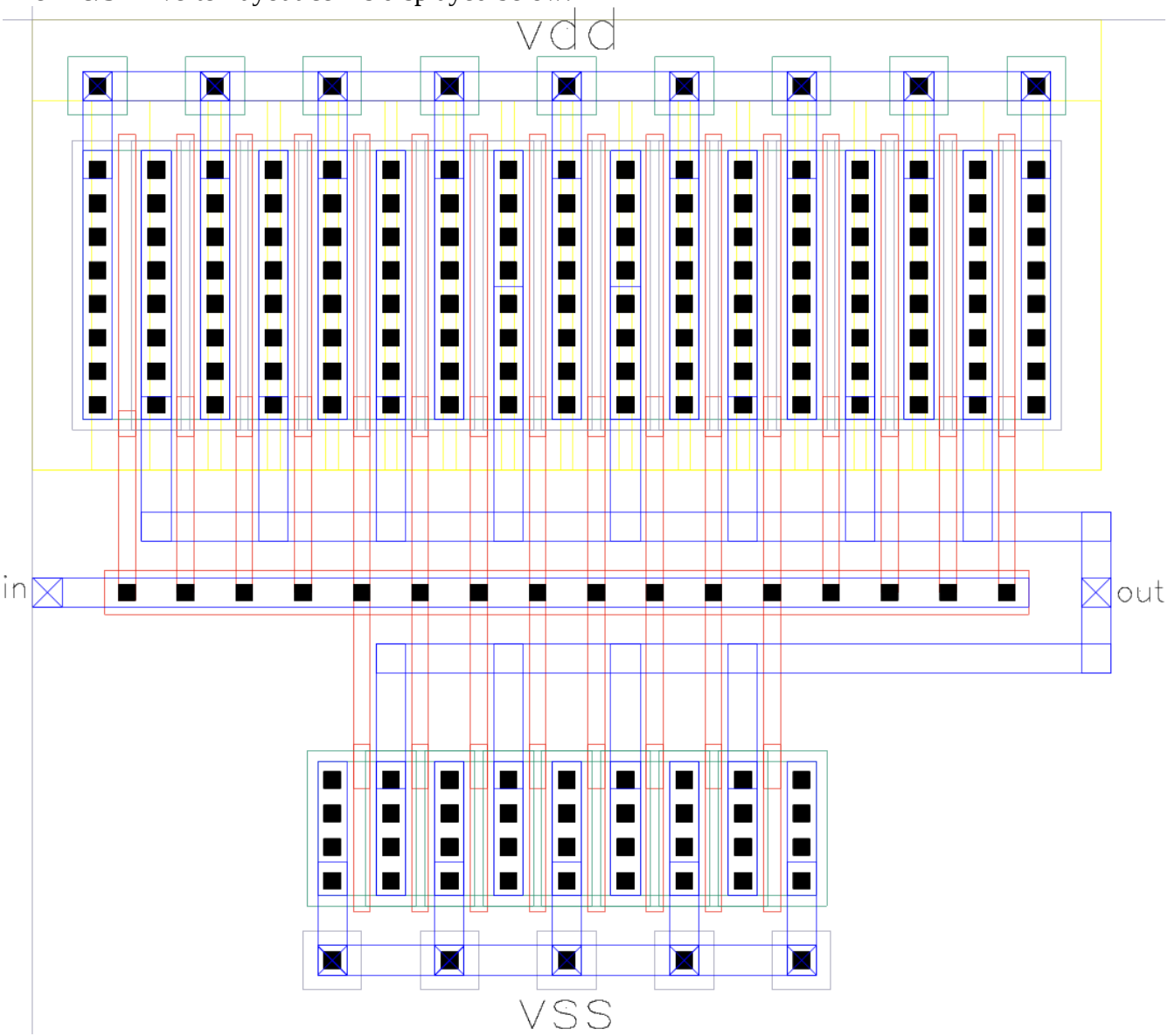
Therefore **our noise margins are**:
$NM_{low} = 1.3734 - 0.2654 = 1.1080\,V = 0.336\,Vdd$
$NM_{high} = 2.9671 - 1.9354 = 1.0317\,V = 0.313\,Vdd$

3.2 Implement layout, DRC and LVS for an inverter with the P/N ratio found in question 3.1.

As the transistor dimensions are large, Initially we planned the layout on paper to understand how to divide the transistor size optimally between m (multiplier: number of transistors in parallel) and Nf (number of fingers). In this case for the PMOS transistor for instance, it is not practical to layout a transistor with m = 128 (128 transistors in parallel would imply a very large poly gate and a finite detrimental resistance between the first and last transistor in parallel which leads to poor performance) nor is it practical to layout a wide transistor with 128 fingers. A better setup is to keep the number of transistors in parallel around below m<10 and size for the number of fingers accordingly to meet device size.
In our case we opted for the use of a unit PMOS transistor (as before) with m = 8 and Nf = 16, and a NMOS unit transistor with m = 4 and Nf = 8 to account for the layout of our 128/32 inverter.

For our layout, we used a minor grid of 0.175μm (λ = f/2 or 0.175μm) and a major grid of 5 λ, together with the good lambda-based rules provided in the class slides (useful to avoid DRC errors, especially off-grid). We used a snap grid of 0.005μm for convenience and toggled gravity as needed for our layout. Additionally we used the NMOS and PMOS template pcells (parametrized cells) as a starting point for our layout (nfet and pfet respectively) for our unit parallel transistors. *The VLSI manual was very helpful in getting up to speed with layout practice in order to complete this question.*

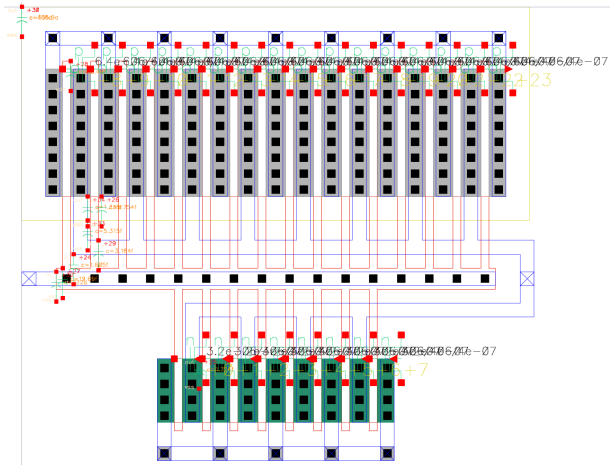
The 128/32 inverter layout cell is displayed below:



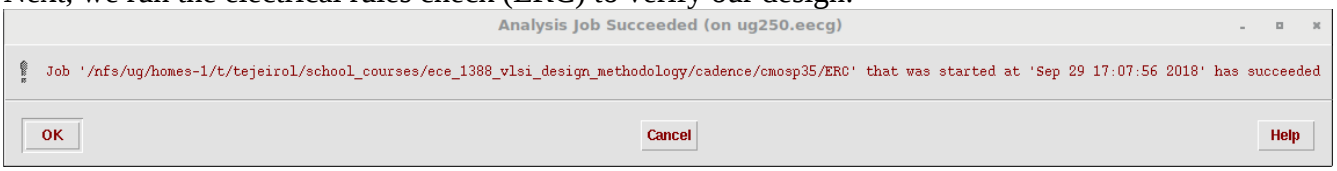
It took quite sometime of understanding errors and modifying layout to pass the DRC:

```
*********   Summary of rule violations for cell "3LargeInverterLayout layout"   *********
  Total errors found: 0
```

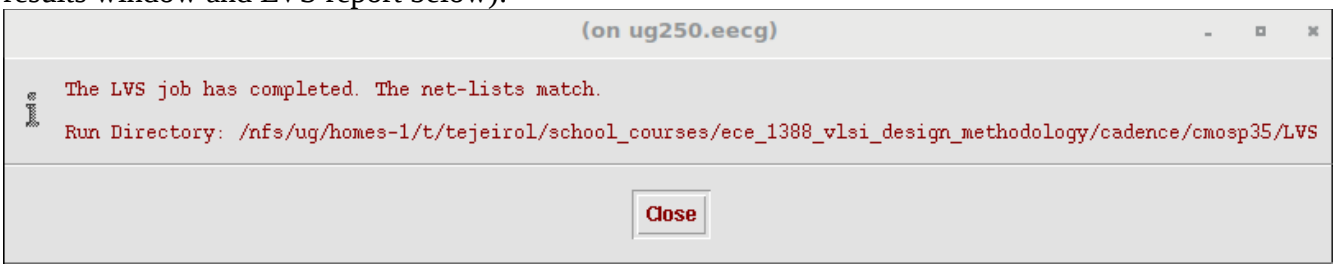
Subsequently we performed layout extraction (extracted layout below):



Next, we run the electrical rules check (ERC) to verify our design:



And then we run LVS to compare our extracted layout with our 128/32 inverter schematic cell (see results window and LVS report below):



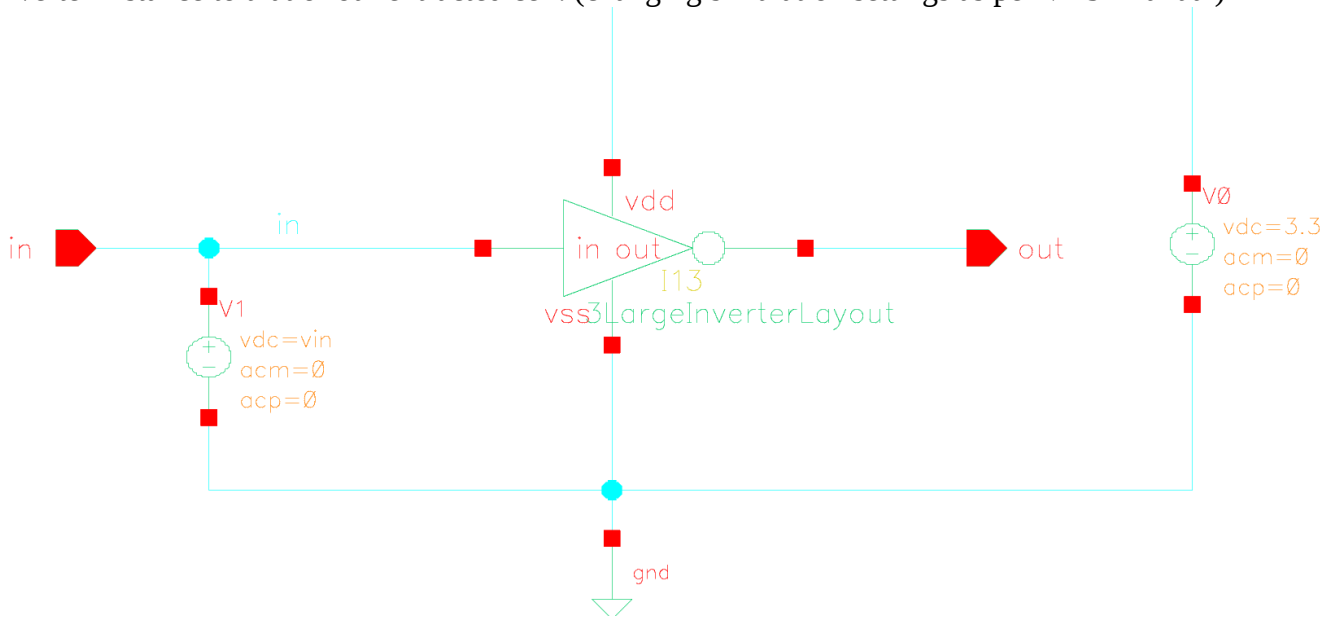
LVS Report

```
@(#)$CDS: LVS.exe_64 version 5.1.0-64b 04/27/2009 03:12 (cicamd10) $

Command line: /nfs/vrg/cmc/cmc/tools/cadence.2000a/IC.5141.ISR200905011535/tools.lnx86/dfII/bin/64bit/LVS.exe -dir /nfs/ug/homes-
1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS -l -s -t /nfs/ug/homes-
1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS/layout /nfs/ug/homes-
1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /nfs/ug/homes-1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS/layout/netlist
       count
       4            nets
       4            terminals
       8            nfet
       16           pfet

    Net-list summary for /nfs/ug/homes-1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS/schematic/netlist
       count
       4            nets
       4            terminals
       1            nfet
       1            pfet

    Terminal correspondence points
    N3        N1        in
    N2        N3        out
    N0        N0        vdd
    N1        N2        vss

Devices in the rules but not in the netlist:
       capacitor resistor

The net-lists match.

                        layout  schematic
                          instances
      un-matched          0      0
      rewired                    0      0
      size errors         0      0
      pruned              0      0
      active              24     2
      total               24     2

                            nets
      un-matched          0      0
      merged              0      0
      pruned              0      0
      active              4      4
      total               4      4

                          terminals
      un-matched          0      0
      matched but
      different type             0      0
      total               4      4

Probe files from /nfs/ug/homes-1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS/schematic

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
```

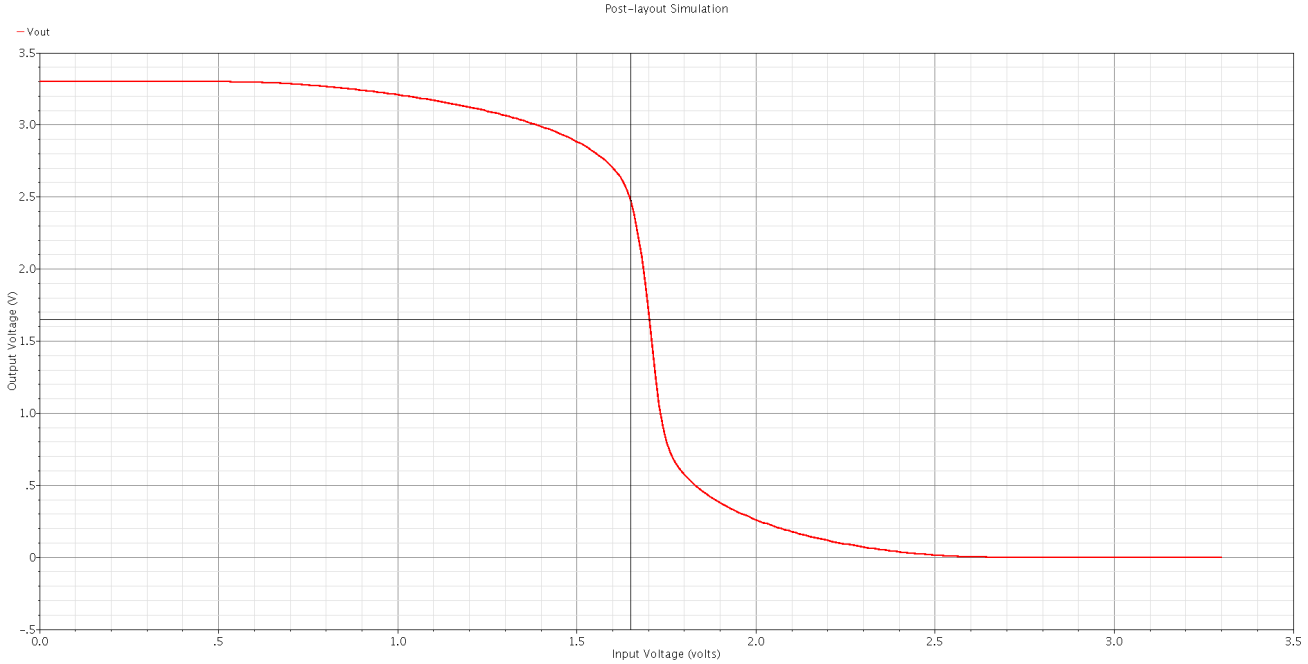
```
prunedev.out:
audit.out:

Probe files from /nfs/ug/homes-1/t/tejeirol/school_courses/ece_1388_vlsi_design_methodology/cadence/cmosp35/LVS/layout

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

Finally we performed Post-layout simulation: first we created a pins-only schematic from the extracted layout, next from the pins only schematic we created its respective symbol.

In order to simulate our layout, we used our single inverter testbench from before and changed the inverter instance to that of our extracted cell. (changing simulation settings as per VLSI manual)



Then we sweep the DC input voltage to find the inverter response and noise margins:



As can be seen, the inverter response from the extracted layout is very close to our desired optimal noise margins response but slightly skewed with β_p/β_n slighlty greater than one.

Specifically from our extracted inverter post-layout simulation we have:
$V_{OH}=2.9462\,V$ $V_{IL}=1.4463\,V$ and $V_{OL}=268.38\,mV$ $V_{IH}=1.9925\,V$

Therefore **our noise margins are**:
$NM_{low}=1.4463-0.26838=1.1779\,V=0.357\,Vdd$
$NM_{high}=2.9462-1.9925=0.9537\,V=0.289\,Vdd$

This amounts to 6.25% greater for our low noise margin and 7.67% lower for our high noise margin.