7 Band Graphic Equalizer Analog Design

EE 433 Lab Project 1

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***Abstract*—** **The purpose of this project was to create a seven band graphic equalizer to give us control over the amplitude of a sound signal at seven different resonant frequencies ranging from bass (low frequencies) to treble (high frequencies) therefore tailoring the sound signal to a listeners preference. An array of specifications had to be met including setting up the equalizer to achieve predefined -3dB frequencies for each band, operation from no more than +/- 12 V rails, and frequency response as linear as possible when all the bands were set to maximum boost, meaning that the entire input signal would get transferred to the output with no attenuation nor ripple.**

Graphic Equalizers; Audio Equalization; Audio Applications; Band Pass Filters

# Introduction

After careful consideration, we decided to model our equalizer circuit topology based on the series RLC resonant filter scheme with inductor simulation (due to the limitations in inductor values). In this type of circuit each band provides a low impedance path to ground at a particular band’s resonant frequency, this is since both the inductor and capacitor will act as “shorts” at that frequency. Each filter is composed of series RLC circuit acting as a band pass filter with the cutoff points defined by the required 3db attenuation and a potentiometer that provides cut or boost based on if it’s turned to the “left” or to the “right” respectively. The inductor is simulated with a gyrator op amp circuit.

# Body

For this design we aimed to both find a circuit topology that was easy to understand intuitively with the knowledge and experience of the lab partners and one in which the equations governing the center frequency and quality factor could be made to be relatively independent of the same components even if this meant a small sacrifice in circuit performance over other more complex designs. The team also aimed to focus on five design priorities: The minimization of power consumption, the efficiency of the output stage, the accuracy of center frequencies and cutoff frequencies, the portability of the design (battery powered) and a relatively small scale discrete implementation

## Design Considerations

The quality factor: After multiple iterations to try to minimize ripple but meet the 3 dB attenuation specs at the corner frequencies, the quality factor Q which determines the bandwidth of the band pass filter was set to 1.7, this is also what was found to be recommended for octave equalizers.

The center Frequencies: Due to the non-idealities of real systems (component tolerance values, breadboard parasitic capacitance … etc.) as compared to simulations, the capacitance values had to be modified In order to set the center frequency as close to the ideal values as possible, this was done via the use of the oscilloscope FFT function as well as through a manual frequency sweep analysis.

The output stage: Pursuing our aim for low power, single supply and maximization of the output stage efficiency we considered the use of a bridge output stage implementation that could drive a load as close to the supply rails as possible, since our experience in efficient output stages is very limited, the decision was to integrate a TDA2822M Integrated chip to our design. The TDA2822M is a monolithic low power single supply dual audio amplifier IC that we configured to run in a bridge configuration.

## Key Design equations

The Design equations used for this circuit topology are the following (Refer to Schematic, Appendix B):

Inductors Reactance:

Quality Factor:

Inductance (Gyrator)

Center Frequency

The previous equations were arranged into iterative component equations, in the following form.

1. Choose R4 = 500Ω, Q = 1.7 and fo = center frequency, compute C2 from the rearranged equation.
2. Compute L
3. Choose R5 = 100KΩ
4. Compute C1 from the rearranged equation:

## Topology Discussion &Intuition behind the circuit

In order for the reader to understand the circuit topology better it is useful to first understand the intuition behind the inductor simulator or gyrator and then visualize two extreme cases while referring to the first band in the circuit schematic (Appendix, B). The first case is the one where the potentiometer is turned to the left completely and the second case is when the potentiometer is turned completely to the right. Let’s first apply a sine wave to the band pass circuit at the resonant frequency and introduce the gyrator; here as the voltage rises capacitor C2 will start charging which will make the potential at its lower plate drop, capacitor C1 in turn will try to decrease the potential at its lower plate by discharging it as well, what we end up then is the op amp’s non-inverting leg buffering this lower potential through the inverting leg to the output and creating a voltage drop across R4, that together with the very low impedance seen at the output of the op amp creates a low impedance path for the signal to ground. Now what this means is that as you sweep the potentiometer completely to the left you will have a voltage divider across R1 and R4 with a buffer at the output op amp U1A such that:

And

Therefore we get attenuation or cut by a factor of ~ 7.6.

As we sweep the potentiometer towards the other side we end up with a whole different scenario, now the low impedance path becomes part of the U1A op amp feedback network thus creating a non-inverting configuration with a gain of:

To get a complete view of the band pass stage let’s also analyze what happens when you sweep the frequency farther from the center frequency, to do this it is easier to go back to the RLC band pass circuit. As the sweeping frequency starts to go higher than the cutoff frequency the inductor will start to act as a complete “open” and thus we get severe attenuation (in the gyrator, the potential difference across R4 will be zero thus no current will go through there and the equivalent resistance will now be R5 = 100KΩ, the high impedance path), the same thing happens as the sweeping frequency proceeds farther than the lower cutoff frequency but now it is the capacitor that acts as an “open” and thus we get attenuation at both high and low frequencies.

# Results

The experimental results differed to some extent from those ideal results encountered during simulation (Appendix, C.3). The flatness of the frequency responses of all the bands under full boost or unity gain conditions was not ideal, during experimentation the gain at the lower frequencies/bands was more than 6 dB higher than that for the bands 6th and 7th, this problem was encountered as well during simulation and it was fixed by decreasing the resistors in the simulated inductor op amp feedback network so that the voltage attenuation and gain at the higher frequencies could be increased to compensate and increase the flatness of the response, this was not without its drawbacks decreasing this resistors would have increased the quality factor of the individual bands thus increasing the ripple considerably when all the bands were boosted. However due to other distortion problems that were at the moment more relevant to the quality of the output signal and a tight deadline, the team could not afford the time to experiment between the gain linearity/ripple tradeoff.

Another topic for concern that came up during experimentation was that of distortion more specifically crossover distortion, this created some harmonics which deteriorated the sound quality. The cause for this distortion after multiple days of research was found to be the operational amplifiers (LM124) being used which required output resistors to bias the output of each op amp and decrease distortion, this design decision would have gone against our aim of a low power equalizer, therefore the LM124 op amps were replaced for the low power MC3403 quad op amps with improvements in performance and power efficiency.

A strong emphasis was put on making sure the center frequencies were at the desired frequency locations, the cutoff points were met with 3dB attenuations, the adjacent center frequencies under single band boost were attenuated by 6 dB and the minimization of the supply rails and power consumption. To make sure that the 3dB points and the 6dB points were met the Q factor was initially set to 1.5, 2 and then 1.7 with the best ripple reduction effects found at 1.7 while still meeting the specs for the 3 and 6dB attenuation points.

To set the center frequencies at their corresponding locations the resistors were set fixed since changing them would have affected not only the center frequencies but also the Quality factors and the gains of each stage, therefore parallel and series combinations of capacitors were used to arrive at the desired center frequencies with very good results, the experimental waveforms arrived at after all the bands were modified was very similar to the simulation waveforms (Appendix C.4 – C.10).

Power efficiency and portability was pursued by limiting the supply voltage to single supply, 5 volts rail and the use of only low power active components and a minimum amount of resistors. The final quiescent current measurement for our circuit was 18 - 20 mA with 8 - 10 mA burned by the output stage alone.

Upon completion of the audio output stage and after thoroughly testing of the current capabilities of the amplifier, the equalizing and output stages were connected but the results were not satisfactory, an unexpected amount of distortion was experienced. The classical solution to this issue is often just very low output impedance from the first stage and very high input impedance for the second stage to prevent loading effects, but considering the fact that the input impedance was quite high to start with in the second stage, this solution provided a minimal increase in performance. The problem turned out to be the coupling of ac noise through both the ground and the Vcc planes, the origin of this noise could not be tracked in time to meet the deadline, however five techniques were used to decrease the noise: A floating load (bridge) configuration was used at the output so that only the difference between the inverted and non-inverted output signal was delivered to the speaker thus reducing common mode noise, a buffer was used at the output of the equalizing stage to make sure that both stages were virtually isolated, bypass capacitors were used at the supply rails to minimize high frequency signals in the rails and finally the breadboard architecture was kept compact and small by reducing the size of the wires and keeping the legs of the components as short as possible.

# Conclusion

The design explored for this project built on concepts that were in agreement with our experience and knowledge; higher complexity filter topologies would have come with increased performance but no real intuition or understanding from our part which we agreed was too high of a price to pay. Equalization and amplification was achieved successfully with a few distortion harmonics explained further in the results section, Power efficiency and portability were our biggest competitive advantage over other more complex designs with our design being able to be powered by 4 AAA batteries, a low idle current, a rail to rail bridge output stage and a very small form factor. Further improvements to this project such as the reduction of supply coupled noise and the increase of gain for the last two stages are clearly possible and will be applied by the designers as time allows.

##### References

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##### Appendix

## Cost Analysis

|  |  |  |  |
| --- | --- | --- | --- |
| Component | Quantity | Cost Per Unit | Total Cost |
| TDA 2822M Audio Amp IC | 1 | 1.62 | 1.62 |
| Electrolitic Capacitors Misc | 7 | 0.01 | 0.07 |
| Ceramic Capacitors Misc | 20 | 0.01 | 0.2 |
| Resistors 1% Tolerance | 22 | 0.01 | 0.22 |
| Potentiometers | 9 | 0.1 | 0.9 |
| MC3403 | 3 | 0.51 | 1.53 |
| Total |  |  | 4.54 |

## Circuit Scchematic

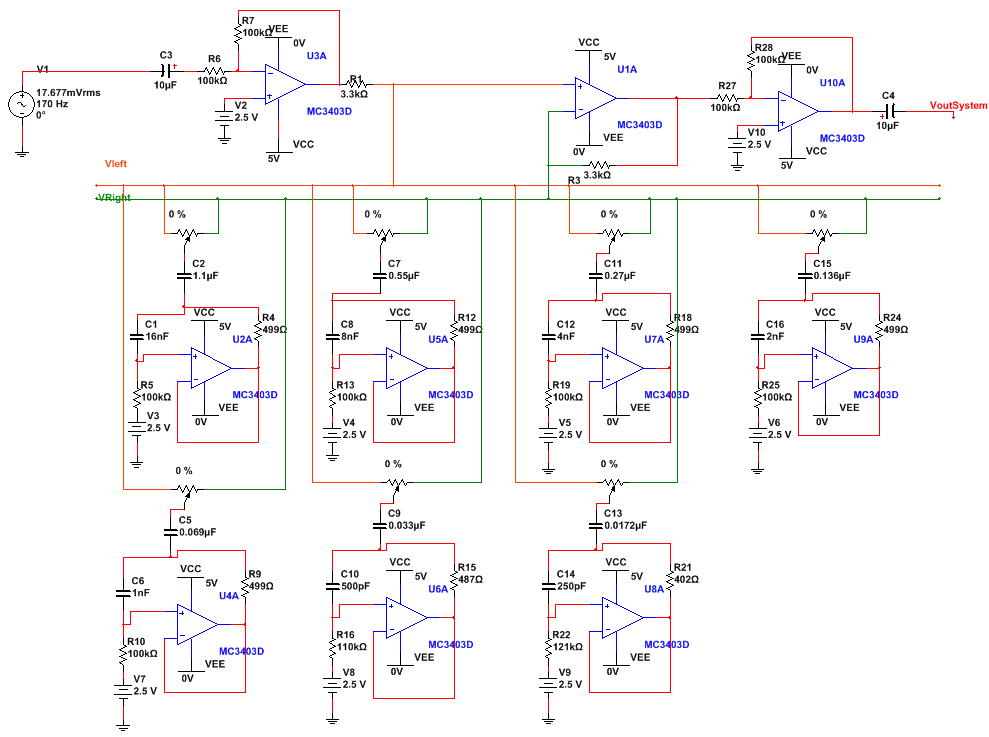


Figure 1. Graphic Equalizer Circuit Schematic

## Performance Analysis

C.1

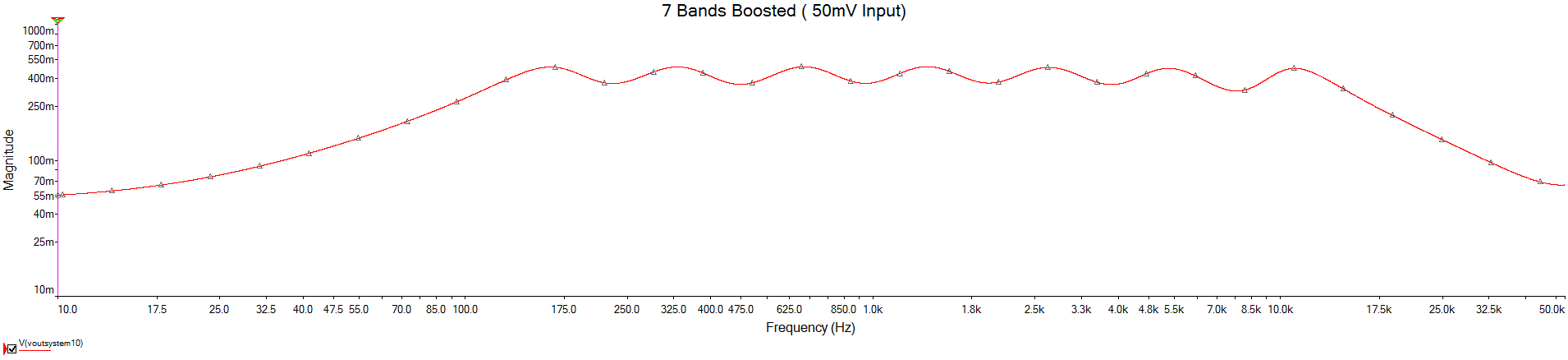


Figure 2. All Equalizer Bands Boosted

C.2

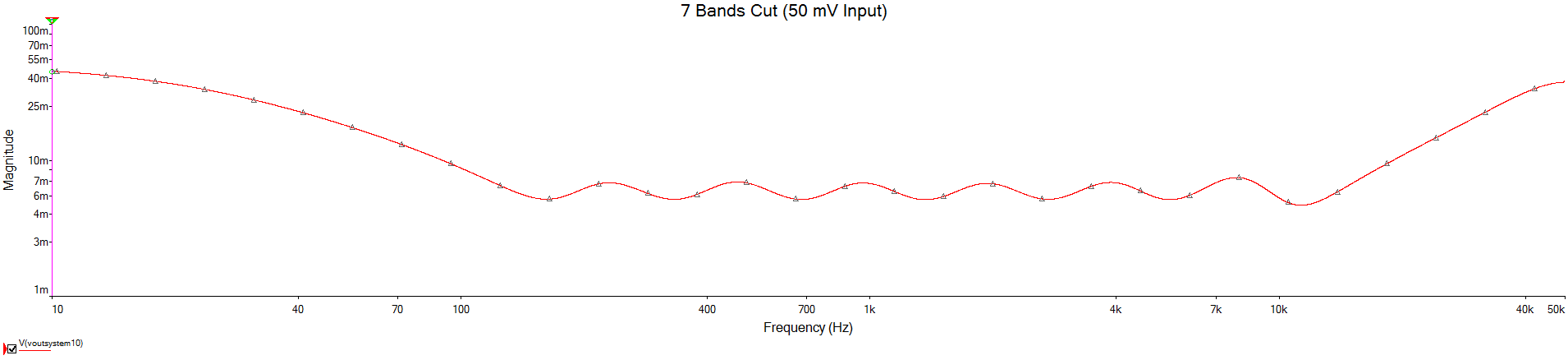


Figure 3. All Equalizer Bands Cut

C.3

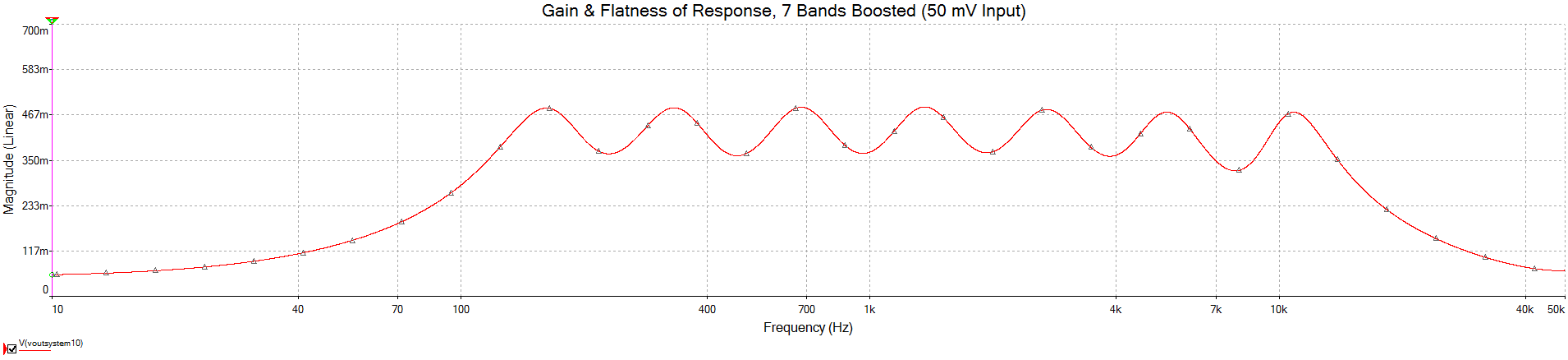


Figure 4. Gain & Flatness Performance Measure

C.4

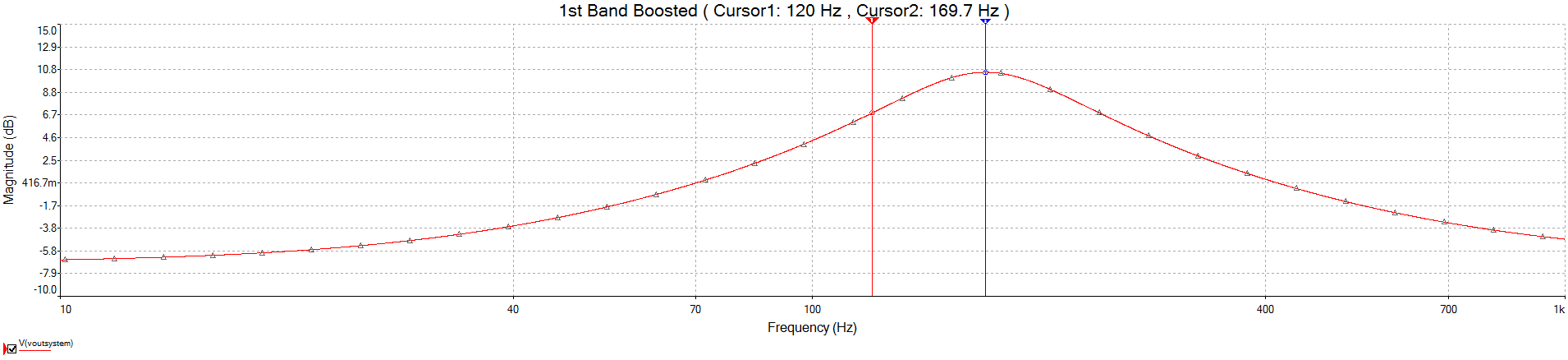


Figure 5. 1st Band Frequency Response

C.5

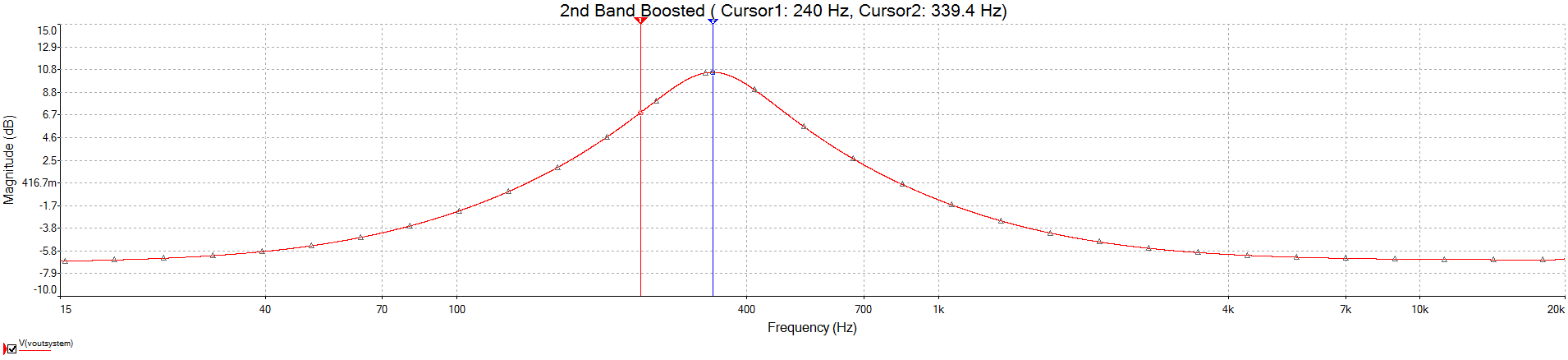


Figure 6. 2nd Band Frequency Response

C.6

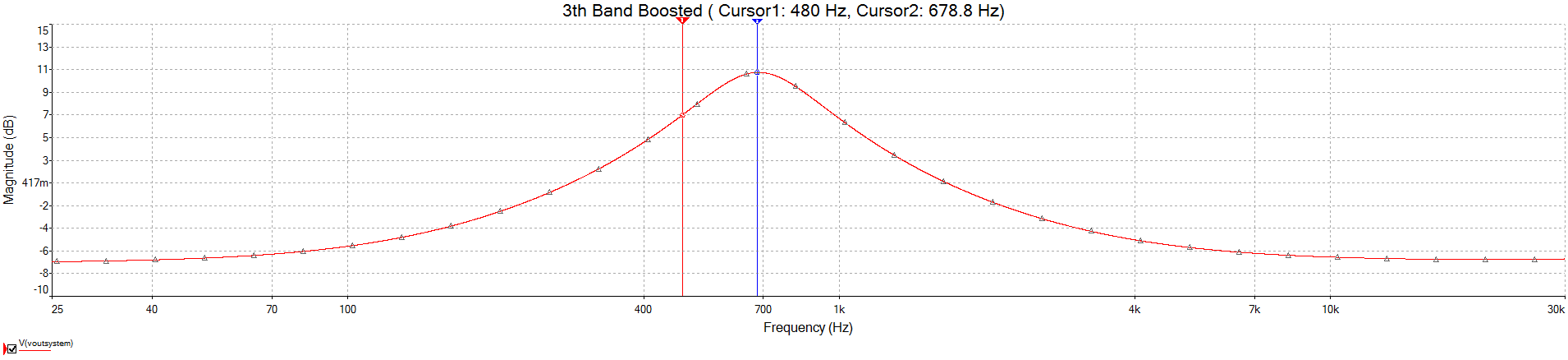


Figure 7. 3rd Band Frequency Response

C.7

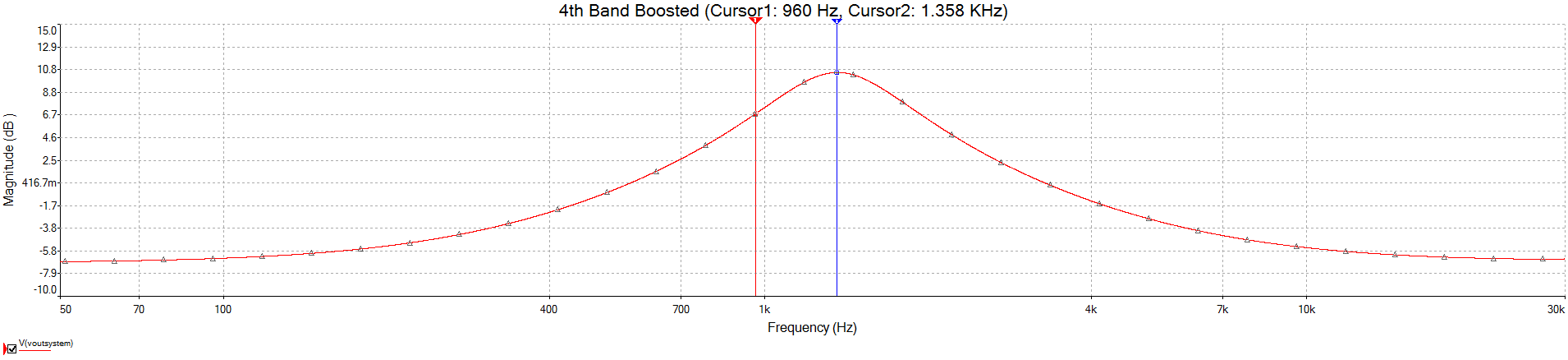


Figure 8. 4rd Band Frequency Response

C.8

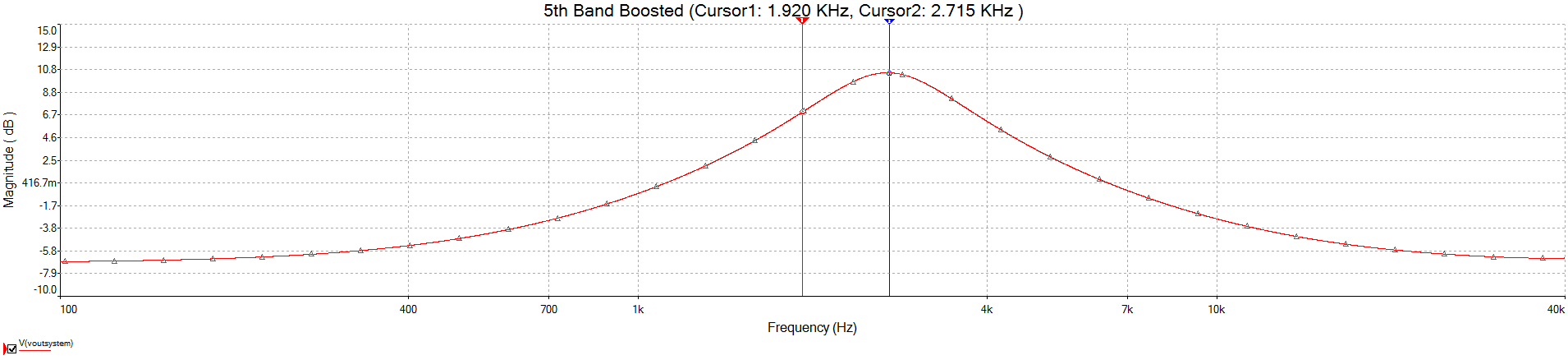


Figure 9. 5th Band Frequency Response

C.9

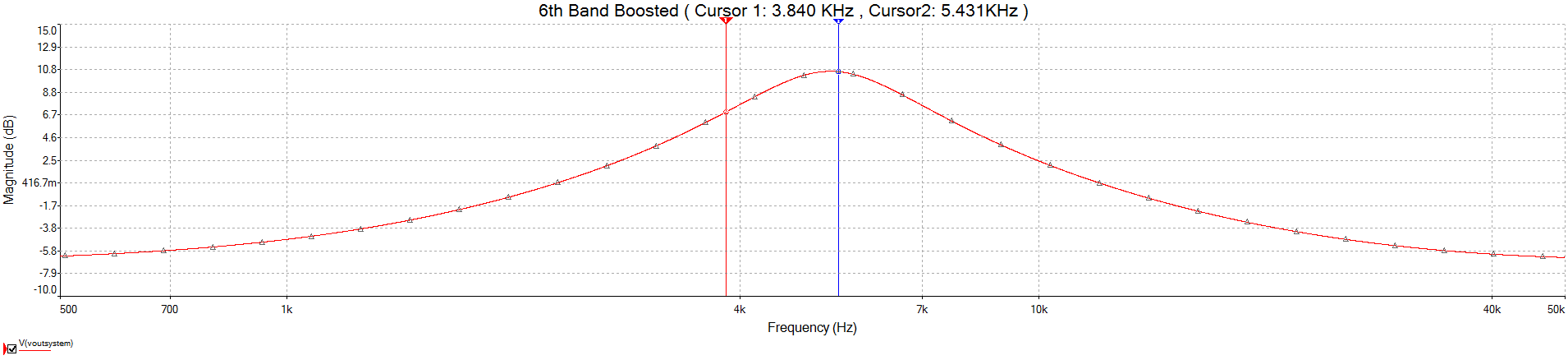


Figure 10. 6th Band Frequency Response

C.10

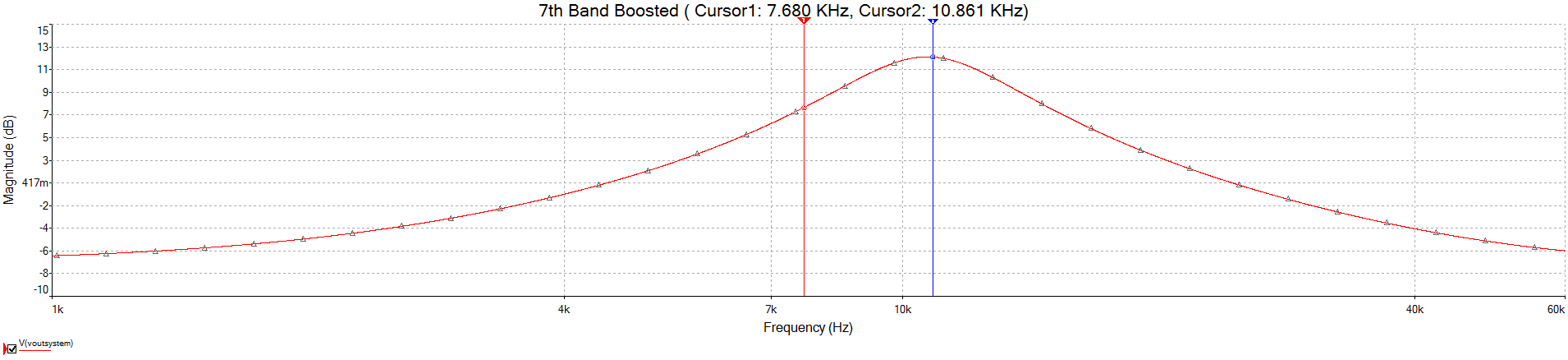


Figure 11. 7th Band Frequency Response