Date: February 10, 2020

Assignment 2 – Computer Organization
Class - 4CSE

Syllabus for First Sessional Examination:

Please find the correct edition of the following book to read

- **CSDA, Heuring 2nd edition: Chapters 1; 2.1-2.2; 7.1 - 7.5**

Practice Questions

[The objective is to get you in the habit of writing clear, precise and neat descriptions with diagrams preferably and also to look up various textbooks/material to find it.]

1. Explain the CPU architecture and instruction encoding of 4,3,2,1, and 0-address machines.
2. Given an expression to evaluate *a=((b+c)*(d-e))/(f+g)*, write minimal assembly code for the above machines.
3. A 64K SRAM chip can be manufactured in various configurations like (a) 64K x 1 or (b) 16K x 4. For each case draw a schematic, compute pin requirements and also discuss options to choose the cell array.
4. Design a 4 to 16 decoder as a (a) tree decoder (b) matrix decoder.
5. Give timing diagrams for read and write operations for a SRAM and DRAM.
6. Show memory cycles for Special purpose DRAMs.
7. How can we increase the address space using multiple SRAM chips? How does the design change if it is DRAM chips?
8. How does hit ratio vary with the set-associativity of the cache?
9. What are compulsory misses, capacity misses and conflict misses.
   Consider a machine with a byte addressable main memory of 216 bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50, 50 two dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses. Calculate the number of data cache misses that will occur in total.
10. Effective Access Time example: A computer has a single cache (off-chip) with a 2 ns hit time and a 98% hit rate. Main memory has a 40 ns access time. What is the computer's effective access time? If we add an on-chip cache with a .5 ns hit time and a 94% hit rate, what is the computer's effective access time? How much of a speedup does the on-chip cache give the computer?
11. Cache/Memory Layout: A computer has an 8 GByte memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4- way set associative cache, what is the new address format?
12. A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.
13. A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.
14. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.
    a. How is a 16-bit memory address divided into tag, line number, and byte number?
    b. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
    c. How many total bytes of memory can be stored in the cache?
    d. Why the tag is also stored in the cache?

15. Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.
   a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.
   b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.
   c. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

16. Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes.
   a. For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct mapped cache.
   b. Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache.
   c. For the main memory addresses of F0010 and CABBE, give the corresponding tag and offset values for a fully-associative cache.
   d. For the main memory addresses of F0010 and CABBE, give the corresponding tag, cache set, and offset values for a two-way set associative cache.

17. Our system has a main memory with 16 megabytes of addressable locations and a 32 kilobyte direct mapped cache with 8 bytes per block. The minimum addressable unit is a byte.
   a. How many blocks are there in the cache?
   b. Show how the main memory address is partitioned.

18. Find the average memory access time for a processor given the following:
   - The clock rate is 1 ns
   - The miss penalty is 25 clock cycles
   - 1% of instructions are not found in the cache.
   - 5% of data references are not found in the cache.
   - 15% of memory accesses are for data.
   - The memory system has a cache access time (including hit detection) of 1 clock cycle.
   - Assume that the read and write miss penalties are the same and ignore other write stalls.

19. Let's say if we make our cache 2-way set-associative over which the following data applies:
   - Data words are 32 bits each.
   - A cache block will contain 2048 bits of data.
   - The address supplied from the CPU is 32 bits long.
   - There are 2048 blocks in the cache.
   - Addresses are to the word.

   Calculate
      a. Number of bits in offset?
      b. Number of bits in index?
      c. Number of bits in tag?

20. Now, let's consider what happens if we make our cache 4-way set-associative. However, as before, the following still applies:
   - Data words are 32 bits each.
   - A cache block will contain 2048 bits of data.
   - The address supplied from the CPU is 32 bits long.

- There are 2048 blocks in the cache.
- Addresses are to the word.

Calculate

a. Number of bits in offset?
b. Number of bits in index?
c. Number of bits in tag?

21. Now, let's consider what happens if we make our cache 4-way set-associative. However, as before, the following still applies:

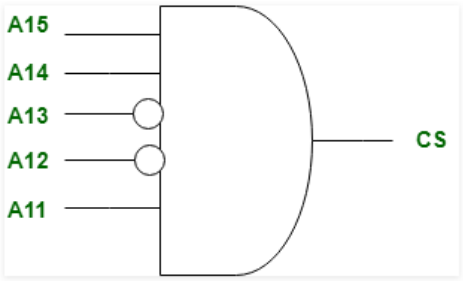
- Data words are 32 bits each.
- A cache block will contain 2048 bits of data.
- The address supplied from the CPU is 32 bits long.
- There are 2048 blocks in the cache.
- Addresses are to the word

Calculate

a. Number of bits in offset?
b. Number of bits in index?
c. Number of bits in tag?

22. A certain processor uses a fully associative cache of size 16 kB, The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the Tag and the Index fields respectively in the addresses generated by the processor?

23. The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A15 to A0. What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?



24. A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM would be?

25. How many 32K x 1 RAM chips are needed to provide a memory capacity of 256K-bytes?

26. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is?

27. A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

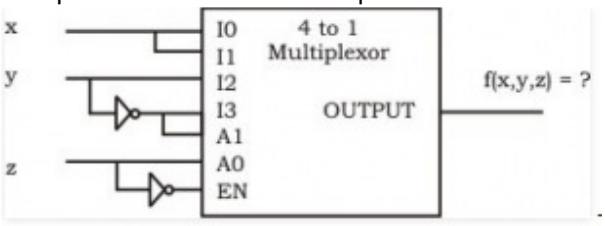
28. Suppose you want to build a memory with 4 byte words with a capacity of 2^{21}bits. What is type of decoder required if the memory is built using 2K x 8 RAM chips?

29. Number of chips (128 x 8 RAM) needed to provide a memory capacity of 2048 bytes?

30. Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

31. How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

32. Consider the following multiplexor where 10, 11, 12, 13 are four data input lines selected by two address line combinations A1A0 = 00, 01, 10, 11 respectively and f is "the output of the multiplexor. EN is the enable input.



33. The function f(x, y, z) implemented by the above circuit is :

34. A multiplexer combines four 100-Kbps channels using a time slot of 2 bits. What is the bit rate?

35. How many RAM chips of size (256K x 1 bit) are required to build 1M Byte memory?

36. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4 x 6 array, where each chip is 8K x 4 bits

37. How many addresses are required for 25 x 40 video RAM?

38. Four memory chips of 16 x 4 size have their address bases connected together. The system will be of size?

39. A 32 bit wide main memory unit with a capacity of 1GB is built using 256 M×4−bit DRAM chips. The number of rows of memory cells in the DRAM chip is 214. The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is?

40. A main memory unit with a capacity of 4 megabytes is built using 1M × 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. What is the time required to perform one refresh operation on all the cells in the memory unit.

For Submission

- Only questions 3, 13, 17 from Assignment 1 and questions 4, 15, 31, 39 from Assignment 2 on Due date: February 25, 2020
- Please submit only through your CR and do the assignment in a notebook and clearly specify your name and enrollment number on top.
- CR to coordinate with TA and transport all the assignments to the TA's cabin.