Computer Organization, 2015

Lab 6: Multi-Core

Due: 2015/06/18

1. Goal

Use the CPU in lab5 to implement a milti-core computing environment.

2. Demand

a. Use LAB5 pipelined CPU to implement multi-core CPU
- Must to implement Hazard Detection and Forwarding Unit.
- Need to forward data if instructions have data dependency.
- Need to stall pipelined CPU if it detects load-use.

b. Use the following instruction sets to do matrix multiplication

Instruction	OP Field	Function field
ADD	0x0	0x32
ADDI	0x8	
SUB	0x0	0x34
MULT	0x0	0x24
AND	0x0	0x36
OR	0x0	0x37
ORI	0x13	
SLT	0x0	0x2A
SLTI	0xA	
SLL	0x0	0x0
BEQ	0x4	
BNE	0x5	
BGT	0x7	
BNEZ	0x5	
BGEZ	0x1	
J	0x2	
JAL	0x3	
JR	0x0	0x8
LW	0x35	
SW	0x43	

c. Initial the matrix content in Data_Memory.v like the following graph
- You can modify the in/output port of Data_Memory.v by yourself
- mem[address](value)
- TAs will modify the initial value when grading LAB6

$$\begin{bmatrix} mem[0](1) & mem[1](3) & mem[2](-100) \\ mem[3](2) & mem[4](-2) & mem[5](10) \\ mem[6](3) & mem[7](1) & mem[8](0) \end{bmatrix} * \begin{bmatrix} mem[9](3) & mem[10](4) \\ mem[11](-2) & mem[12](5) \\ mem[13](-1) & mem[14](6) \end{bmatrix} = \begin{bmatrix} mem[15] & mem[16] \\ mem[17] & mem[18] \\ mem[19] & mem[20] \end{bmatrix}$$

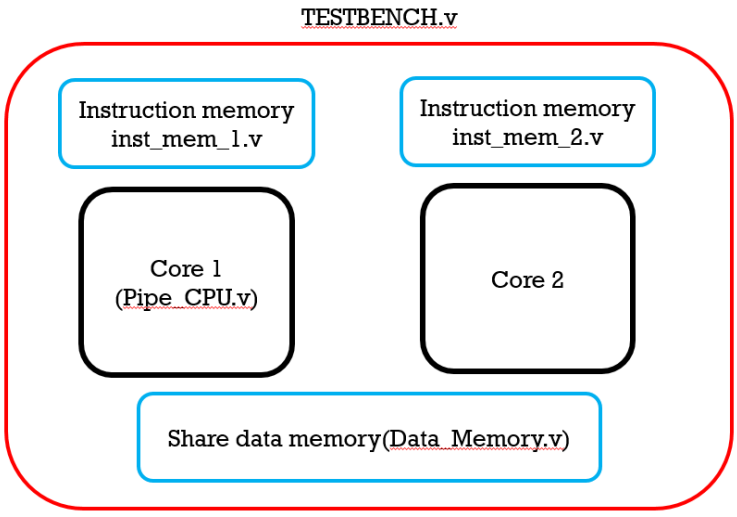
(Please initial the data like the figure. We will check the answers of this figure)

d. Submit your machine code and assemble code

- File name:
  i. LAB6_machine_1.txt / LAB6_ASM_1.txt (for core 1)
  ii. LAB6_machine_2.txt / LAB6_ASM_2.txt (for core 2)
- No grades will get if the file name is wrong

d. Write your own testbench called TESTBENCH.v

e. Architecture:



f. Answer the following questions in your report:

- How do you separate the program for the two cores?
- Assumed that programmers do not know the platform architecture (i.e. single core or multi-core) how can programmers manage their program partition?
- Assumed that each core has private cache. If core1 write a new data at address 0x123, how could core 2 get the new data from 0x123? (hint: coherence)
- Draw the detail architecture and describe your design in your report.
- Say something if you want

3. Grade

- Total score: 100(65 for RTL code and 35 for report pts.) COPY WILL GET 0 POINT!
- Delay: 10%off/day
- NO Demo in LAB6

4. Hand in your assignment

- Please upload the assignment to the E3.
- Put all of .v (include TESTBENCH.v) source files and report into same compressed file. (Use your student ID to be the name of your compressed file, EX: 0256065.rar