Computer Organization 2015

Lab 4: Pipelined CPU I

**Due: 2015/05/11 23:59:59**

1.Purpose

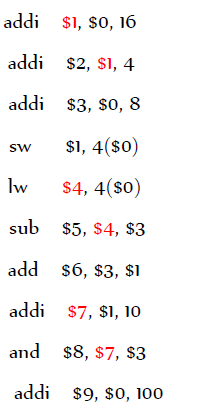
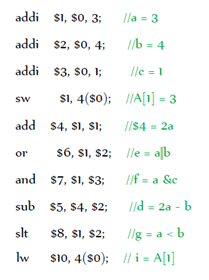
Based on lab3, implement a simple pipeline CPU that can run R-type and I-type instructions.

2.Requirement

* Please use Modelsim or Xilinx as your simulation platform
* It’s a no team assignment. Please attach your names and student IDs as comments in the top of each file. The assignment you upload on e3 must have the form of "student\_ID.rar ".
* Reg\_File[29] represents stack point. Please give an initial value to Reg\_File[29] as 128, others 0
* You must use the Reg\_File.v provided for this LAB.
* You need to implement the following basic instructions: ADD, SUB , AND , OR , SLT , ADDI , LW , SW (60 %)
* “CO\_P4\_TEST1.txt” is a simple testing file and you can verify your design by running the file.
* Some of the Instructions in “CO\_P4\_TEST2.txt” have data dependency , you need to modify the content of the file to get the right answer. Hint: adding NOP instruction between instructions or you can rearrange the ordering of the instruction but without changing the result. You need to hand in your CO\_P4\_TEST2.txt as well. (10%)
* This LAB needs demo. During the demo , TA will ask each of you some question about this LAB or the design. Get prepared! (20%)
* Also, you need to hand in your Report for this LAB.(10%)
* You need to upload your file to E3 before deadline or 10 % off each day

CO\_P4\_TEST1.txt

CO\_P4\_TEST2.txt



3. Pipeline Architecture

