**CO project 1 – ALU**

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1. **Introduction**

In this lab, we are required to implement a ALU with two 32-bit source input, one 4-bit control input, one 32-bit result output and a zero flag output on behavioral level.

1. **Procedure**

I consider using always block which is triggered by the change of ctrl\_i, src1\_i and src2\_i. In the block, I use case statement to decide which branch should be executed according to the value of ctrl\_i. In add and sub section, I treat the input as signed number by using $signed(). Also I consider using signed number in all the comparison sections. By default, I set result\_o to unknown.

1. **Results**

It seems my ALU module can pass all the test cases except the last one. I think it compares unknown value with unknown value, which results in the inequality.

1. **Conclusion**

Since I haven’t learned how to program in Verilog before, I spend a lot of time learning this programming language and getting familiar with the Modelsim environment. I hope my understanding of this assignment and the method of using the test bench is correct.