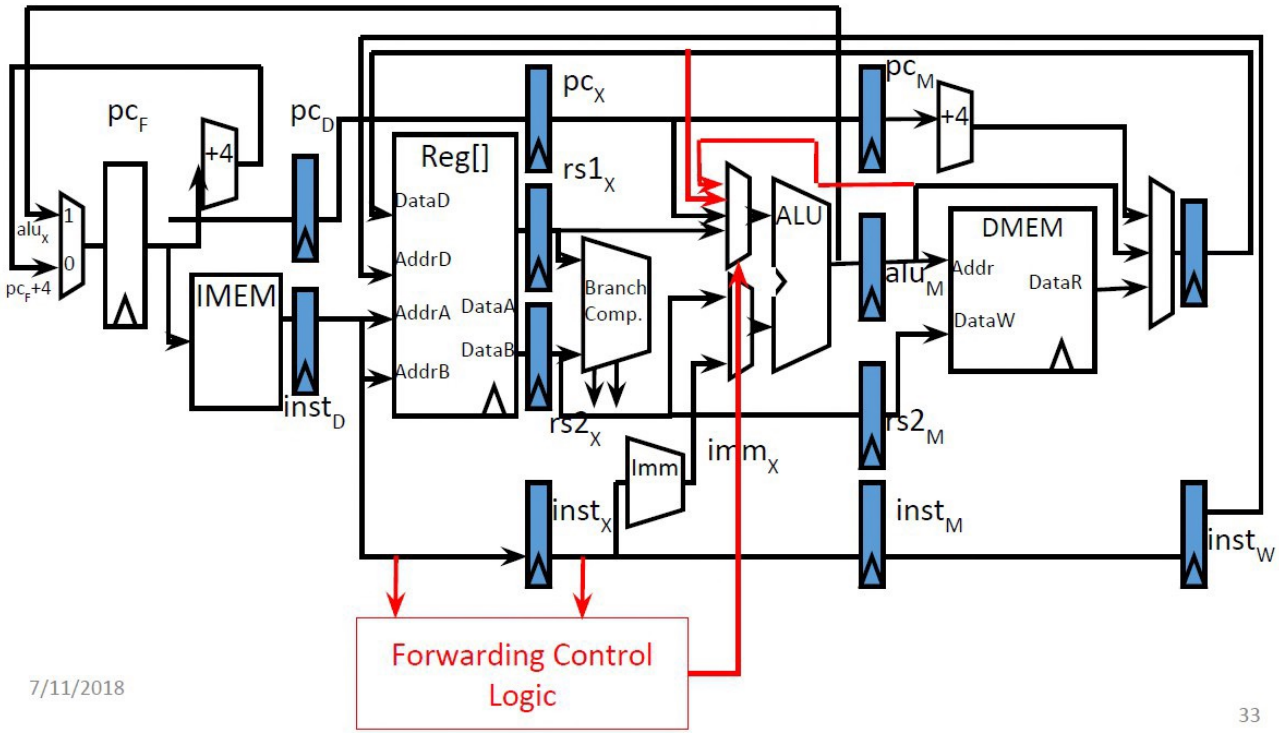
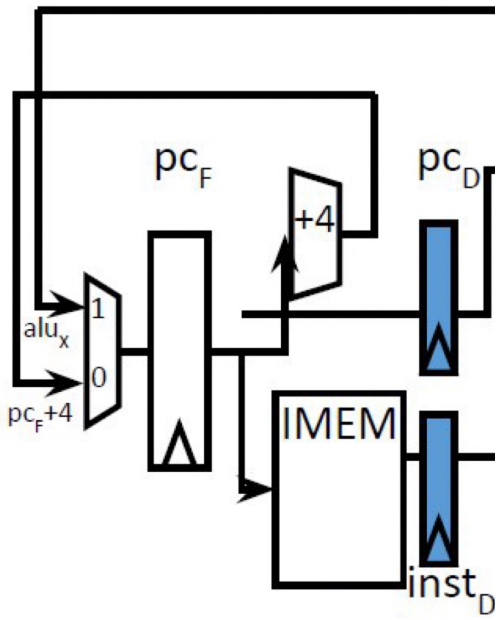

pc_F
+4
pc_D
pc_X
pc_M
+4
Reg[]
DataD
AddrD
AddrA
DataA
DataB
AddrB
rs1_X
ALU
DMEM
Addr
DataR
DataW
alu_M
alu_X
1
0
pc_F+4
IMEM
inst_D
Branch Comp.
rs2_X
rs2_M
Imm
imm_X
inst_X
inst_M
inst_W
Forwarding Control Logic

STAGE 1 fetch



dp out

dp in

stage in

stage out

PC Inc

PC

PCSel

ALU

PCinc

PCEN

IFregEn

EN

PC_IF

PCout

NOP

IFregEn

EN

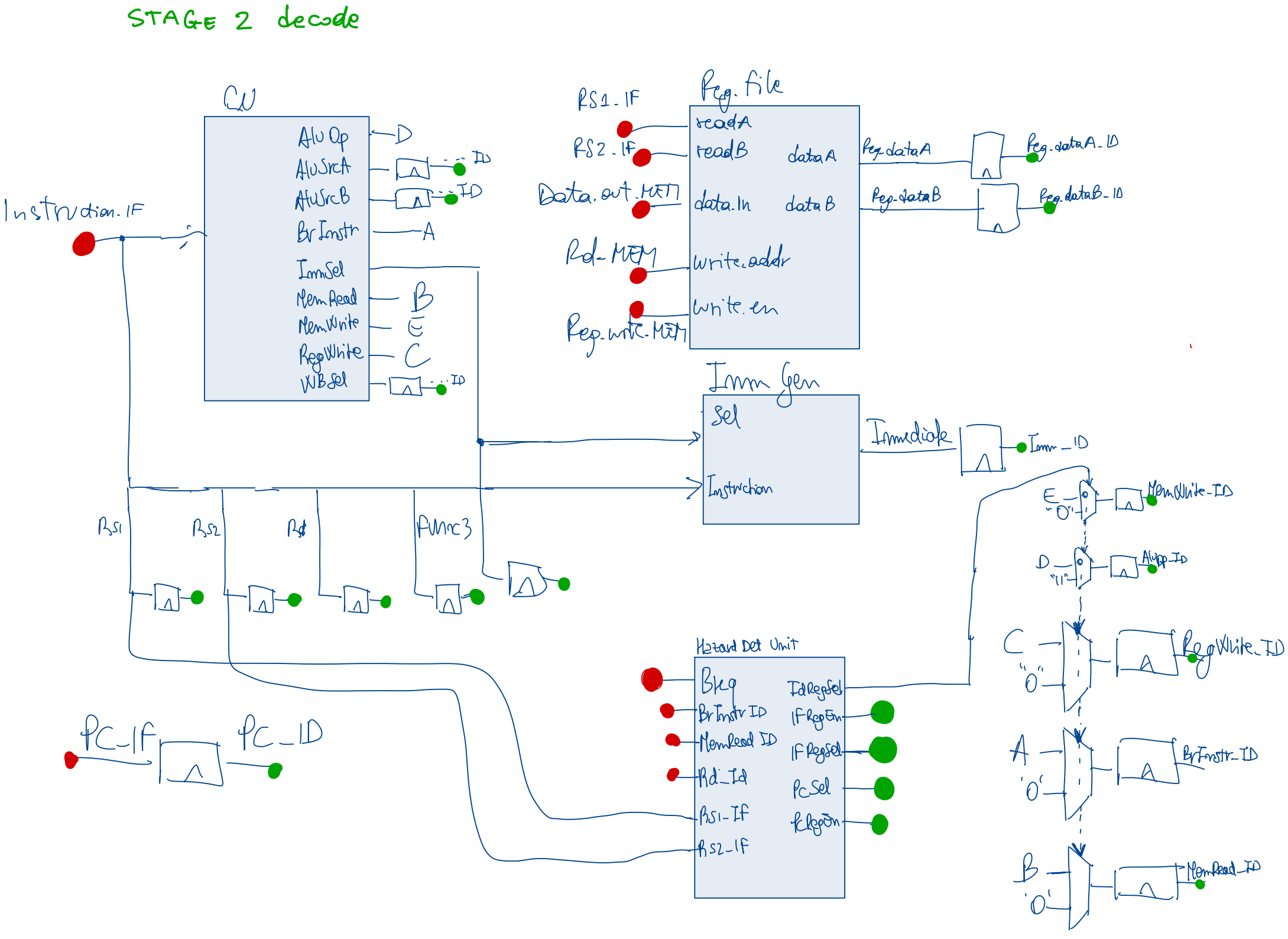
Instruction_IF

Instruction

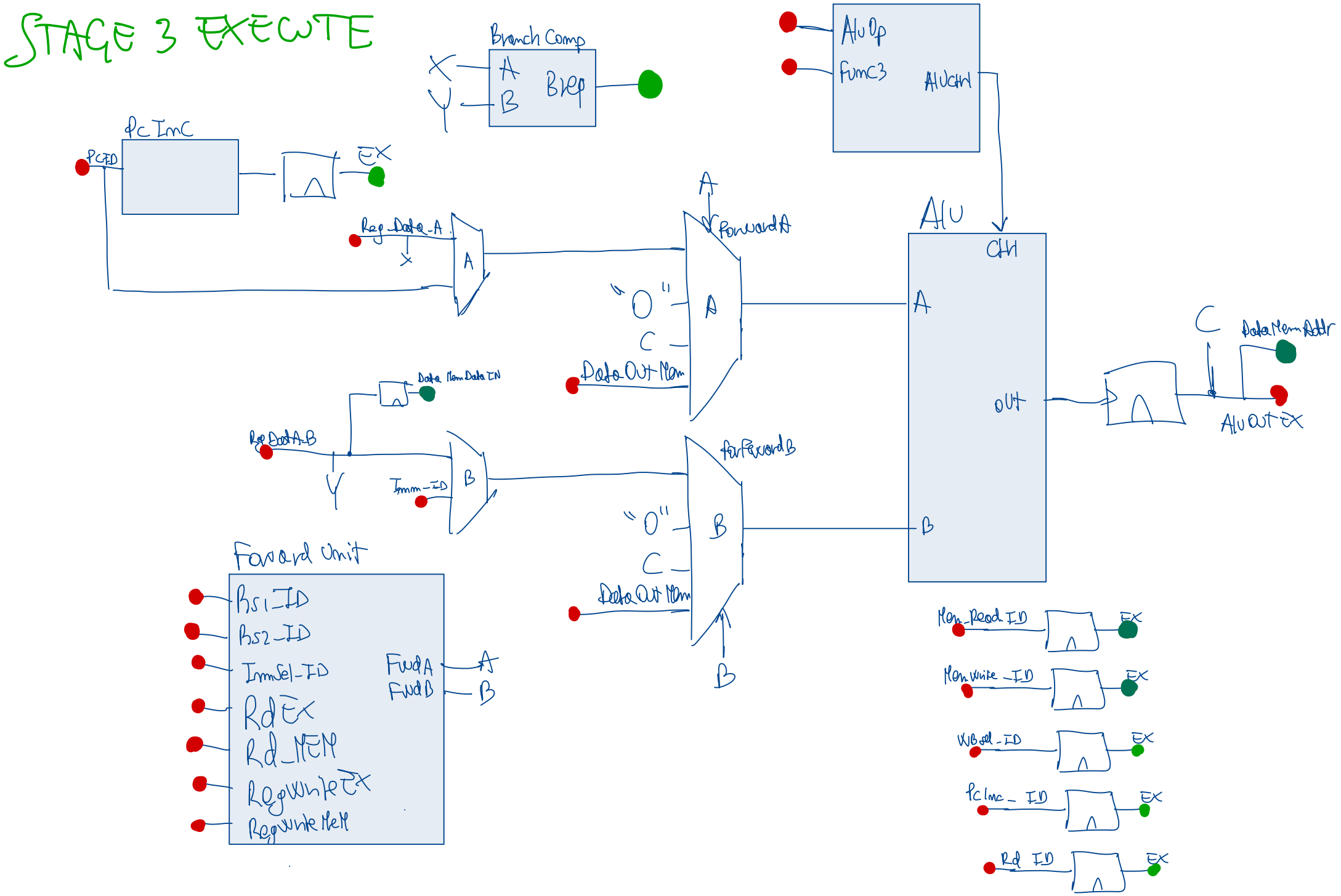
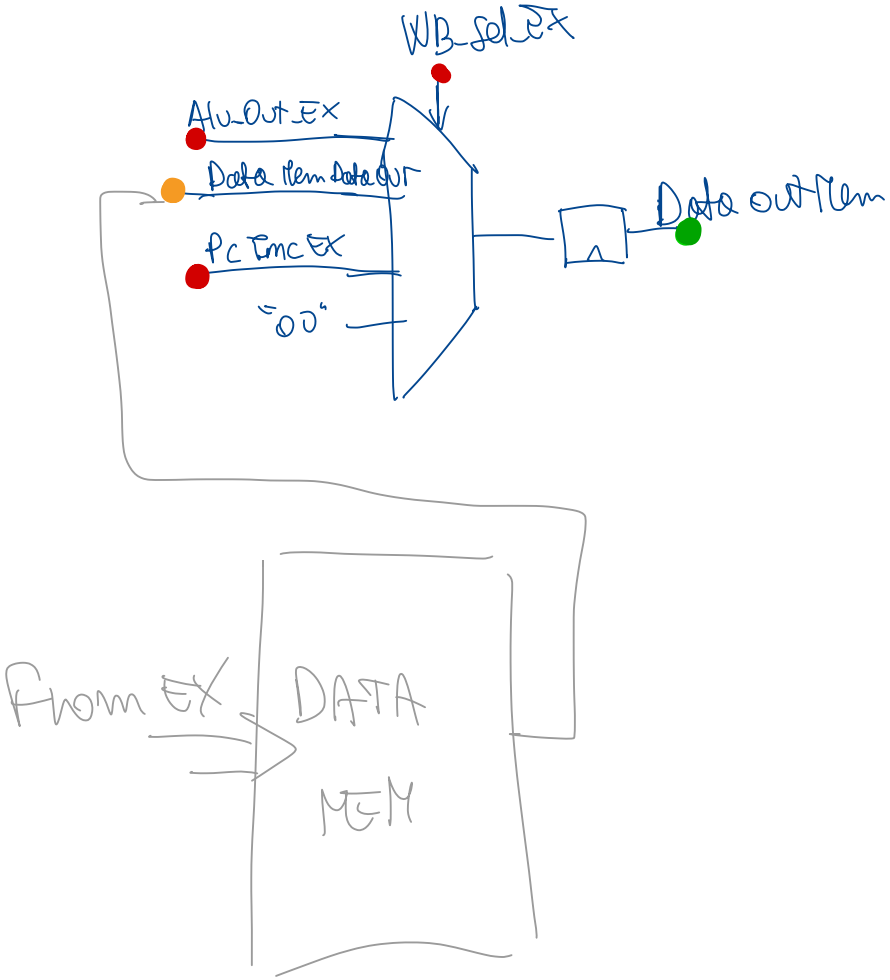
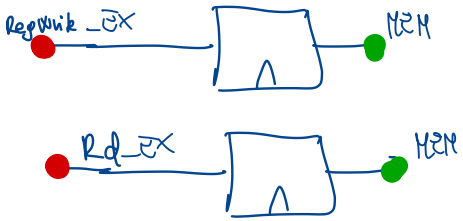
IF_reg_en

INSTR

MEM


STAGE 2 decode
CU
AluOp
AluSrcA
AluSrcB
BrInstr
ImmSel
MemRead
MemWrite
RegWrite
WBSel
ID
A
B
C
Instruction_IF
RS1_IF
RS2_IF
Data_out_MEM
Rd_MEM
Reg_write_MEM
Reg. file
readA
readB
data.In
write.addr
write.en
dataA
dataB
Reg_dataA
Reg_dataB
Reg_dataA_ID
Reg_dataB_ID
Imm Gen
Sel
Instruction
Immediate
Imm_ID
RS1
RS2
Rd
Func3
Hazard Det Unit
Rdq
BrInstr ID
MemRead ID
Rd_Id
RS1_IF
RS2_IF
IdRegSel
IFRegEn
IFRegSel
PcSel
PcRegEn
PC_IF
PC_ID
MemWrite_ID
ALUop_ID
RegWrite_ID
BrInstr_ID
MemRead_ID

STAGE 3 EXECUTE



STAGE 4 MEMORY