
UNIVERSITÀ DEGLI STUDI DI MILANO

INFN
Istituto Nazionale di Fisica Nucleare

# ABBA firmware status and latency correction

ALESSANDRA CAMPLANI – UNIVERSITÀ DEGLI STUDI E INFN MILANO

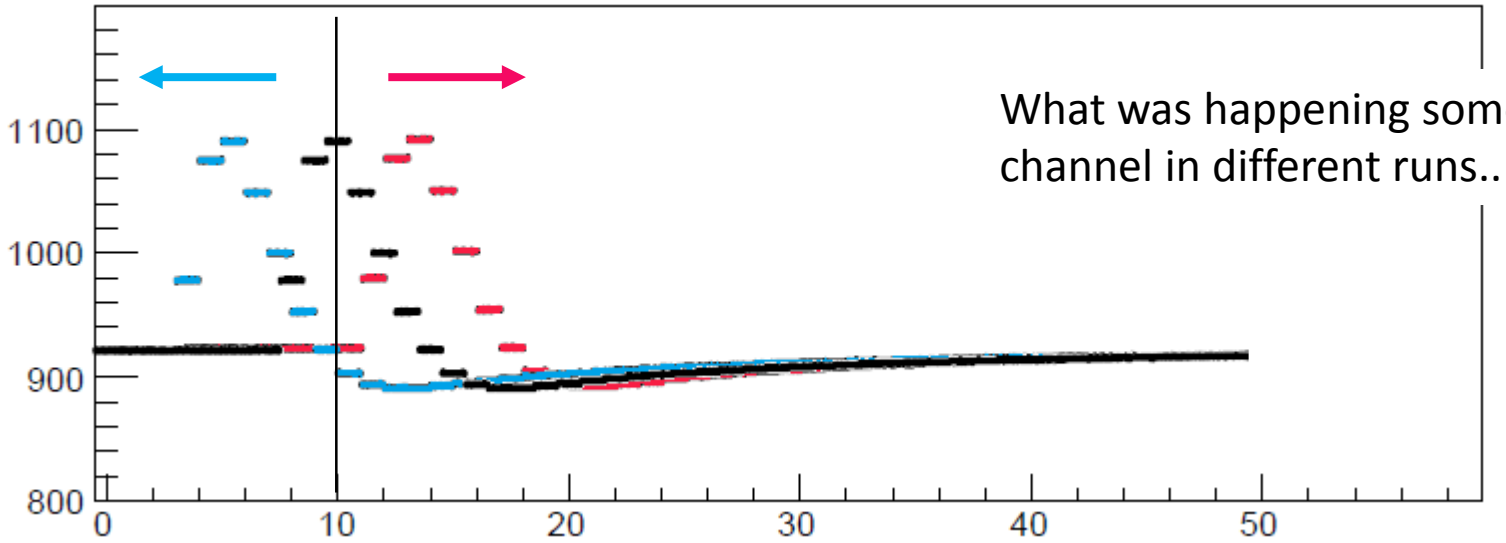
07-03-2017

# Reminder

The peak position of the pulse can be off by 1/2 BC on the same fiber in different runs

- Reason: uncertainty of phase of the hardware transceivers locking after reset

  - **Goal**: have a fixed latency upon fiber locking to avoid “random” misalignments




What was happening sometimes on the same channel in different runs..

# How to improve

Test firmware version for Front FPGA: **v0.98 1**

- Key value: the latency difference between the TTC BCR in ABBA and the LTDB BCR (K-code)
  - Measured by Nicolas DD a long time ago: LAr Week March 2015
    The delay between TTC BCR in ABBA and LTDB BCR is 0x44

- Assuming 0x44 to be the “real” latency value between the two boards, then we can calculate fiber by fiber:
  - $L_{real} - L_{measured}$ = Correction value

  (which could be either positive or negative)

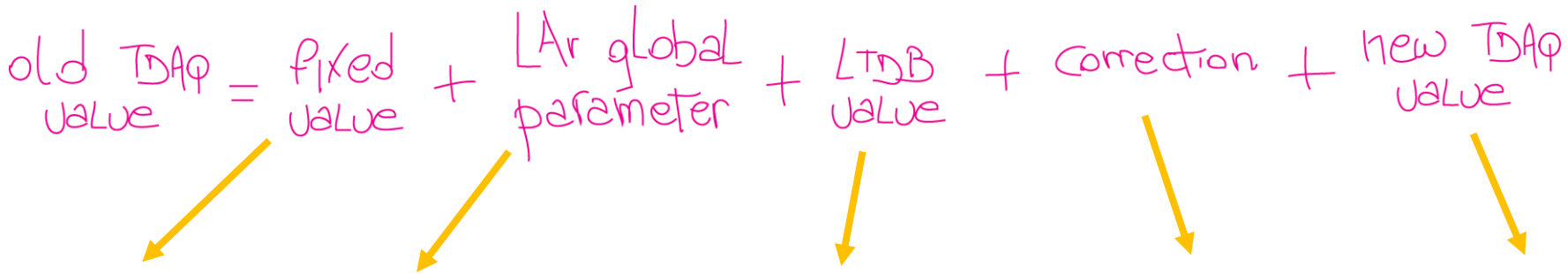
But this is not the end….

# New values

Value set via the TDAQ panel (IGUI) used now (to have the pulse peak at position 20 in the readout window) for:

- Physics BNL = 0x56
- Physics LAL = 0x4e

In the firmware this value will be substituted by this **combination of values**:




Set in the firmware and calculated to comply the LAr global and the new TDAQ value: it will be -46

For example, 104 for LAr Physics, to be set through TDAQ

Set in the firmware, it will be 8 for BNL LTDB and 0 for LAL LTDB, according to the latency between the two boards

Set in the firmware, it is the value explained previously

To have the pulse at position 20 in the readout window, this value will be set directly to 20 in the panel

# Firmware and TDAQ

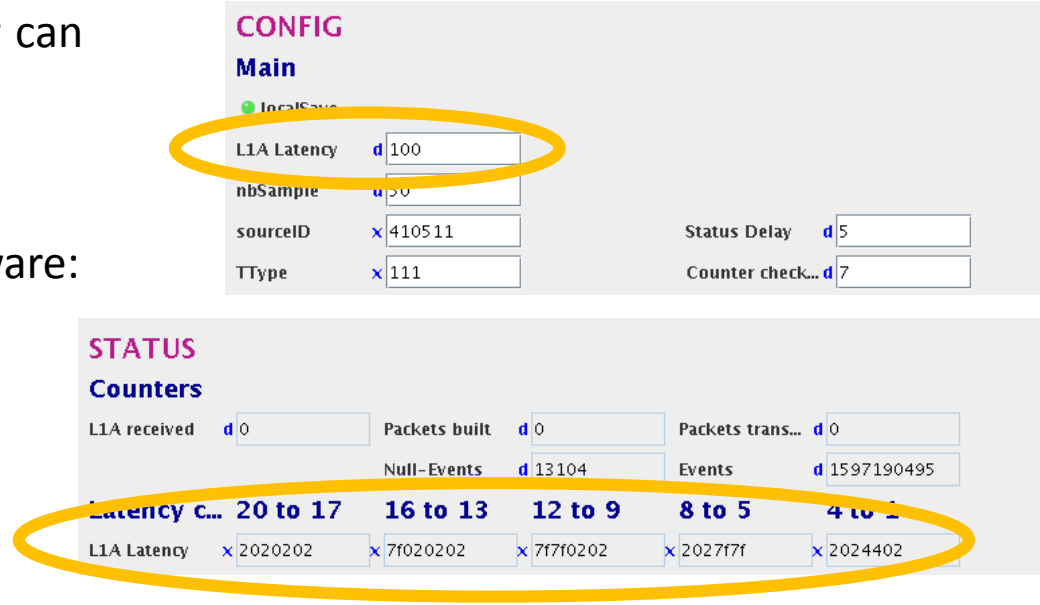
- This **correction** is applied only to FPGAs connected to BNL LTDB.

For LAL LTDB: phase is not defined, can happen that any fiber can take any (of 9 possible) phases of the K-code.

- No correction applied to the LAL data.

- *Abba package* has some **new features** to use the new firmware:

- L1A Latency (which will need some more improvements)
  - Split the value into two:
    - LAr global parameter
    - New TDAQ value (pulse peak position)
- Latency correction monitoring



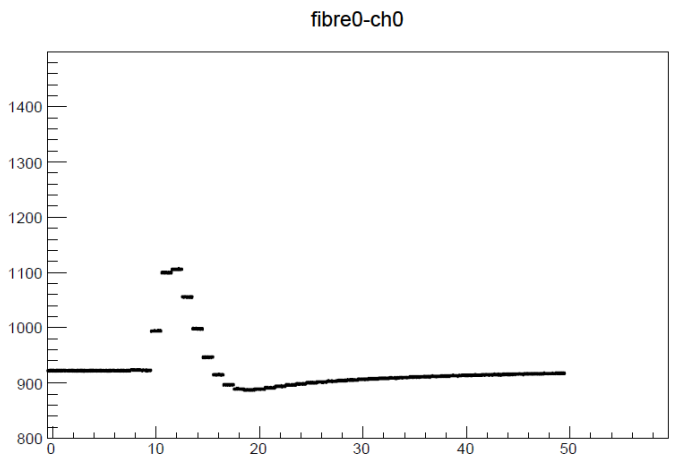

- **Standalone tool** has been updated as well

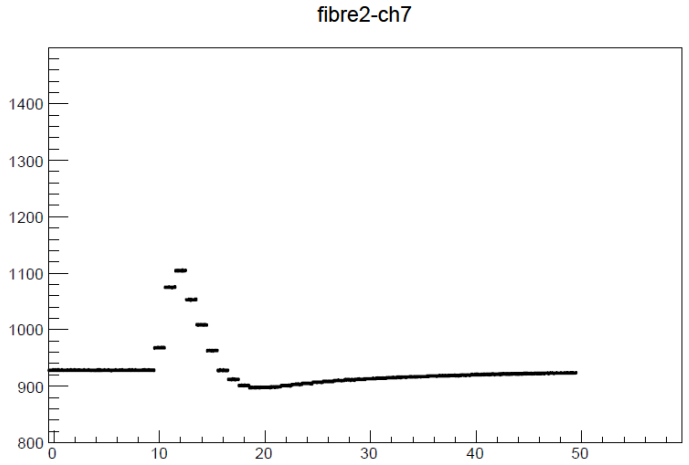
# Calibration runs 316873

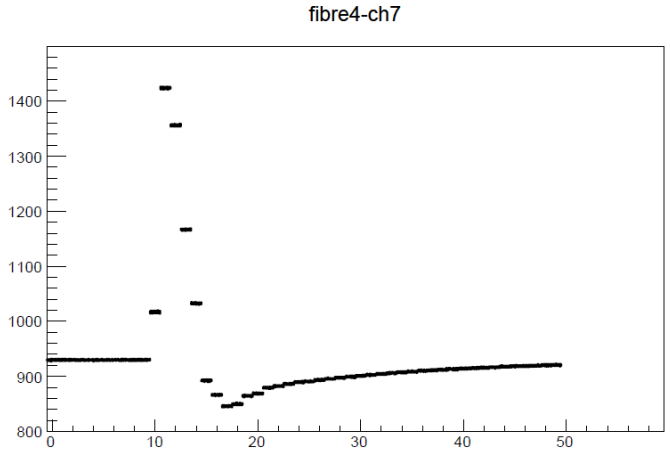
1 March 2017 - time 09:18

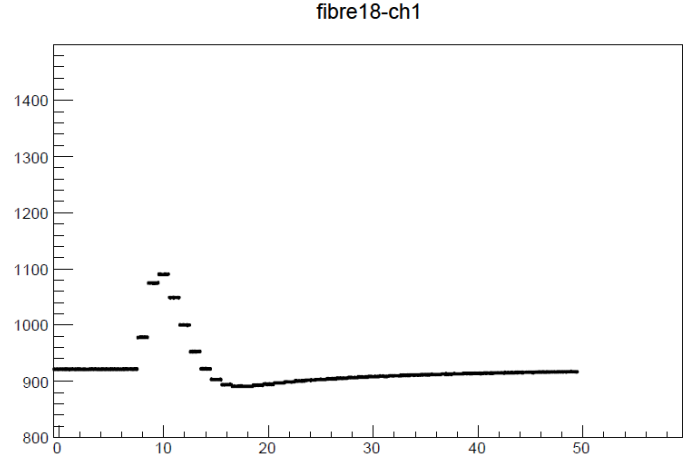
FPGA 19:2

Latency value se to 100



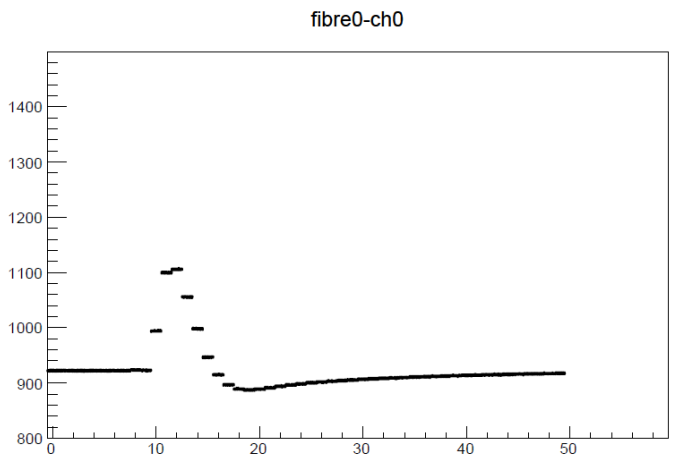



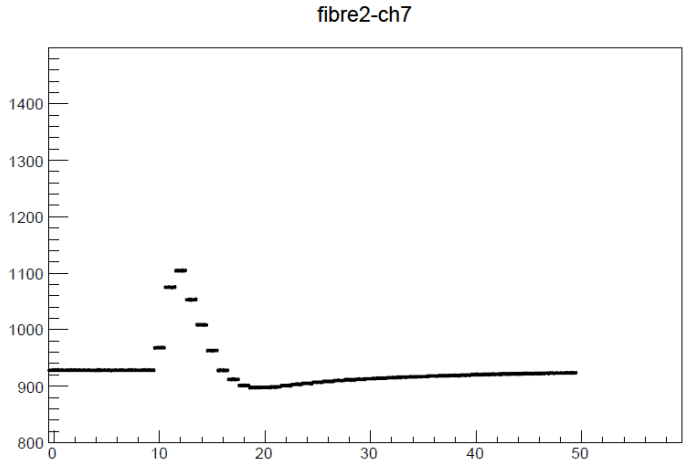
# Calibration runs 316957

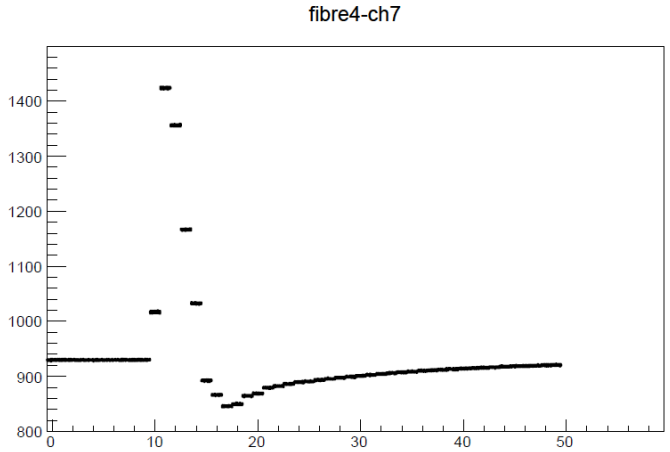
1 March 2017 - time 18:47

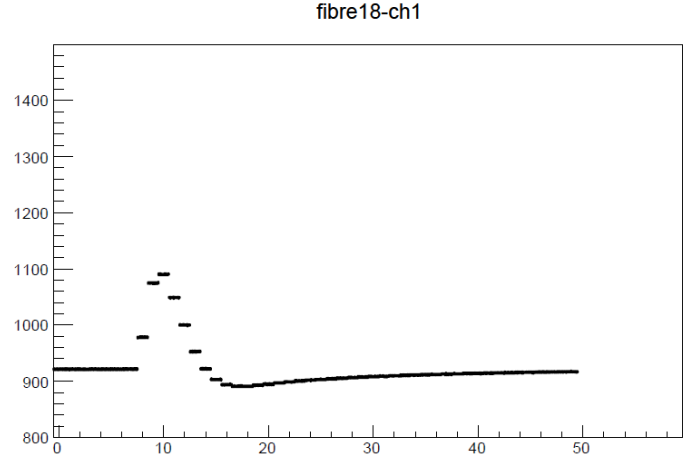
FPGA 19:2

Latency value se to 100



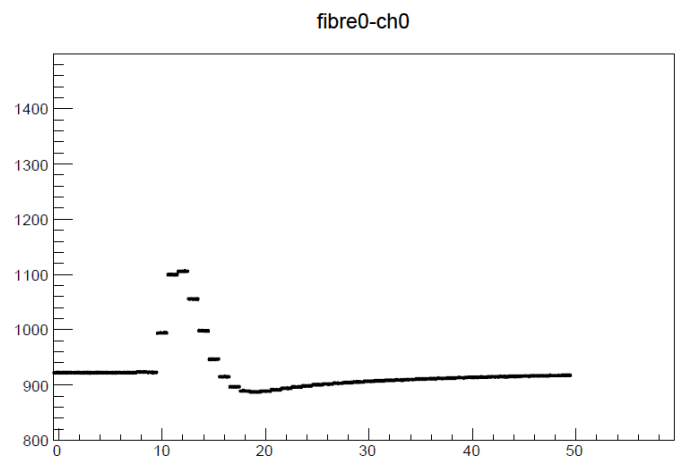
# Calibration runs 317019

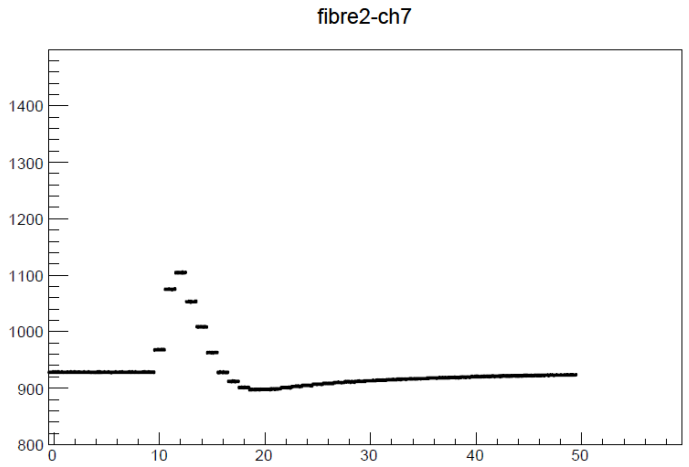
2 March 2017 - time 12:22

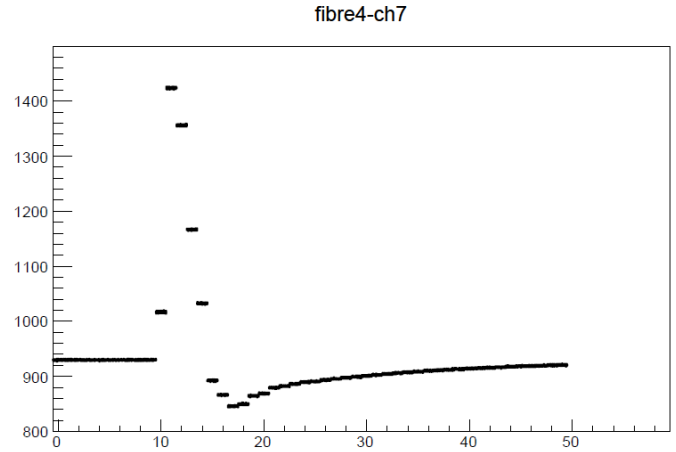
FPGA 19:2

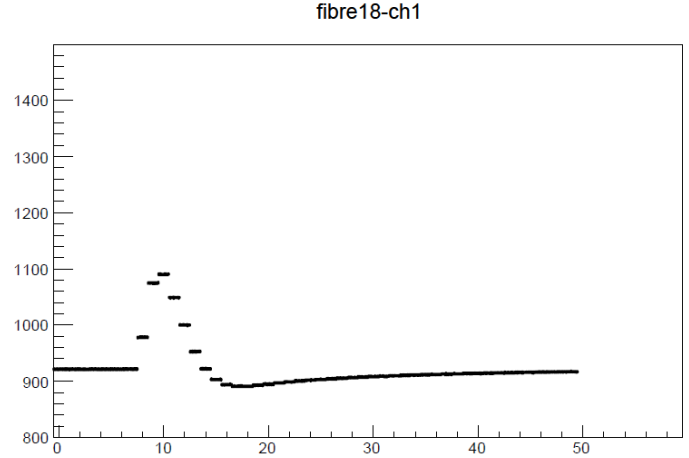
Latency value se to 100

FPGA 20:2 has the very same nice behaviour.



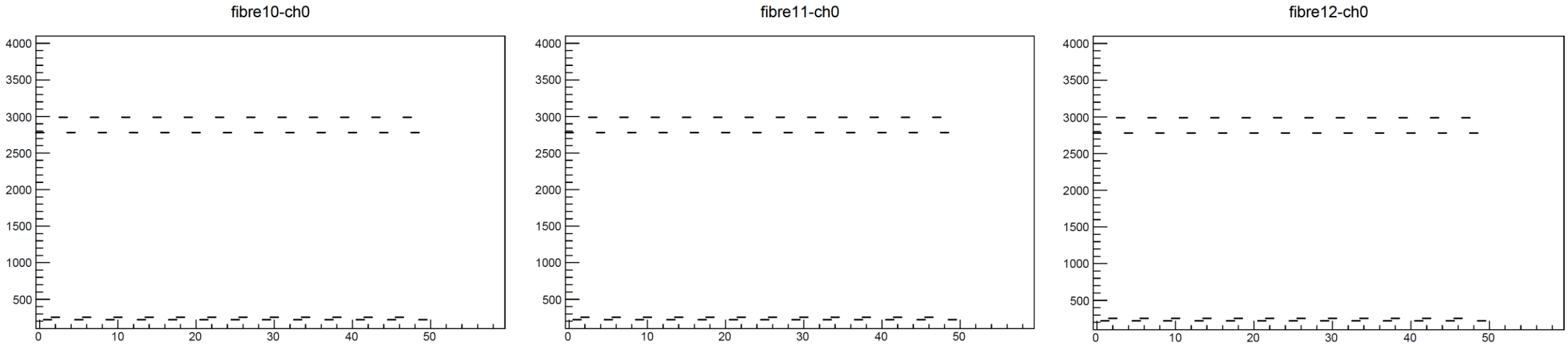



# Unlocked fibers pattern

Another important update in the firmware:

- when a fiber is unlocked now **a fixed pattern** is appearing.

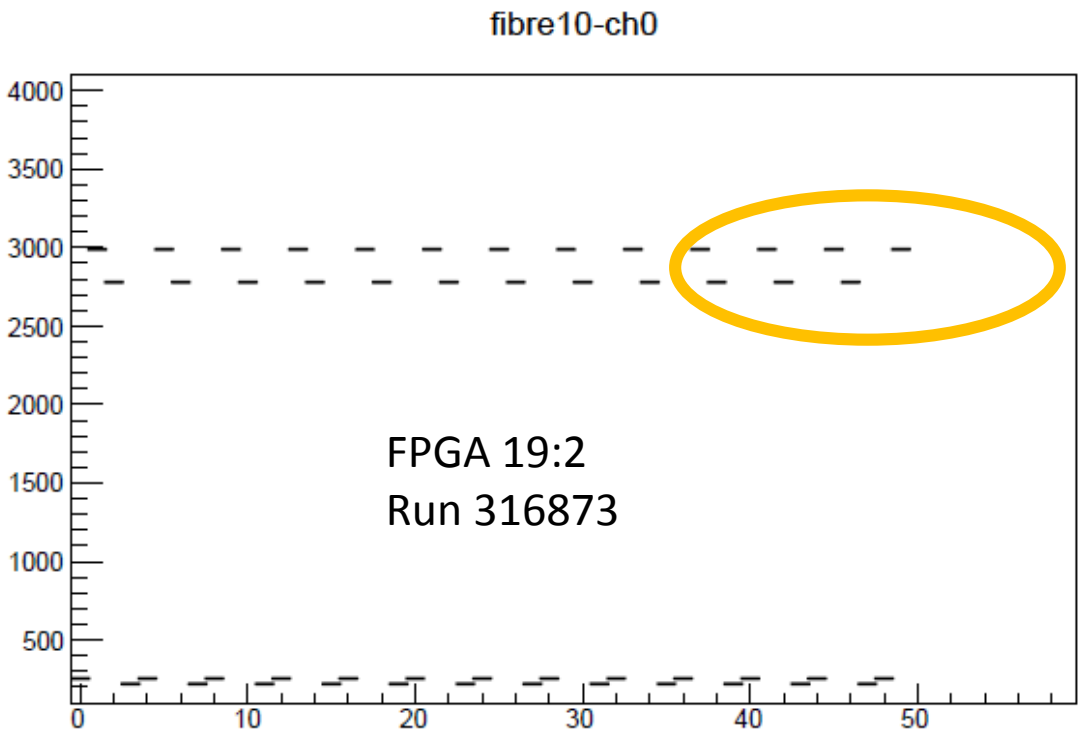
Four words are rotating: x"BAD", x"ADC", x"0DD", x"0FF"

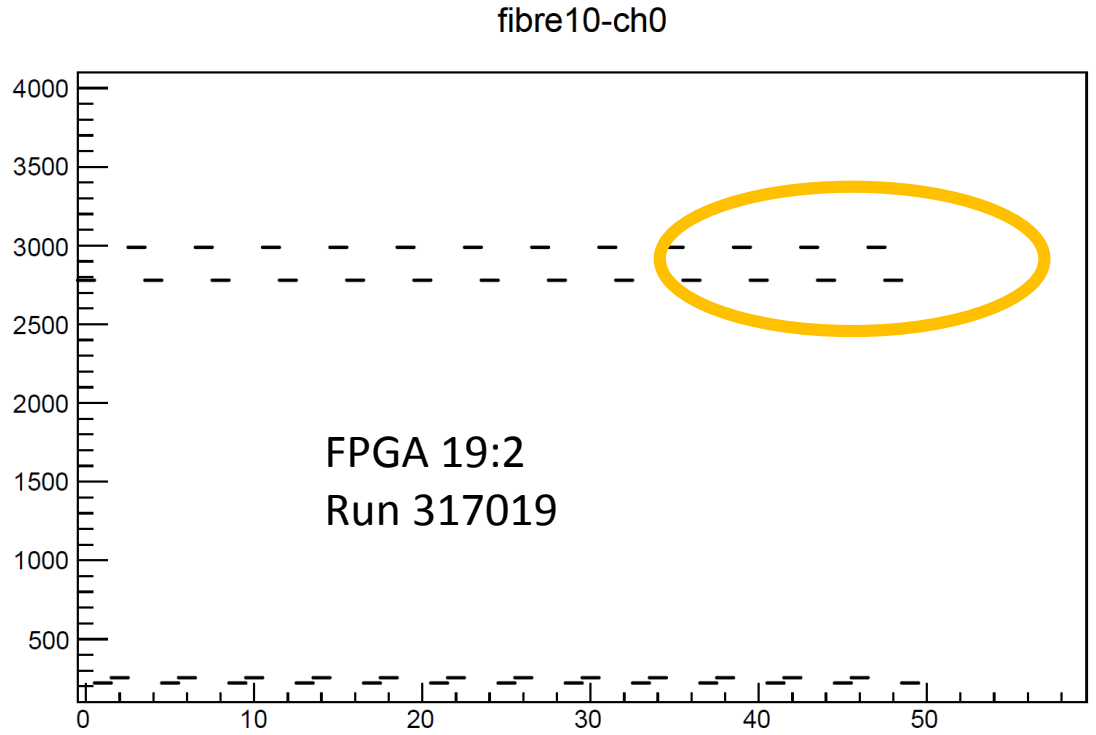



FPGA 19:2 - Run 317019

# Unlocked fibers pattern(2)

- Still a bit different because not yet properly aligned (known phase misalignment)
  - ➢ But this **is undestood and going to be corrected** as well



# Conclusion

- **New test firmware Front FPGA** (v0.98 1) is ready and has been tested in USA15
  - The official version will be released soon

- **Latency correction** per fiber has been implemented
  - Showing very good result
    - Every time the same behaviour on the same fiber (from different runs)
    - Correction is calculated and applied only on BNL data
  - Not applied on LAL data (missing hardware piece to have a fixed latency phase)

- **Defined pattern** for unlocked fibers has been implemented
  - Applied to both BNL and LAL data
  - Alignment of the pattern will be done soon