



UNIVERSITÀ  
DEGLI STUDI  
DI MILANO



# ABBA firmware status

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# Firmware version

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During the last Upgrade Week, firmware versions presented:

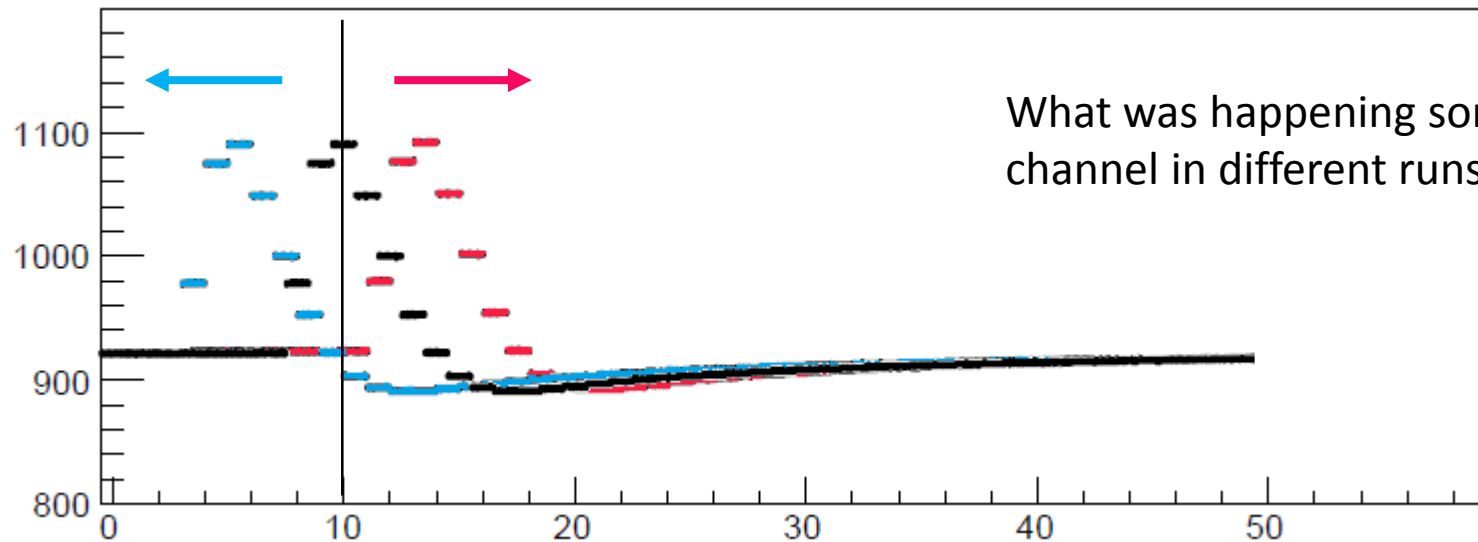
- **Front FPGA: v0.97\_1 (= v0.98)**  
Implemented protection against early readout.  
Simulation files for front FPGA firmware are now available.
- **Back FPGA: v0.70**  
Improved communication between front and back FPGAs adding ID for packet tracing.  
This version requires v0.97 of the Front FPGA firmware.

Used for the last data taking.

# Latency issue

The peak position of the pulse can be off by  $1/2$  BC on the same fiber in different runs

- Reason: uncertainty of phase of the hardware transceivers locking after reset
- **Goal:** have a fixed latency upon fiber locking to avoid “random” misalignments



# Improvements in Front FPGA

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## Front FPGA test version: v0.98 1

- Key value: the latency difference between the TTC BCR in ABBA and the LTDB BCR (K-code)
  - Measured by Nicolas DD a long time ago: [LAr Week March 2015](#)  
The delay between TTC BCR in ABBA and LTDB BCR is 0x44
- Assuming 0x44 to be the “real” latency value between the two boards, then we can calculate fiber by fiber:
  - $L_{\text{real}} - L_{\text{measured}} = \text{Correction value}$   
(which could be either positive or negative)

# New values

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Value set via the TDAQ panel (IGUI) used now (to have the pulse peak at position 20 in the readout window) for:

- Physics BNL = 0x56
- Physics LAL = 0x4e

In the firmware this value will be substituted by this **combination of values**:

$$\text{old TDAQ value} = \text{fixed value} + \text{LAR global parameter} + \text{LTDB value} + \text{correction} + \text{new TDAQ value}$$

Set in the firmware and calculated to comply the LAR global and the new TDAQ value: it will be -46

For example, 104 for LAR Physics, to be set through TDAQ

Set in the firmware, it will be 8 for BNL LTDB and 0 for LAL LTDB, according to the latency between the two boards

Set in the firmware, it is the value explained previously

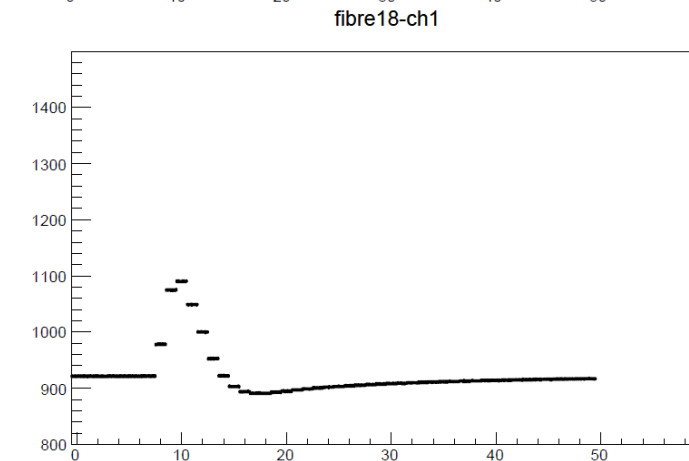
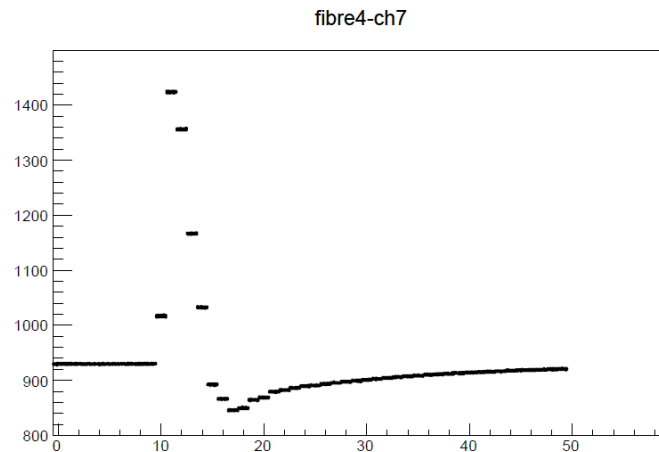
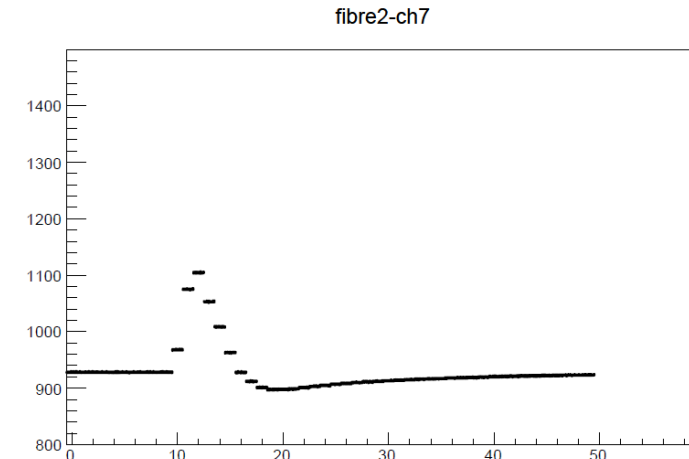
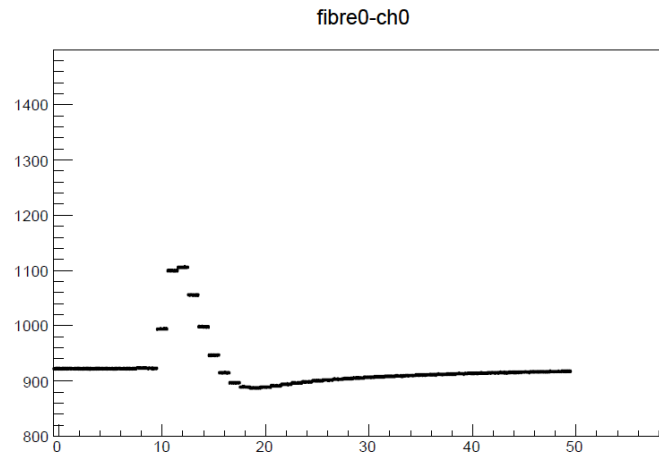
To have the pulse at position 20 in the readout window, this value will be set directly to 20 in the panel

# Calibration runs 316873

1 March 2017 - time 09:18

FPGA 19:2

Latency value se to 100



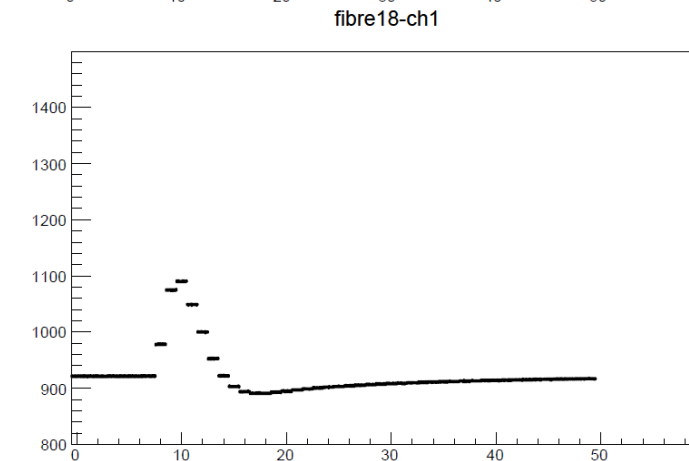
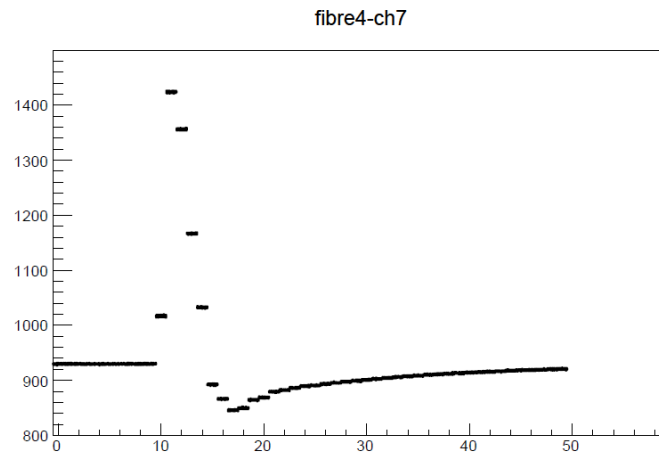
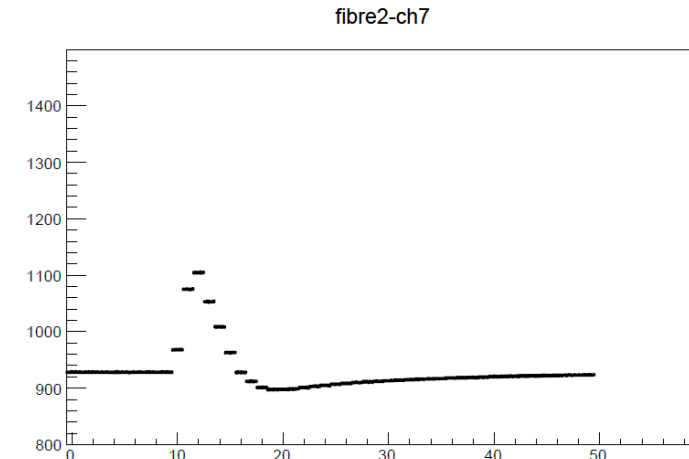
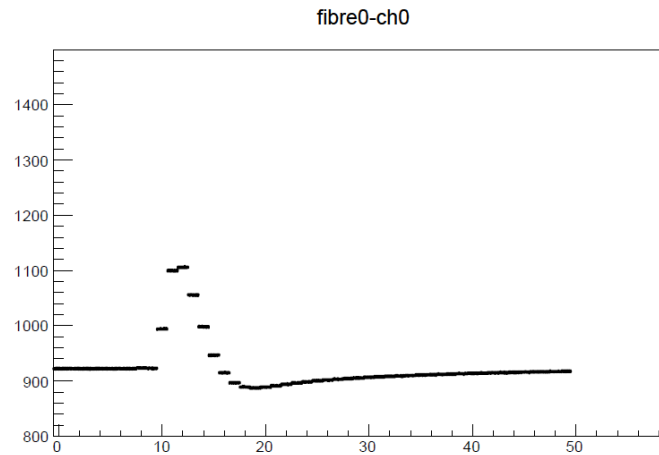
# Calibration runs 317019

2 March 2017 - time 12:22

FPGA 19:2

Latency value se to 100

FPGA 20:2 has the very same  
nice behaviour.

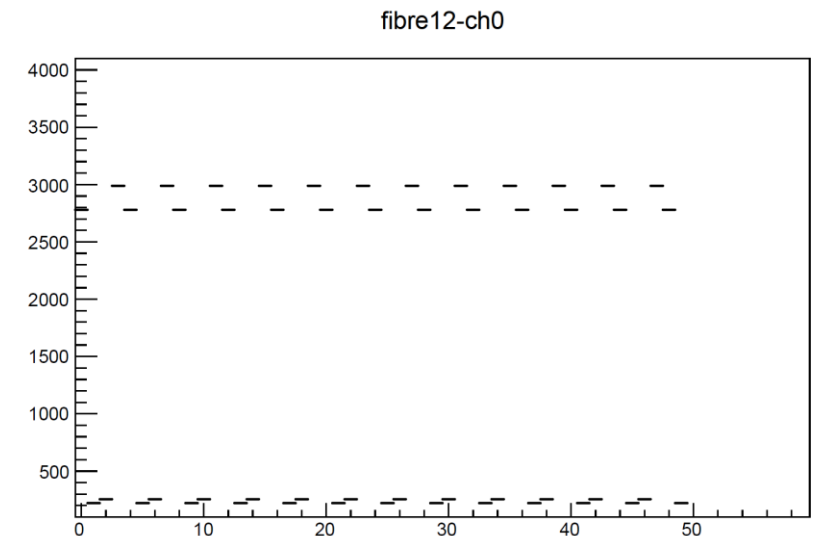
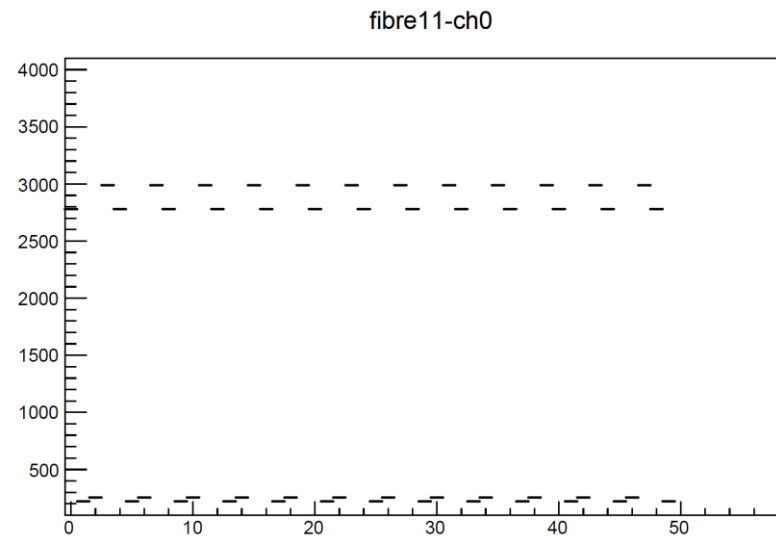
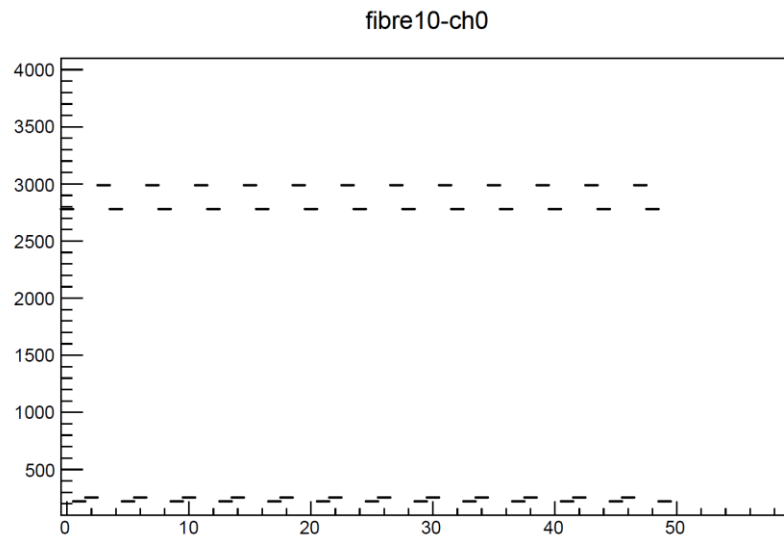


# Unlocked fibers pattern

Front FPGA test version: **v0.98 1**

➤ when a fiber is unlocked now a **fixed pattern** is appearing.

Four words are rotating: x"BAD", x"ADC", x"0DD", x"0FF"



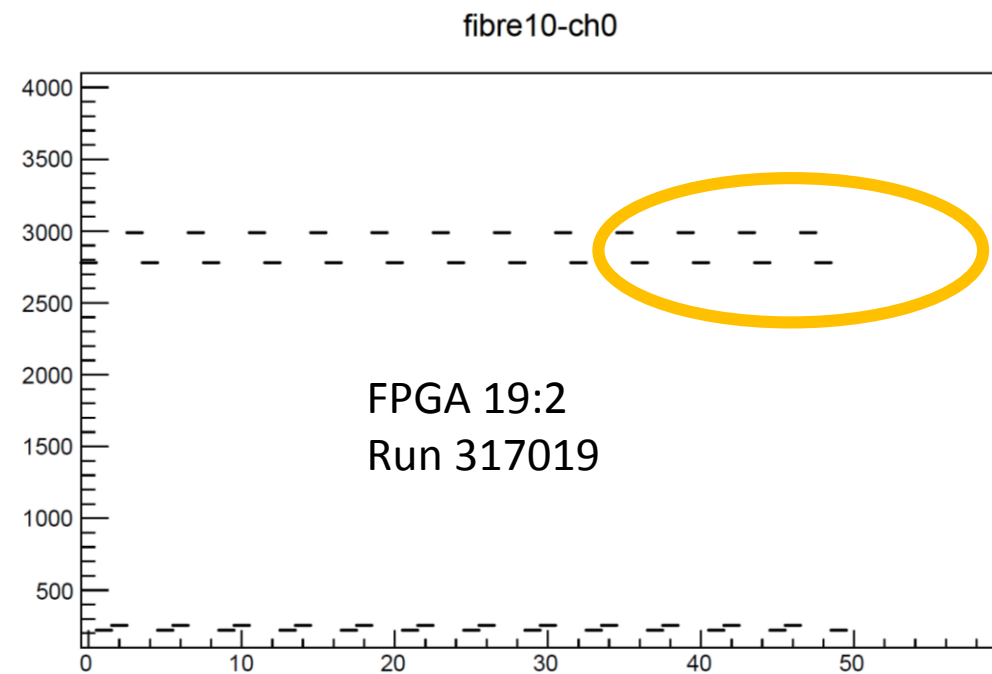
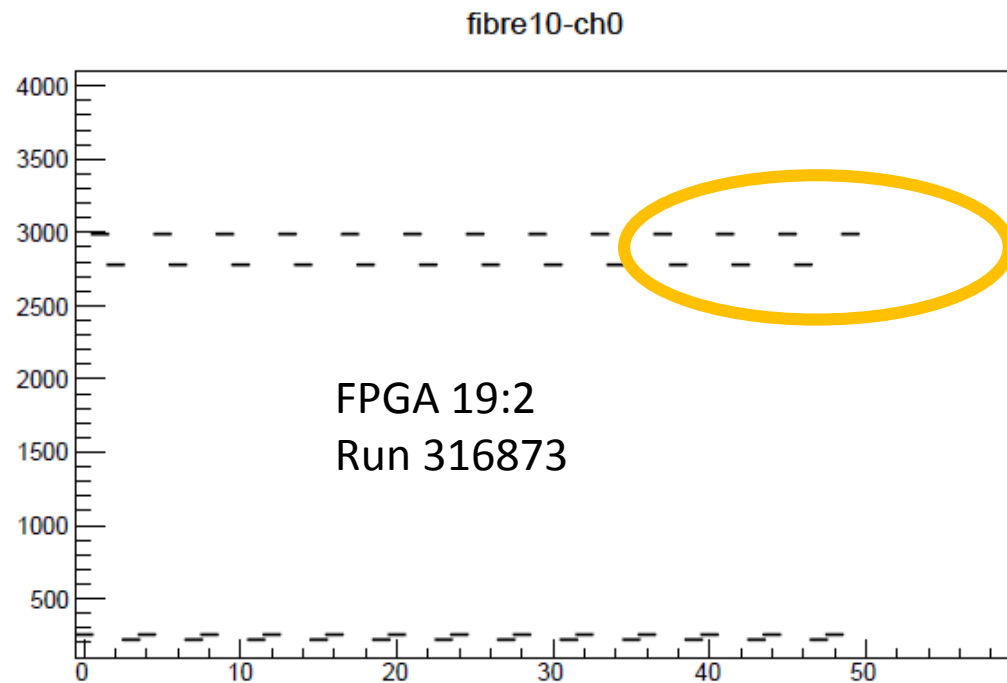
FPGA 19:2 - Run 317019



# Unlocked fibers pattern(2)

**Front FPGA test version: v0.98\_2**

- Not properly aligned (known phase misalignment)
  - Under improvement



# Back FPGA firmware

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- Now that the ID tracing is implemented between Front and Back FPGA:
  - It can be possible to monitor and count the packets lost between the Front and Back FPGAs
    - To monitor we need registers and IPbus in the Back FPGA.  
A basic implementation is already there but something more is needed.
    - Re-use the IPbus code already implemented in the Front FPGA firmware  
(Philipp Horn is working on this implementation)
- Updated MAC addresses for USA15 boards and both MAC and IP addresses in EMF boards

# Conclusion

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- **New test firmware Front FPGA (v0.98 1)** is ready and has been tested in USA15
  - Version v0.98\_2 is under test
- **Latency correction** per fiber has been implemented
  - Showing very good result
    - Every time the same behaviour on the same fiber (from different runs)
    - Correction is calculated and applied only on BNL data
  - Not applied on LAL data (missing hardware piece to have a fixed latency phase)
- **Defined pattern** for unlocked fibers has been implemented
  - Applied to both BNL and LAL data
  - Alignment of the pattern study
- **Work ongoing for new Back FPGA firmware**

Backup