ABBA firmware (and partition) status

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Improvements in the firmware

Last presented version:

- Front FPGA: **Version v0.96c**
- Back FPGA: **Version v0.69a1**

New versions:

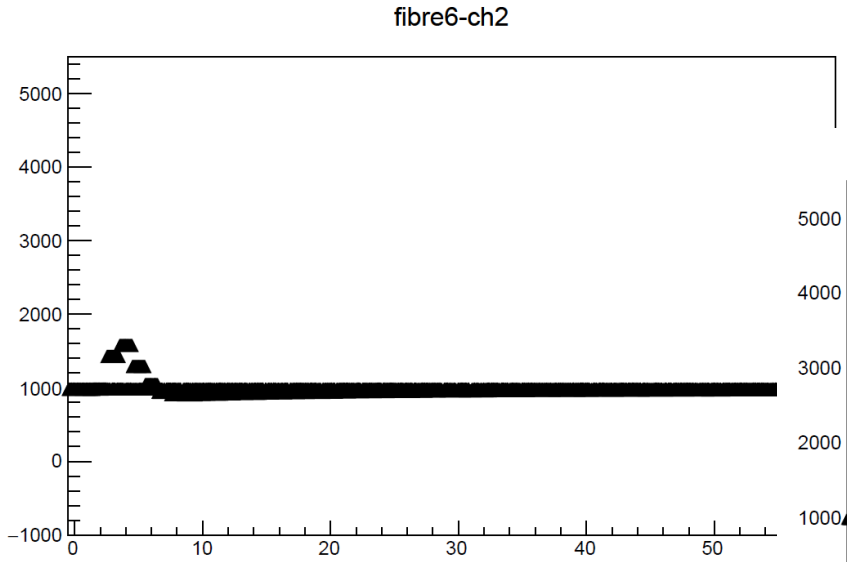
- Front FPGA: Version v0.96c1/ v0.96c2
  - merging and reworking some common vhdl files (Thanks to Philipp!)
- Front FPGA: **Version v0.96d**
  - Released version after tests in EMF
  - Tested at EMF, but not applied yet in USA15 (same functionality of v0.96c)

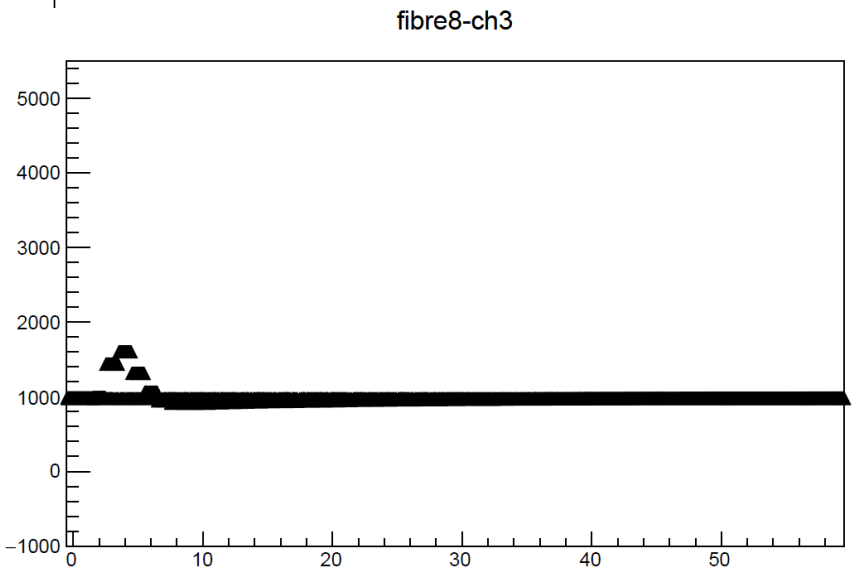
- Back FPGA: Version v0.69a2
  - Again, merging and reworking some common vhdl files (Re- thanks to Philipp!)
- Back FPGA: **Version v0.69b**
  - Released version after tests in EMF
  - Tested at EMF, but not applied yet in USA15 (same functionality of v0.69a)

Tests for the new firmware in EMF

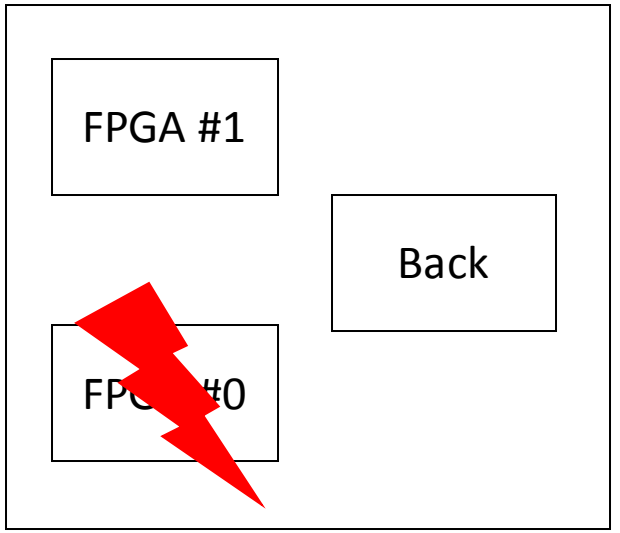
The new firmware version has been tested in EMF, taking some calibration runs.
One FPGA (remained) and used for this purpose.

The pulse is still here! ☺





IP 168.192.10.4



Some more details: EMF run 303830

- high ramp
- #events 1000
- #sample 60
- latency 0x45

Latency settings

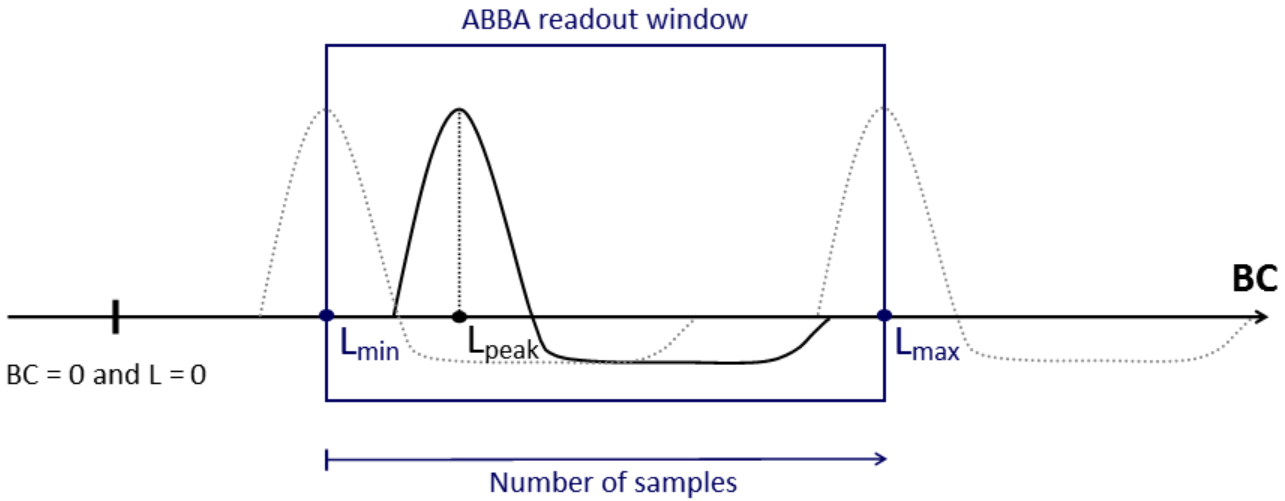
Some calibration runs, with different latency seettings, have been taken in USA15.
For more details you can look here.

The position of the pulse (L_{peak}) has been checked for each run (thanks to Adriana!).

The test confirmed that: a shift of 1 BC corresponds to a shift of 1 unit for the latency value.
So for example from an initial setting of 0x56 (86 in decimal):

- to shift the pulse 10 BC to the right: increase the latency setting by 10, hence set it to 0x60 (96 in decimal)
- - to shift the pulse 10 BC to the left: decrease the latency setting by 10, hence set it to 0x4C (76 in decimal)

Furthermore, **the change in the number of samples doesn't** modify the pulse position in the readout window.
The number of samples moves the right end of the readout window: the left side of the window (L_{min}) is fixed, while the right side (L_{max}) is varied by modifying this value.



System latency differences

The latency settings correspond to a specific position in the readout window, but this position can be different depending on the hardware chain.

For the following different scenarios, the very same latency setting will show up the pulse in different positions:

- **Physics runs vs. calibration runs in USA15**

  The difference between the pulse peak in physics runs and calibration runs in USA15 is of ~10 BC:

  $L^{Phy}_{peak} + 10\ BC = L^{Calib}_{peak}$

- **BNL LTDB vs. LAL LTDB in USA15**

  The difference between the pulse peak from the BNL LTDB and from the LAL LTDB in USA15 is of ~8 BC:

  $L^{BNL}_{peak} + 8\ BC = L^{LAL}_{peak}$

- **Calibration in EMF vs. calibration in USA15**

  The difference between the pulse peak in calibration runs in EMF and in USA15 is of ~15 BC:

  $L^{EMF\text{-}Calib}_{peak} + 15\ BC = L^{USA15\text{-}Calib}_{peak}$

Now documented in the Twiki !!

System latency now

BNL LTDB vs. LAL LTDB in USA15

The difference between the pulse peak from the BNL LTDB and from the LAL LTDB in USA15 is of ~8 BC:
BNL_{peak} + 8 BC = LAL_{peak}

- **Latency settings have been changed** to have all the pulses (of ~ 30 samples) recorded with ABBA starting at around sample 10 (the peak will be at sample 12).

The two different LTDBs now have specific settings (here all the details):
- **0x44 for LAL LTDB** (FPGAs 18:2 and 19:1)
- **0x4d for BNL LTDB** (FPGAs 19:2 and 20:2)

Front End issue

- **On July 12** first issue with FE (during the calibration runs)
  - BNL LTDB links all unlocked: issue solved using some python scripts provided by BNL group

- **On July 15** again the same issue (during the latency setting change)
  - BNL LTDB links again all unlocked: this time the python scripts didn't work
  - Most of LAL LTDB links were locked

- **On July 18** the situation was not improving
  - BNL LTDB was still unlocked
  - Most of LAL LTDB links unlocked. Tried reconfiguration of LTDB with some scripts (already tested and working) provided by Stefan Simion: configuration completely failed.
  - All the LTDB links were unlocked

  - **FINALLY SOLVED!**
    - BNL LTDB - After re-powering the GLIB card, the python scripts were working again
    - LAL LTDB - Stefan stopped the monitoring of the link status: this was causing a conflict with the reconfiguration

All the details here, here and here

Conclusion and outlook

- **New firmware versions (front and back):**
  - Merging and reworking some common vhdl files
- **Latency issue solved**
  - Latency: found a fine position for the pulse fot both LTDBs and finally documented on the Twiki
- **FE issues solved**
  - After re-powering GLIB card and reconfiguration of BNL LTDB: link status is ok
  - After stopping the monitoring of the LAL LTDB link status and after its reconfiguring: link status is ok