Status of LAr Phase-I Upgrade

ATLAS Week – 16 FEBRUARY 2017

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On behalf of the LAr Phase 1 group

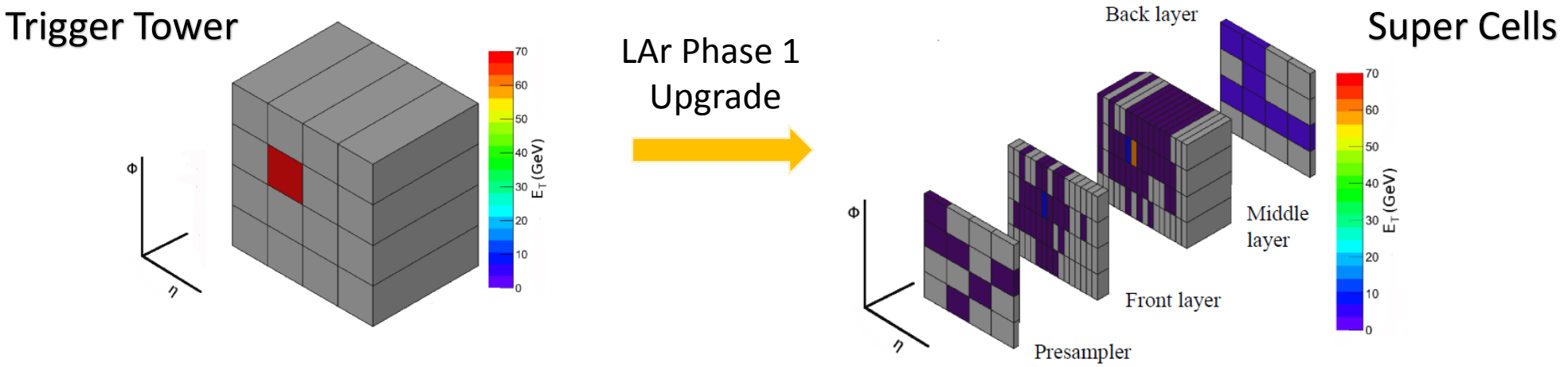
Outline

- Introduction
- LAr Phase-I Upgrade Project
  - LAr Demonstrator
  - Baseplane and LSB
  - Front End: LTDB
    - ASICs
    - Development
  - Back End: LDPS
    - AMC
    - Carrier
- Summary

Introduction

Calorimeter Upgrade

LAr Phase-I upgrade: **new calorimeter trigger electronics** with increased granularity and functionality for LAr calorimeter level 1 trigger



Trigger Tower to Super Cells:

- Granularity increased 10 times per each trigger tower
- Provided information for each calorimeter layer for the full η range
- Finer segmentation in the front and middle layers of the EM barrel and endcap
- Higher resolution and shower information

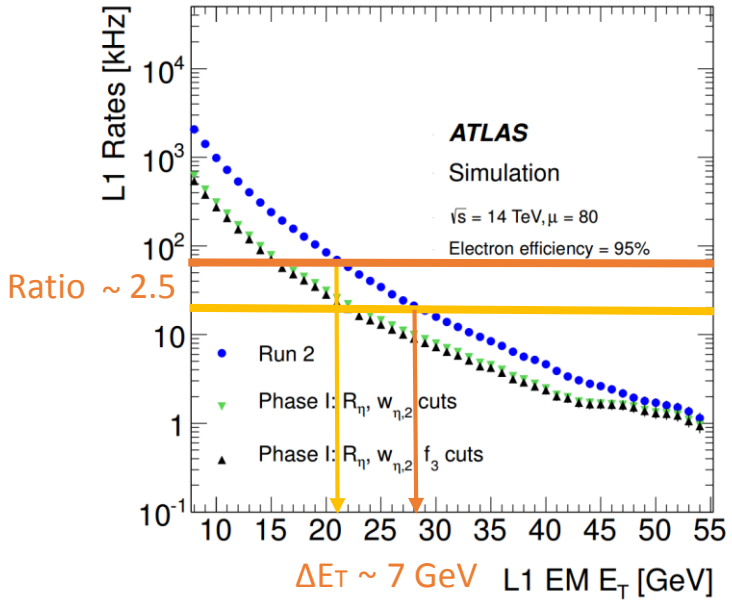
Motivation and strategy

- Main goals: deal with the **luminosity increase,** maintaining a **low-pT lepton threshold** and keeping the **same trigger bandwidth**

With the new Phase-I electronics:

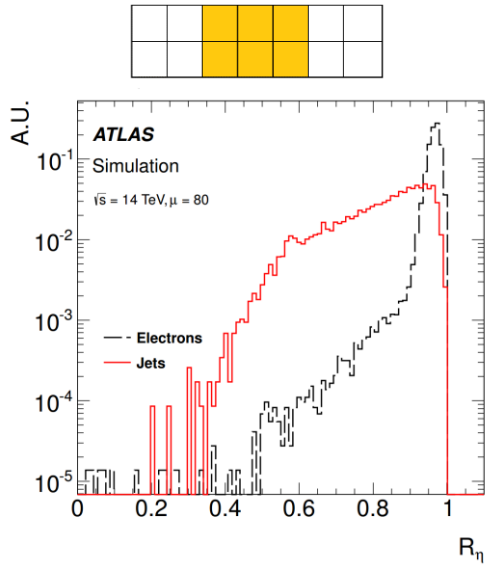
- Make use of **shower shape variables**: a more sophisticated rejection of jet backgrounds

- **Level-1 threshold** for a given bandwidth of e.g. 20 kHz (28.5 GeV assuming Run 2 conditions) could be lowered by 7 GeV



$$R_\eta = \frac{E_{T,\,\Delta\eta\times\Delta\phi=0.075\times0.2}}{E_{T,\,\Delta\eta\times\Delta\phi=0.175\times0.2}}$$

Ratio between the transverse energy of a Super Cells group of dimension 3x2 and the transverse energy of a group 7x2.

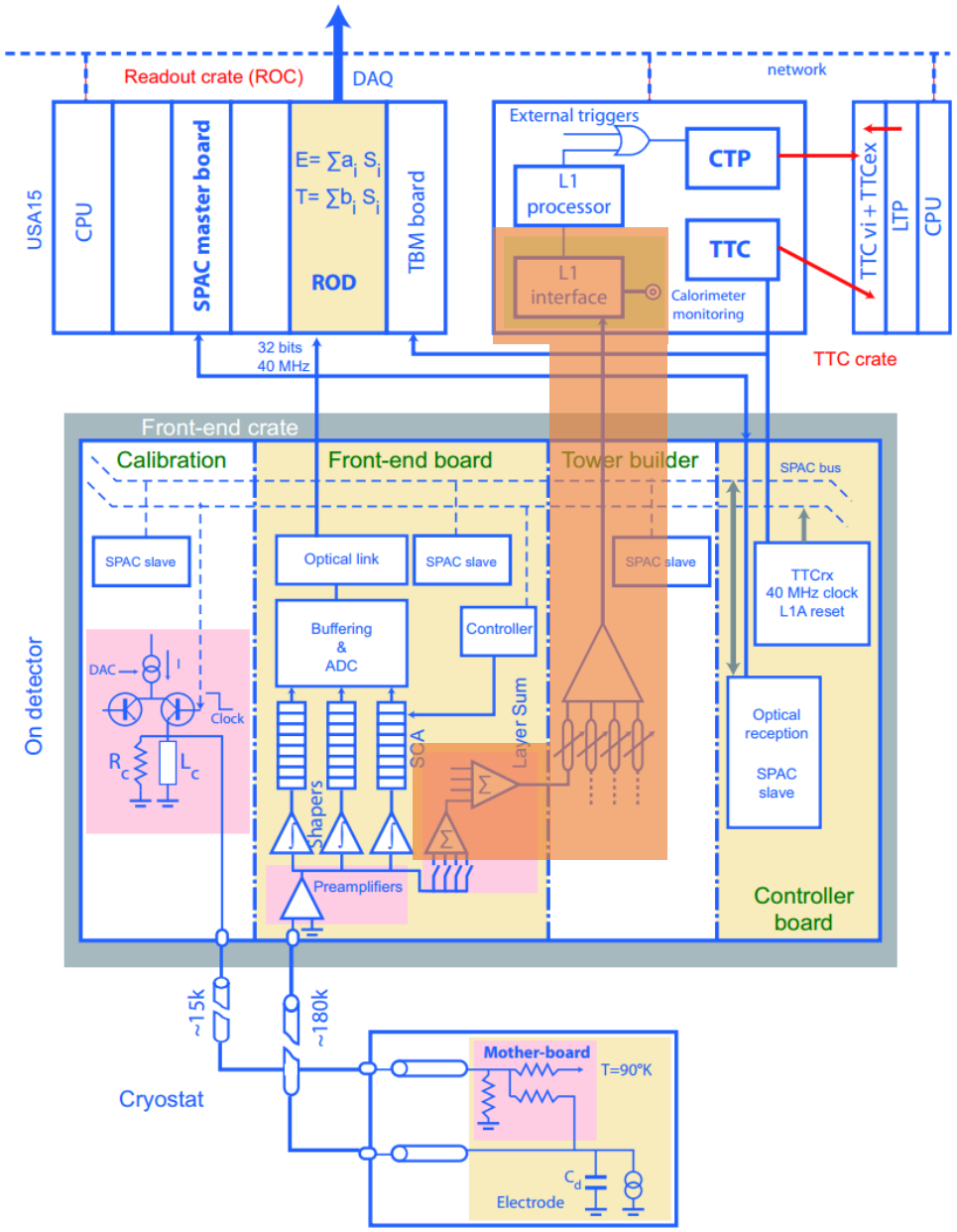


LAr Phase-I Upgrade Project

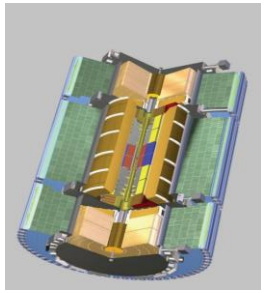
Current system

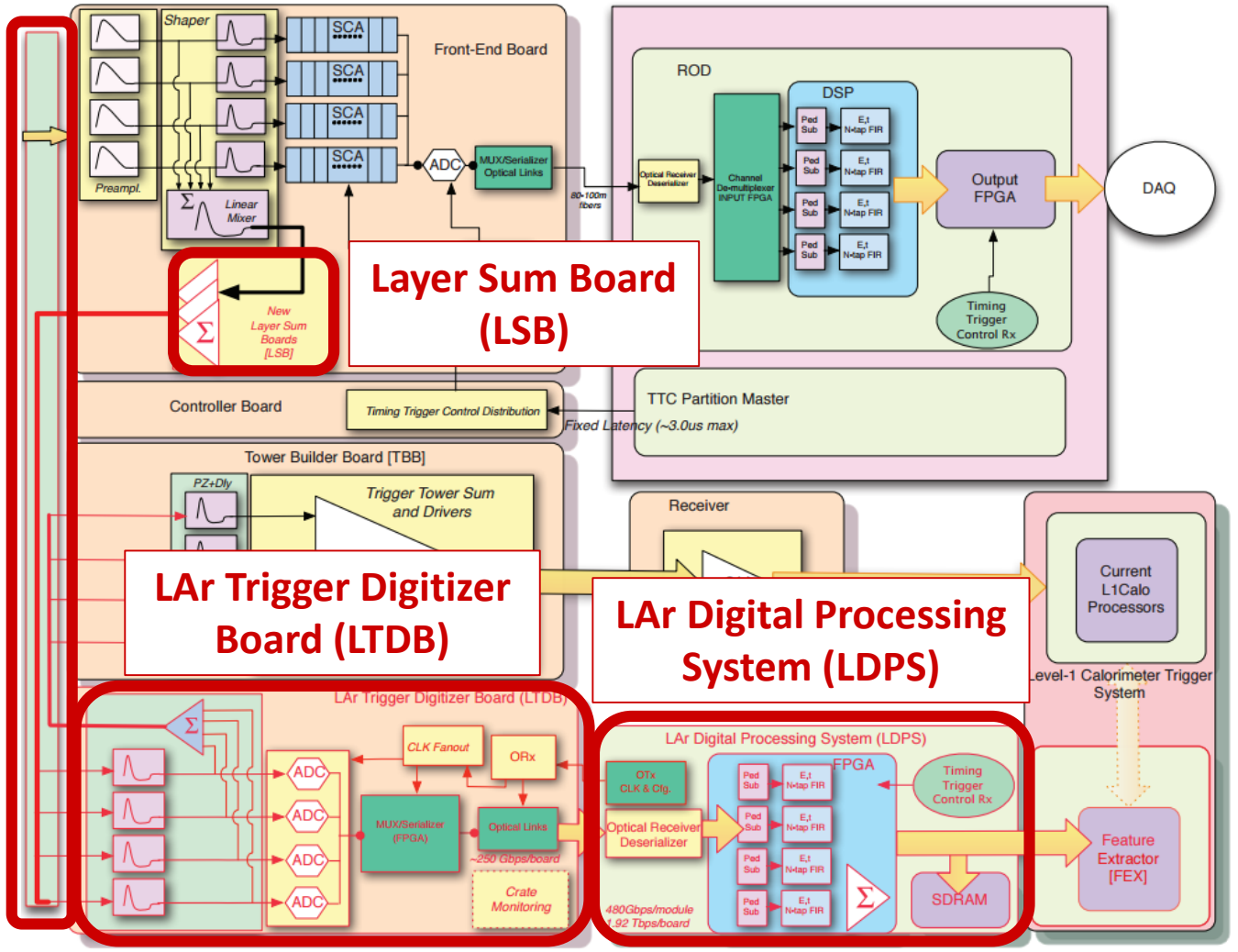
- Schematic block diagram of the current LAr readout electronics architecture.
- The LAr ionization signal proceeds upwards, through the FE crates mounted on the detector to the BE electronics in the USA15.

Electronics to be addressed for Phase-I Upgrade



LAr Phase-I Project





- New elements are highlighted in RED

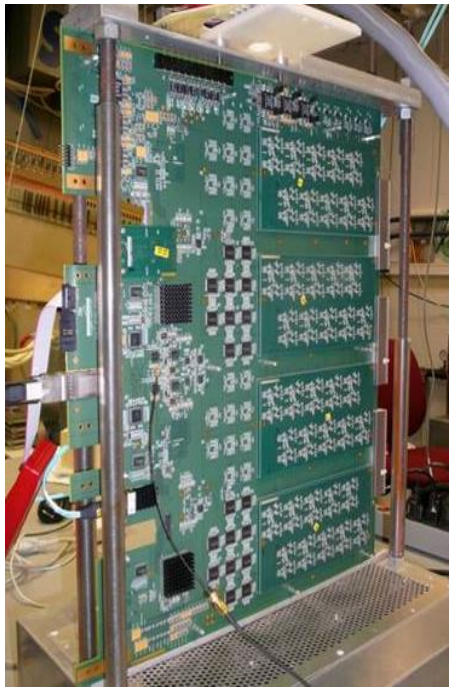
LAr Demonstrator

- Demonstrator installed in summer 2014
  - 2 **LTDBs** readout via **ABBA** boards

- Biweekly system test and demonstrator integration meeting

- Successful 2016 ATLAS **pp data taking**
- No L1Topo during **HI period**
  - LArABBA partition active for some runs, triggering on Physics + Calo

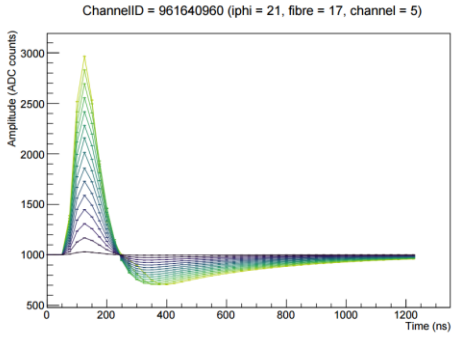
- Getting more **EOS space**
  - EOS request accepted
  - Rights given, data moved to the new data path: /eos/atlas/atlascerngroupdisk/larg-upgrade/ABBA/ATLAS/rawdata



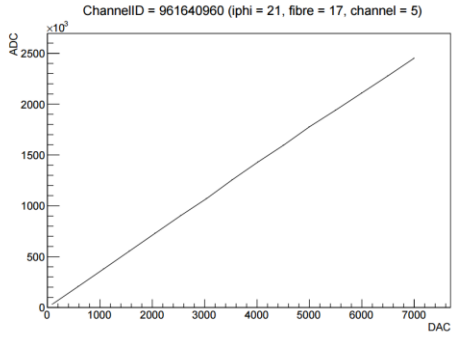
LAr Demonstrator (2)

➢ **Development and analysis works are making progress**

- Continuous **development** on **firmware** and **software**
  - Corrected latency shift happening during long runs
  - Introduce ID for tracing packets between FPGAs
  - Integration of ABBA as a new segment of ATLAS
- **Calibration** data taking has been carried out
- **New Ntuples** format for demonstrator data



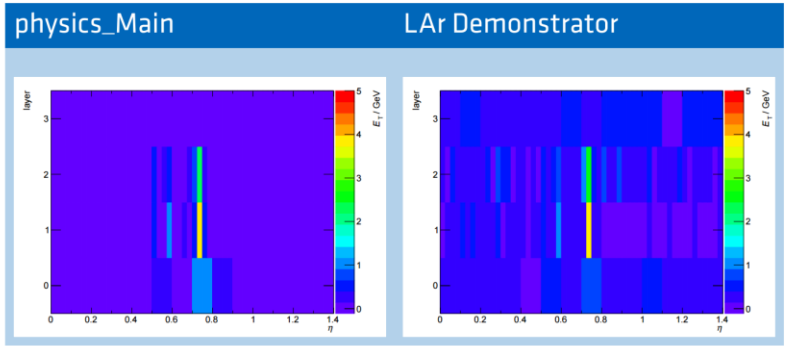
Raw ramp measurements

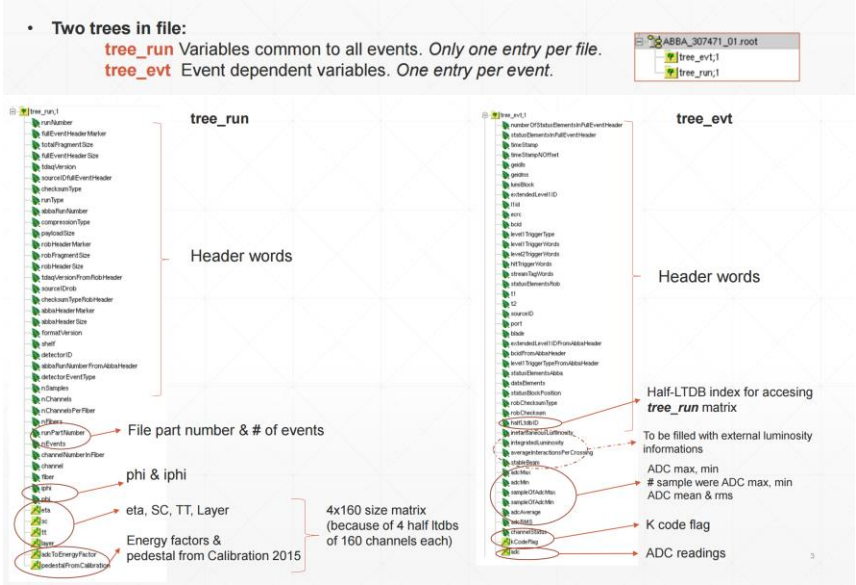


ADC to DAC linearity

Matched example shower in 313285

- Example shower in 20:2, lb=221, bcid=465, l1id=3858919763, ttype=0x84

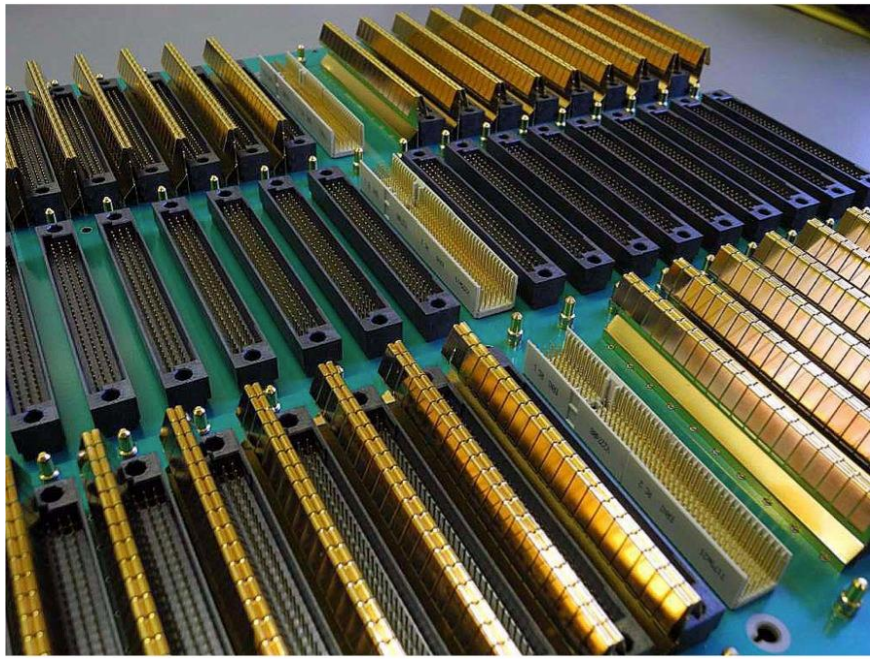




Baseplane

➢ **FDR of Baseplanes : 30 June 2015**

- **EMB and EMECStd** full contract awarded, first item to arrive around the end March 2017 (100 pcs)
  - PRR to release production around April 2017
- **HEC** prototype done, advance testing, preparing production (8 pcs)
- **FCAL** side A prototype under test. FCAL side C needs a modified design (2 pcs)
- **EMEC SP** Prototype in fabrication (8 pcs)

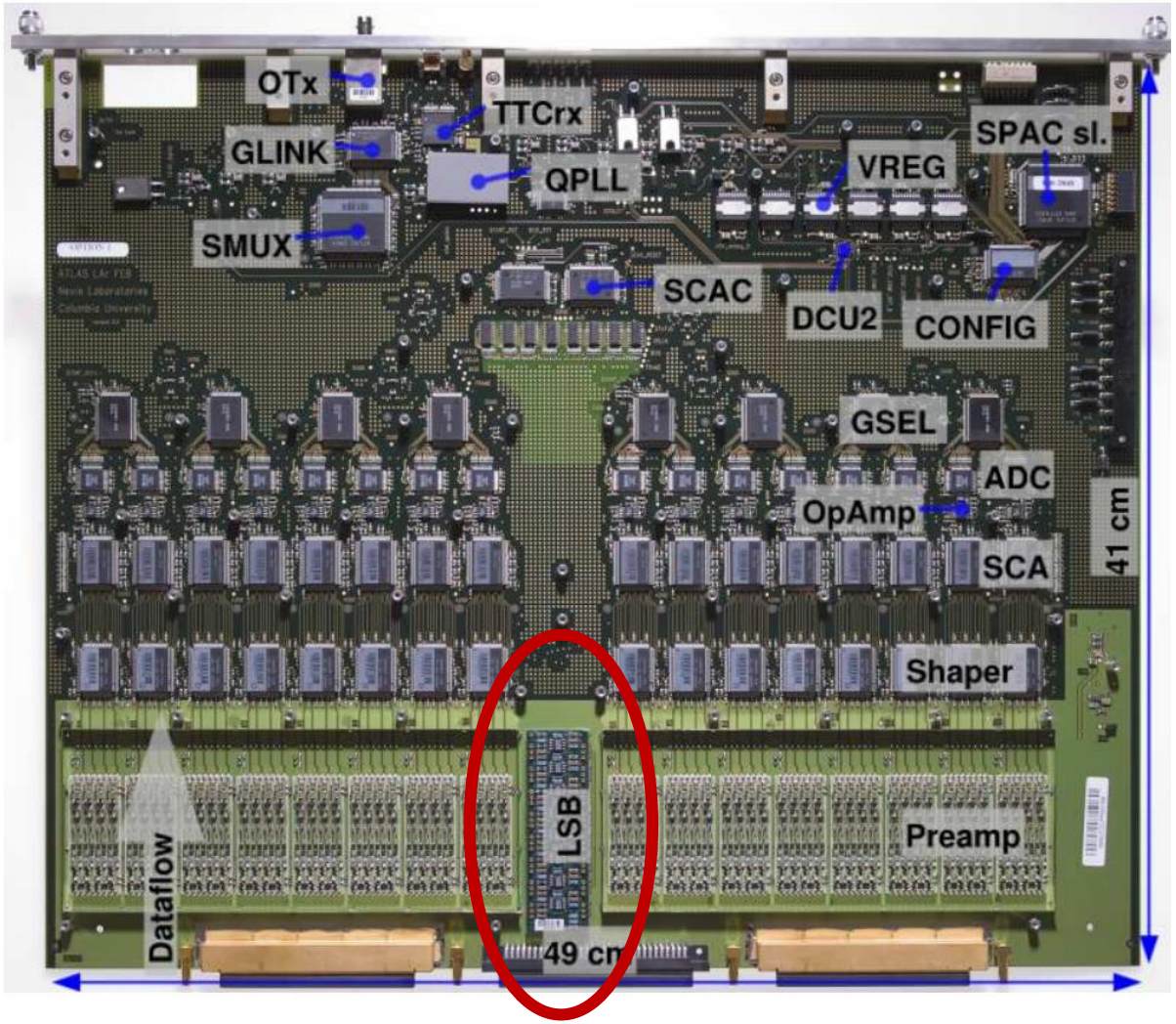


- Manufacturer identified for *RF springs* (original 2005 vendor dismissed), trying to pass full PO from CERN

Layer Sum Board

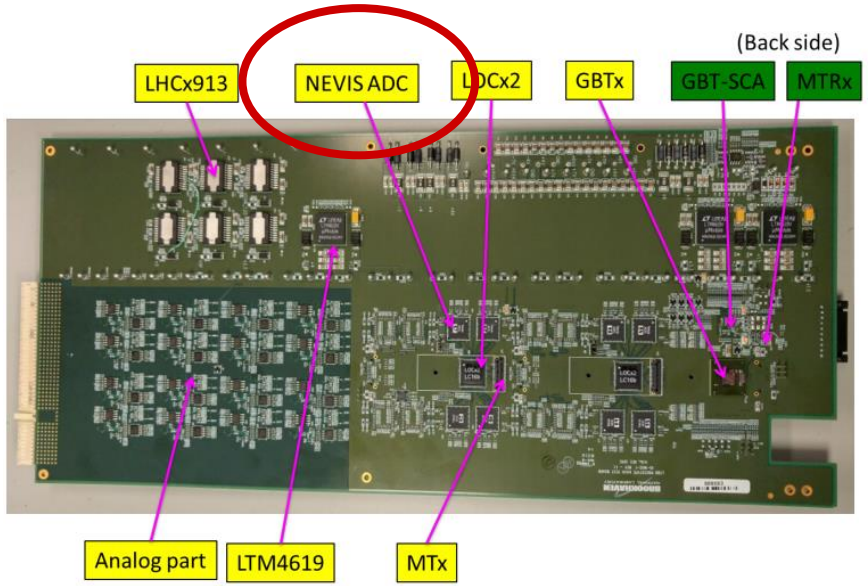
- **FDR of LSBs: 30 June 2015**
- **First part of LSB PRR on July 19:**
  https://indico.cern.ch/event/547081/
- **Second part of LSB PRR on October 19:**
  https://indico.cern.ch/event/574104/

- All qualifications done
- Single lot opamps ordered and arrived
- LSBs production ongoing



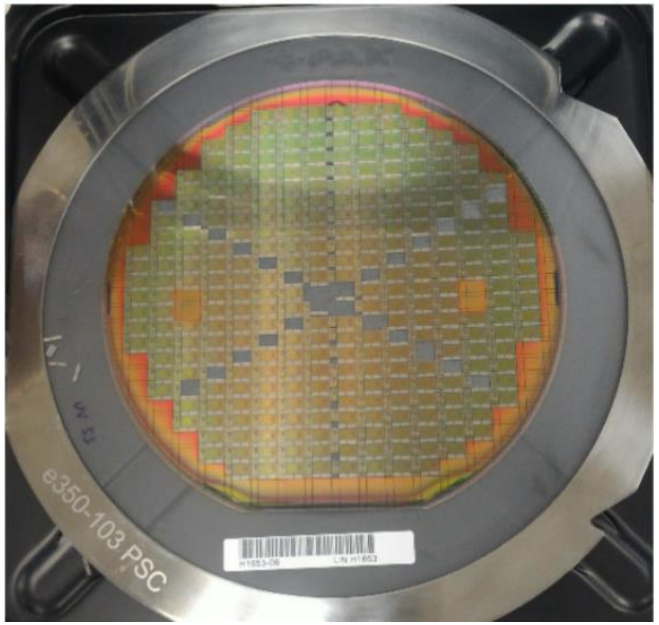
LTDB: ADC

- **PDR of ADC (May 2014)** : use Nevis ASIC
  - Power, latency gain



- **Nevis13 - Nevis14**: found digital issue (2015), ADC producing “bad codes” = “spikes” @~10 Hz
- **Nevis15 chip**: “minimal” modification (no analog changes)
- Available March 2016 and tested on 64 channels board: **OK**
  - QA to select good chips
- Mini-production end 2016 for ~180 chips for the assembly of LTDB prototypes

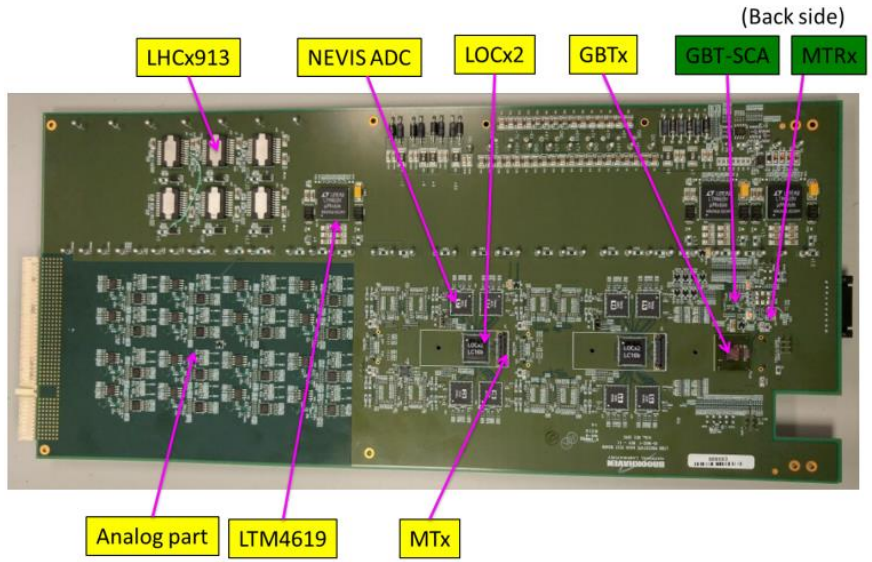
LTDB: LOCx2 & LOCld



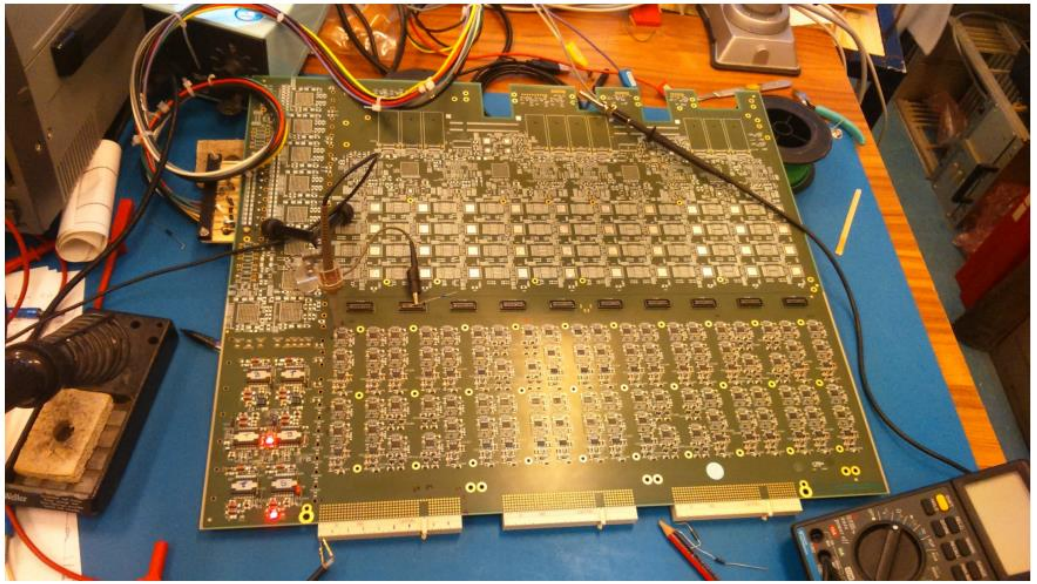
- **LOCx2 (Serializer) / LOCld (opt. Link)**
  - Baseline option **250 nm SOS** (Silicon On Sapphire)
    - After production failure, **130 nm CMOS backup solution**
      - LArTDS: serializer based on GBTx IPs
      - Design done (submission August 2016)
      - Chips delivered, currently under test
      - First operation seems OK.
  - **4 different processed wafers** received on August 2016 : **OK,** minor yield differences
  - Ordered full production of 20 wafers: **16/20 OK**.
    - Dies starting to be packaged now.
    - Should have proof of functioning at the end of February
- **If all OK** (yield ~> 50%), sufficient chips in hand next months
- **QA plans** in preparation and **radiation tests** to be repeated

LTDB Development

- **LTDB 64ch prototype**
  - Fully tested
  - Checked all chip control
    - GBTx, GBT-SCA, MTx, MTRx
    - Nevis14 - Nevis15
  - Also September LOCx2, all OK
  - Confidence building for 320 channels prototype

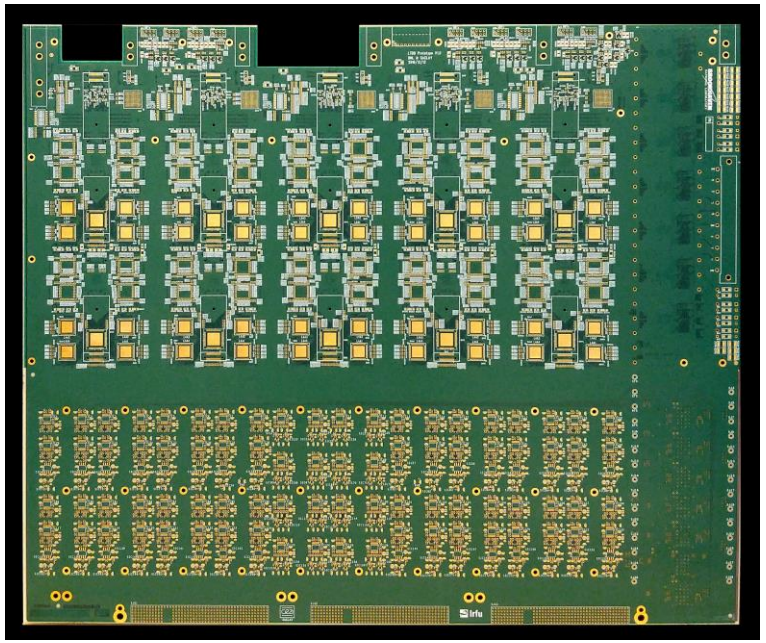


- **LTDB pre-prototype 320ch**
  - Design Integration learning
  - Large board manufacturing
  - Analog performance check @ Saclay
  - Digital Readout tested at BNL with FELIX board

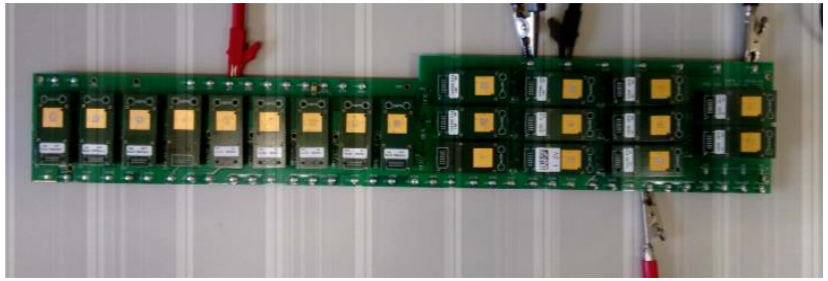


LTDB Development (2)

- **LTDB prototype**
  - Gerber merged at the end of December
  - Some delay came from details Milano/Saclay/BNL for the PDB (Power Distribution Board) pins + monitoring signal
  - PCBs received Jan 31st. Board expected end February
  - Tests in ~March @ BNL, @ Saclay
  - **AIM:** 2 LTDB prototypes could be used to **replace LTDB demonstrators** in January 2018



- **Power Distribution Board (PDB)**
  - Based on FEAST device from CERN, development on going (Milano)
  - PDB design and submission by end February 2017

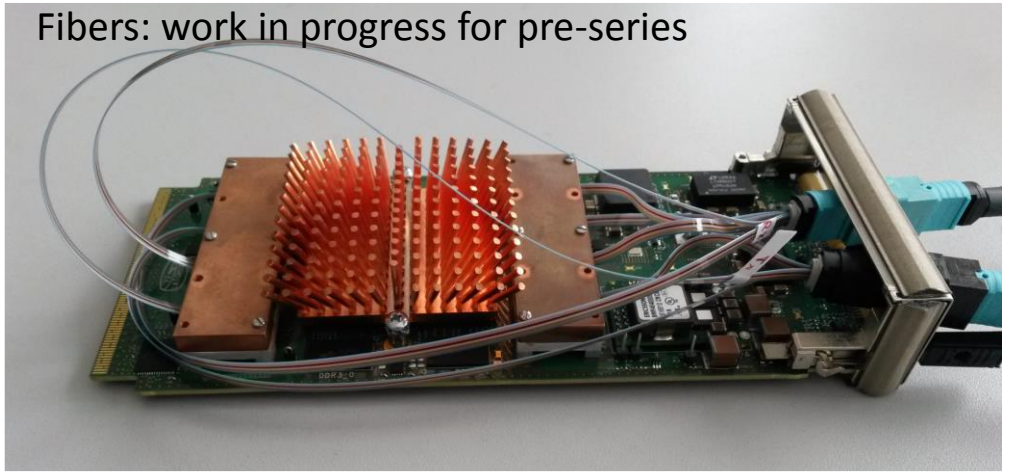


  - Joint test LTDB-PDB (expected April 2017) will define FE reviews
    - FDR of LTDB, PRRs of ASICS (~May 2017)

LDPS Development

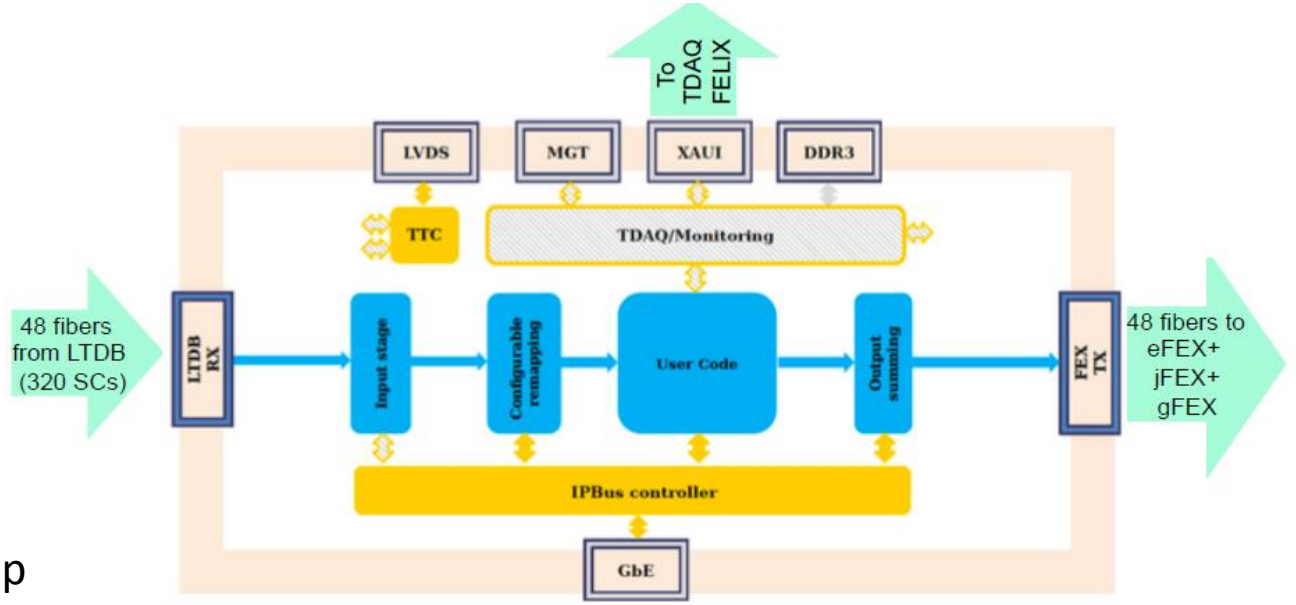
- **LATOME**
  - Based on Altera Arria10 FPGA
  - AMC : LATOME V2 ready at the end of 2016
    - Functional tests : OK
    - Optical tests : PRBS @12.8Gb/s OK

- **Carrier board V1 2015, FDR passed with AMC**
  - V2 available since Spring 2016
    - On board Ethernet HW chip
  - V3 already assembled
    - Test ongoing
    - To be used in further integration

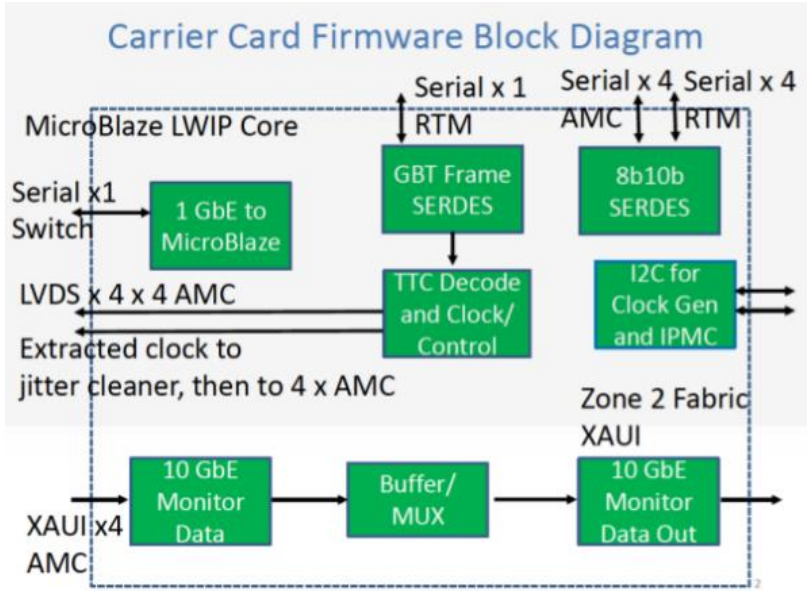


LDPS Firmware

- **LATOME firmware development ongoing**
  - Block deliverables:
    - quite some groups contributing
  - Emphasis on simulation and integration
  - Latency and resources verified at each major step
  - Adapt to System Test milestones : implement on HW

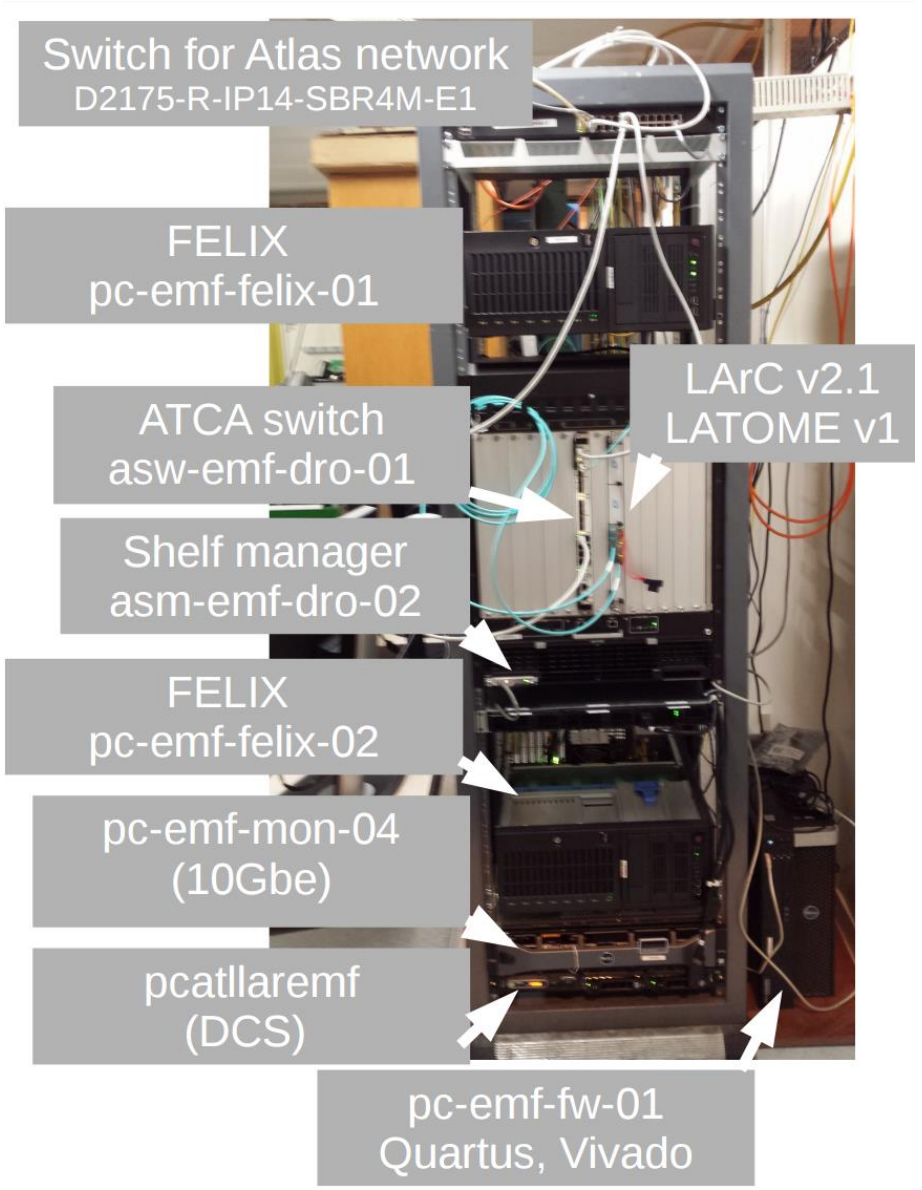


- **Carrier firmware development ongoing**
  - Development of Carrier firmware continues with emphasis on completing a baseline project
  - Testing of Carrier hardware and firmware at EMF will be ongoing (TTC, 1GbE, 10GbE etc.)
  - Stability issue of uBlaze project to be addressed



Back End System Test

- **Demonstrate feasibility of BE system**
  - Pass PRR for releasing series board production
  - Show operation of all parts of system
  - Verify operation of FPGAs
  - Test Power-Cooling in ~final conditions
  - Boost coding, testing and debugging of FW
  - Boost coding, testing and debugging of Online SW (incl. TDAQ)
  - Mobilize whole LAr Ph-1 community
  - Eventually connect to LTDB
    - Full system test



Back End System Test(2)

- ST-M0 completed on November 2016
  - Clock from FELIX well recovered on LArC and LATOME
- ST-M1 had a slight delay, ~OK on January 2017
  - Good progress on firmware and software side to R&W in registers via 1GbE
- DCS monitoring completed for ST-M2 on December 2016
- ST-M3 will be the next major milestone: planned for

  March 2017
  - Inject LTDB data, and readout FEX data for comparison
- ST-Mxx to M11: the last one to be completed ~Fall 2017

Milestone	Date of Completion	Goal (done at EMF)
M0	15/10/2016	• **Recover the TTC clock** with LArC up to LATOME v1 (FW needed to be ready). Running: 1 LArC + 1 LATOME v1 + 1 Felix (TTC only) Test done in the ATCA crate moved from building 104 to EMF.
M1	1/11/2016	• **Board configuration:** hw, some mapping and some calibration parameters **via Largonline** → to be determined: which registers we want to use • **Read board status:** information to IS via 1 GbE (preliminary check that the links are working, to be check again during M3 while reading LTDB data)
M2	1/11/2016	• **DCS:** understand how to deal with DCS and get monitoring info (T, V, I histograms)
M3	1/12/2016	• **FEX test:** 1 LATOME inject & read (A) + 1 LATOME operating (B), A inject LTDB data into B, B compute E_T and send FEX data to A (via µPods), check that data injected and read by A are OK via base interface (1 GbE) • **Power and thermal tests** (test by varying the number of samples used for the E_T computation) • **Overnight tests**
M4	15/12/2016	• **L1A, Trigger Type and BCR decoding** (+possible other TTC commands) [GBT down flow] • **Check time alignment** (BCR in injected data compared to BCR from FELIX)
M5	15/01/2017	• **Readout TDAQ data with FELIX** (+possible other TTC commands) [GBT up flow] • **BUSY test** (to be discussed with L1CALO) • **Stress test:** run >100 kHz to see the freq. max (need some basic "HLT" to write on disk only reasonable amount of data)
M6	15/01/2017?	• **Readout monitoring data** of operating LATOME through 10 GbE (fabric interface), write on disk. To be determined: which data we want to monitor
M7	1/02/2017	• **LATOME v2:** redo up to M6 with LATOME v2 • **Fully functional user code** (use all constants, complete mapping)
M8	8/02/2017	• **Operate 2 LATOME** (can be done first with v1 in case v2 is not yet ready), check time alignment
M9	15/02/2017	• **Operate 4 LATOME** • **Test time aligment:** use fibres of different length? (or simply put some delays in FW)
M10	28/02/2017	• **Operate 2 carriers** (8 LATOME), 2 TTC to test delay between them
Final	March 2017	Full setup running in an ATCA crate: • **12 LATOME v2** running fully functional user code (e.g. compute E_T + saturation detection) • **3 LATOME** emulating LTDB + FEX (+3 optical splitter) • **mini Felix** reading TDAQ data (warning: only 4 GBT links whereas 5 needed for 1 carrier → not all GBT links can be tested together) • **Power & Thermal tests**

Summary

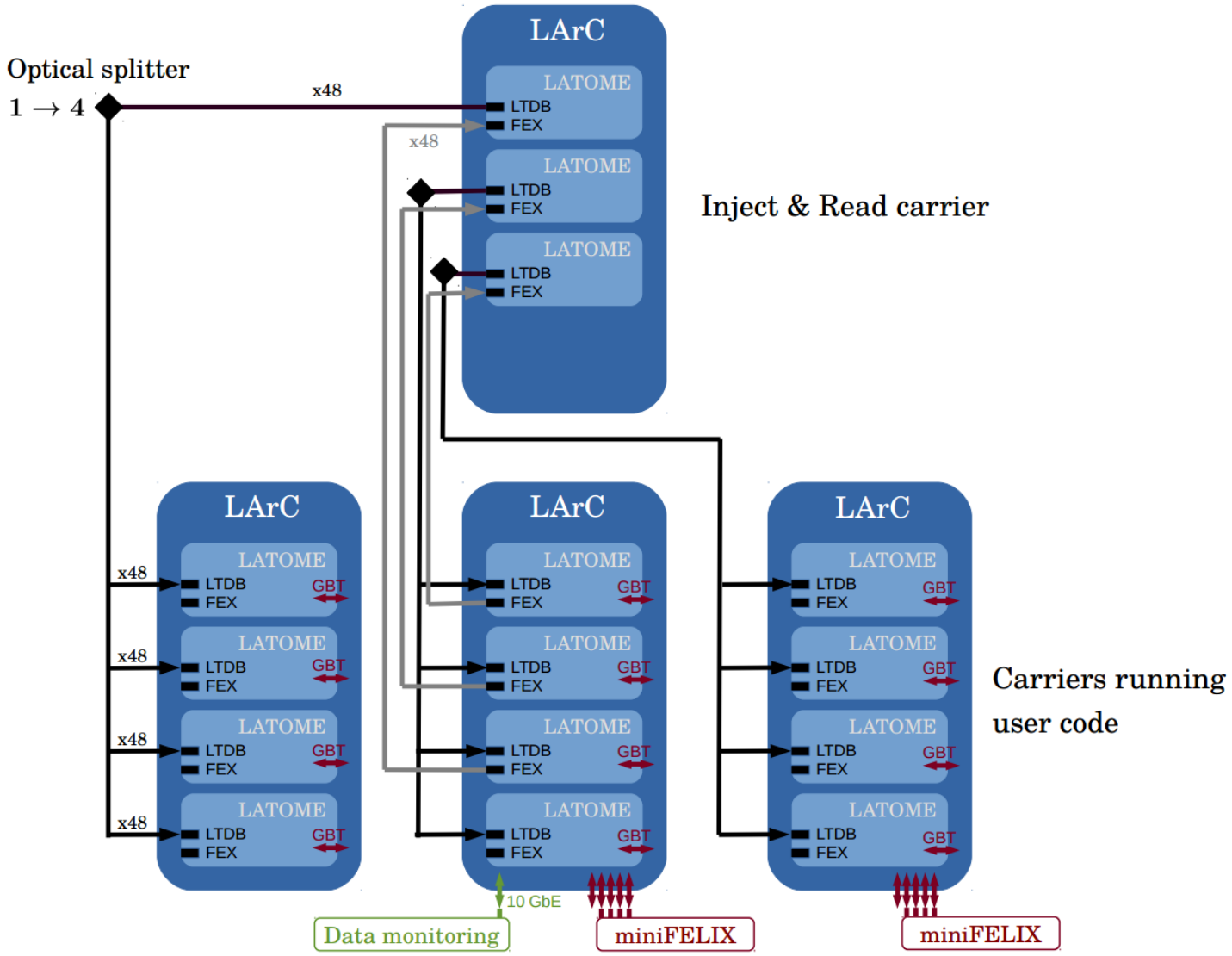
Summary

- LAr Demonstrator has successful 2016 ATLAS pp data taking
  - Preparation for 2017 run has started
- Baseplane is making progress
  - Manufacturer identified for *RF springs*, trying to pass full PO from CERN
- LSBs production ongoing
  - Passed PRR in October successfully
- Front end LTDB
  - Nevis15 ADC tested on 64 channels board and OK, plan to address it by QA
  - LOCx2 16/20 wafer are ok, proof of functioning at the end of February
  - LTDB board development is progressing well with baseline design: FDR by spring 2017
- Back end LDPS
  - LATOME V2 ready at the end of 2016, functional tests OK
  - Carrier V3 assembled
  - Firmware development is making good progress and BE system integration is marching to the next major milestone

Backup slides

Test setup

- 1 carrier :
  - **Inject « LTDB » data**
  - **Read « FEX » data**
  - **→ data verification**
  - **3 optical splitters 1⟶4 : feed the 3 other carriers**
- 3 carriers running user code :
  - **compute E_T for L1 (FEX)**
  - **Send data to TDAQ via FELIX**
- TTC signal via FELIX
- Data Monitoring via 10 GbE
- Test done at EMF



Number of boards

LTDB : 124

LAr Carrier : 31

LATOME : 124

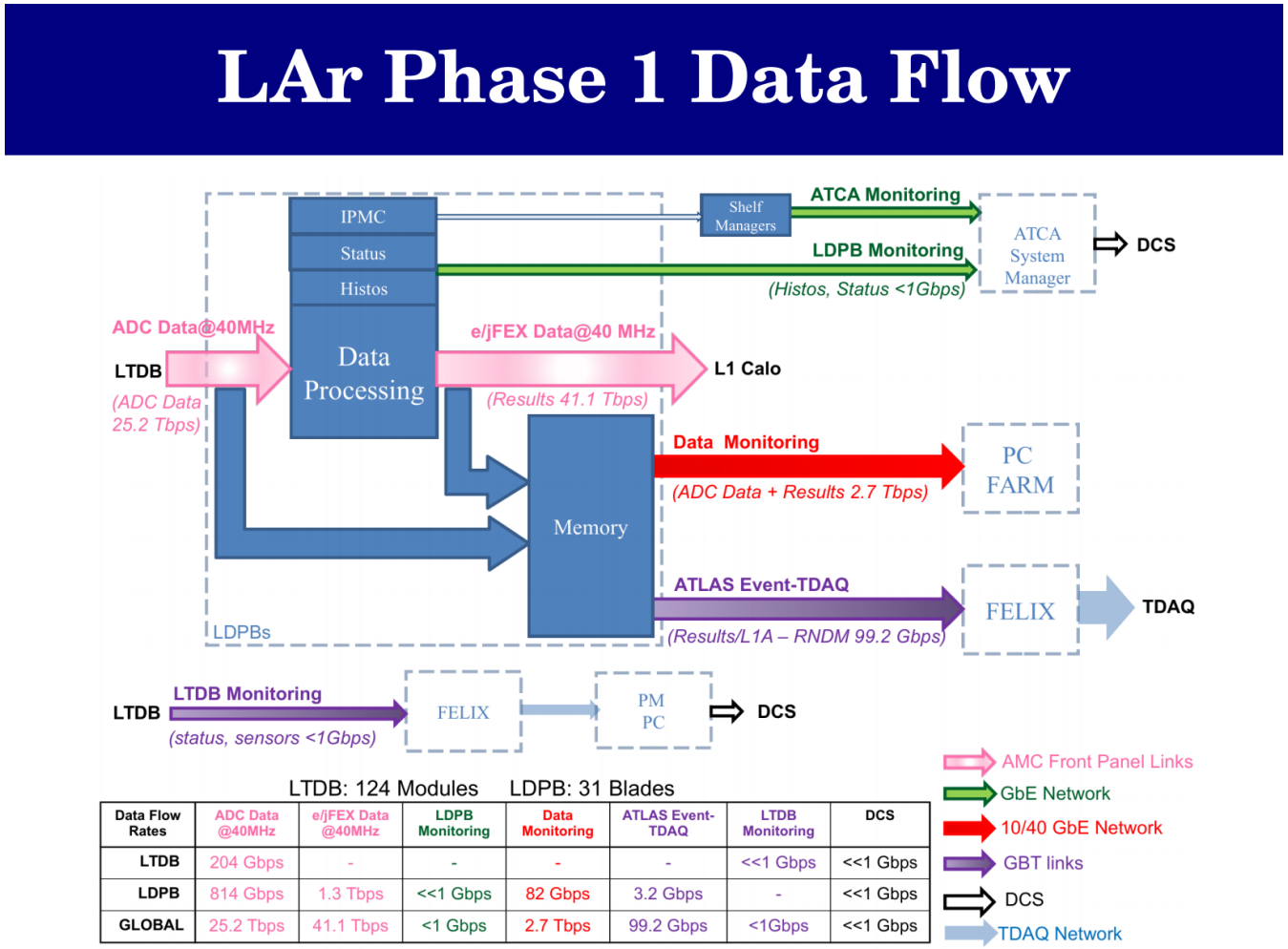
Planning (1)

Milestone	Date of Completion	Goal (done at EMF)	Online SW	FW	HW	People involved
M0	15/10/2016	• **Recover the TTC clock** with LArC up to LATOME v1 (FW needed to be ready). Running: 1 LArC + 1 LATOME v1 + 1 Felix (TTC only) Test done in the ATCA crate moved from building 104 to EMF.	IPMC soft ready (no other online sw needed) → power the board properly	Test of clock for LArC, LATOME with FELIX	• 1 LATOME v1 • 1 LArC v2.1 • 1 pseudo-FELIX • 1 PC (felix) on GPN • ATCA crate • 1 PC with a screen (to run quartus, vivado...). on GPN • 1 switch for ATCN	**software:** Fatih, Danièle **firmware:** Nicolas DD, Ken, Dean, Bernard, Nour, Franck **EMF installation:** Luis, Guy Andrei, Alexis, Ken, Dean, Dirk
M1	1/11/2016	• **Board configuration:** hw, some mapping and some calibration parameters **via Largonline** → to be determined: which registers we want to use • **Read board status:** information to IS via 1 GbE (preliminary check that the links are working, to be check again during M3 while reading LTDB data)	• Partition "EMF_Phase1" with GUI • Calibration: dedicated DB (if not yet ready can start with already existing static config) • hw config: OKS • mapping: OKS	Read and write in registers	+ 1 switch ATCA	**software:** Fatih, Alexis **firmware:** Determined by FW group
M2	1/11/2016	• **DCS:** understand how to deal with DCS and get monitoring info (T, V, I histograms)		Determine critical FPGA parameters to be monitored by DCS (via ATCA)	+1 PC running DCS software	**DCS:** Sergey **firmware:** Nicolas DD, Alexis, Dean **software:** Fatih (IPMC, MMC)
M3	1/12/2016	• **FEX test:** 1 LATOME inject & read (A) + 1 LATOME operating (B), A inject LTDB data into B, B compute E_T and send FEX data to A (via µPods), check that data injected and read by A are OK via base interface (1 GbE) • **Power and thermal tests** (test by varying the number of samples used for the E_T computation) • **Overnight tests**	Read FEX data + check	• Generate LTDB data (pulse) • Compute E_T • Read and check FEX data	+1 LATOME v1	**software:** Fatih. Alexis **firmware:** Determined by FW group
M4	15/12/2016	• **L1A, Trigger Type and BCR decoding** (+possible other TTC commands) [GBT down flow] • **Check time alignment** (BCR in injected data compared to BCR from FELIX)	LTP program to generate different Trigger Type	• Decoding of TTC • Check of time alignment (put by hand some delay in the FW) To be determined: GBT stream got from FELIX send well TTC commands		**software:** Alexis **firmware:** Determined by FW group

Planning(2)

M5	15/01/2017	• **Readout TDAQ data with FELIX** (+possible other TTC commands) [GBT up flow] • **BUSY test** (to be discussed with L1CALO) • **Stress test:** run >100 kHz to see the freq. max (need some basic "HLT" to write on disk only reasonable amount of data)	[Offline analysis of data]	GBT link fully bidirectional	FELIX-PX moved to ATCN + 1 PC with 10 GbE	**software:** Fatih. Alexis **firmware:** Determined by FW group
M6	15/01/2017?	• **Readout monitoring data** of operating LATOME through 10 GbE (fabric interface), write on disk. To be determined: which data we want to monitor	Develop readout via push mode? (pull mode may be less efficient)	fabric readout		**software:** Fatih. Alexis **firmware:** Determined by FW group
M7	1/02/2017	• **LATOME v2:** redo up to M6 with LATOME v2 • **Fully functional user code** (use all constants, complete mapping)	Constants read from DB	User code fully functional	• 1 LATOME v2 (operating) • 1 LATOME v1 or v2 (I&R)	**software:** Fatih. Alexis **firmware:** Determined by FW group
M8	8/02/2017	• **Operate 2 LATOME** (can be done first with v1 in case v2 is not yet ready), check time alignment			• 2 LATOME (operating) • 2 LATOME (I&R)	
M9	15/02/2017	• **Operate 4 LATOME** • **Test time aligment:** use fibres of different length? (or simply put some delays in FW)			• 4 LATOME (oper.) • 1 LATOME (I&R) [can also use 2 other LATOME v1 to read in total 3 operating LATOME] • 2 LArC • 1 optical split. 1→4	Bernard test that the optical splitting 1→4 is working
M10	28/02/2017	• **Operate 2 carriers** (8 LATOME), 2 TTC to test delay between them			• 8 LATOME (operating) • 2 LATOME (I&R) • 3 LArC • 2 optical split. 1→4 • 2 FELIX	
Final	March 2017	Full setup running in an ATCA crate: • **12 LATOME v2** running fully functional user code (e.g. compute E_T + saturation detection) • **3 LATOME** emulating LTDB + FEX (+3 optical splitter) • **mini Felix** reading TDAQ data (warning: only 4 GBT links whereas 5 needed for 1 carrier → not all GBT links can be tested together) • **Power & Thernal tests**			• 15 LATOME (12 operating, 3 I&R) • 4 LArC • 3 optical split. 1→4 • 1 PC running DCS software • 1 PC with 10 GbE for data monitoring • 2 PC for (mini)FELIX [only 1 PC if regular FELIX available] • 1 PC with a screen (to run quartus, vivado...) • 18 cables of 48 fibres MTP (for µPODs)	

Phase-I Data Flow



Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

Phase-I Data Flow