UNIVERSITÀ DEGLI STUDI DI MILANO

INFN
Istituto Nazionale di Fisica Nucleare

ABBA firmware and system checks

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Getting ready

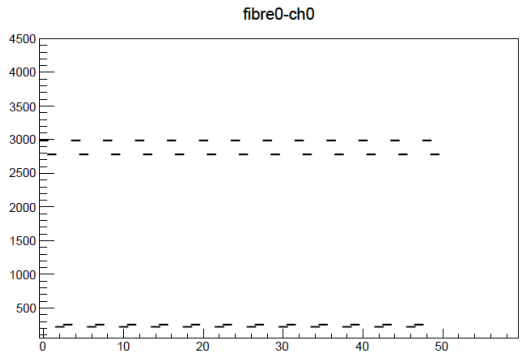
Firmware version (official released) v0.99 (re)tested in USA15 on all FPGAs.

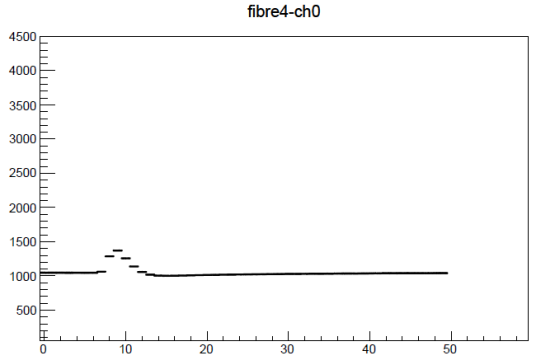
(No changes on the back FPGA firmware version for the moment)

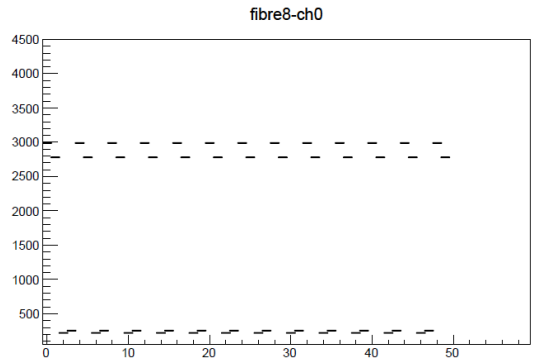
Software on call (Jue) took a new set of calibration run on 16th of May: run number 323511 with the usual pattern for firmware tests.

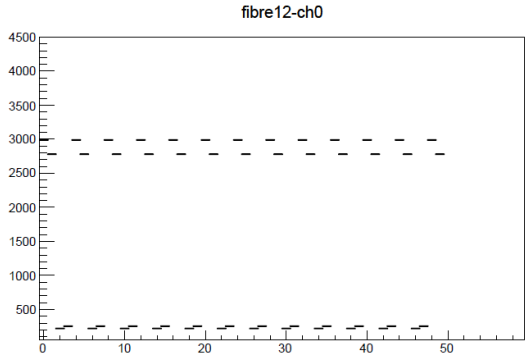
- Check the BNL pulses stability
- Check the peak position and eventually correct the internal value in the firmware
  - Set in the panel the correct peak position

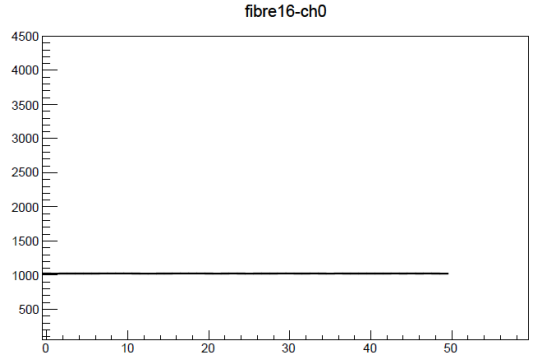
Run 321355 (28th of April) – FPGA 18:2 (French LTDB)

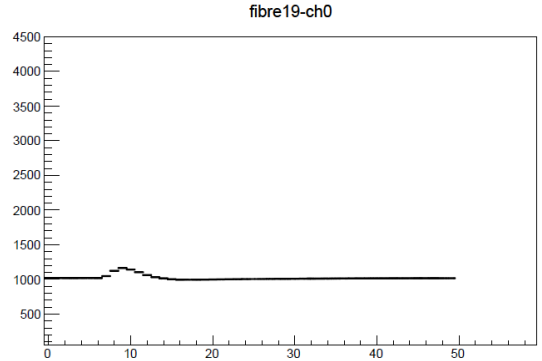




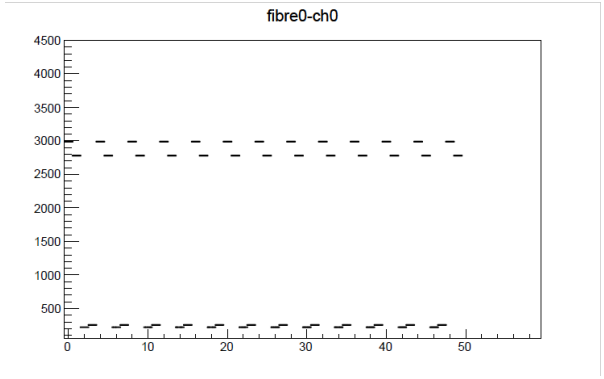


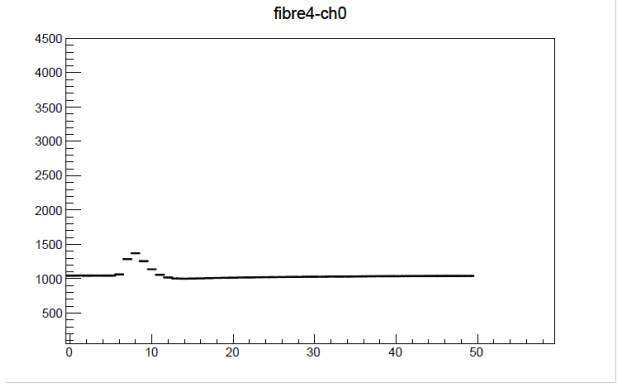


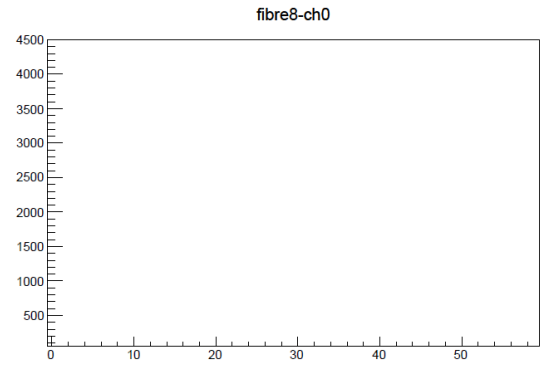


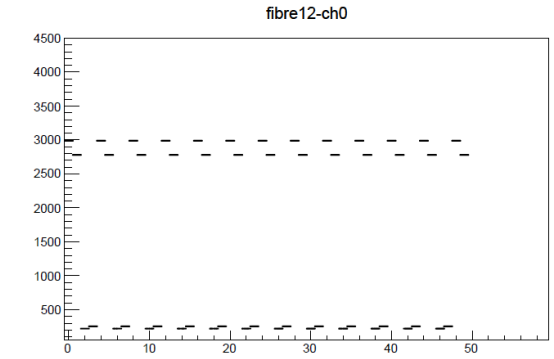


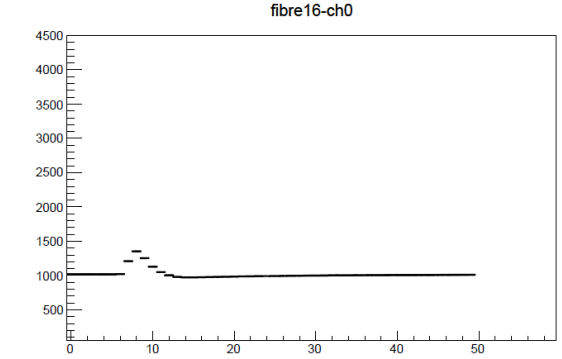
Run 323511 (16th of May) – FPGA 18:2 (French LTDB)

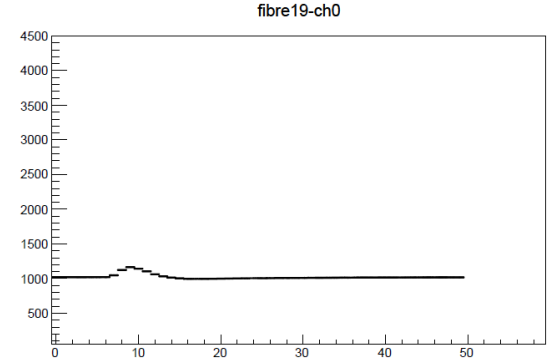




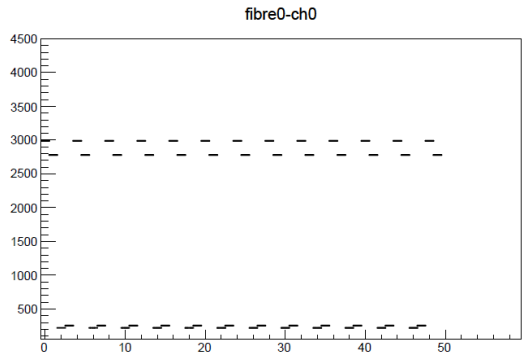


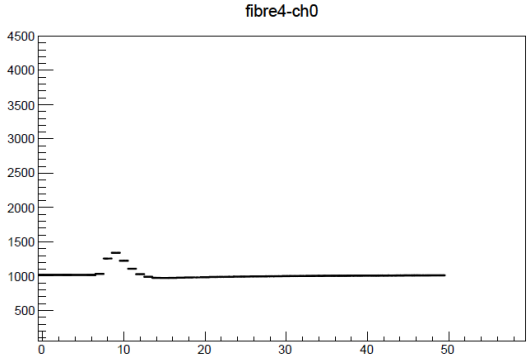


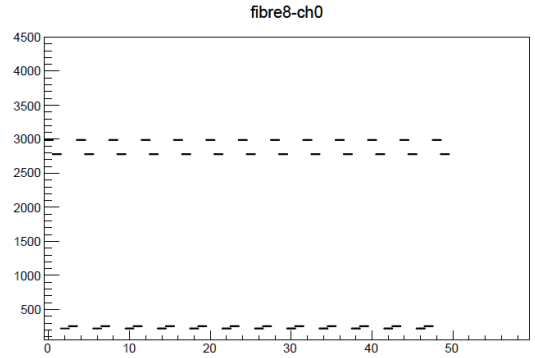


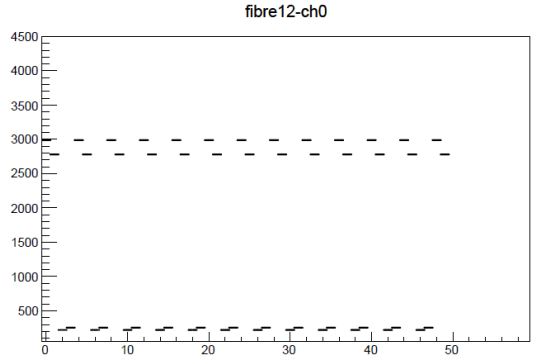


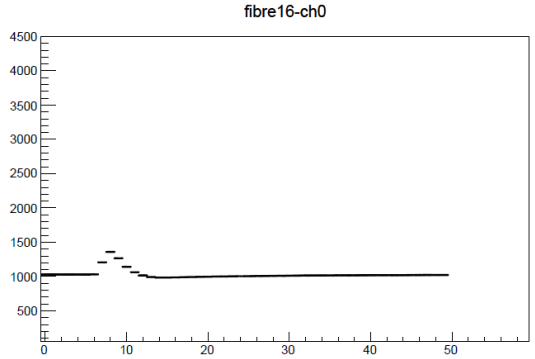
Run 321355 (28th of April) – FPGA 19:1 (French LTDB)

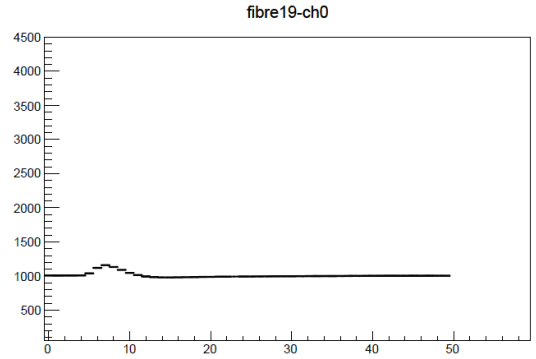




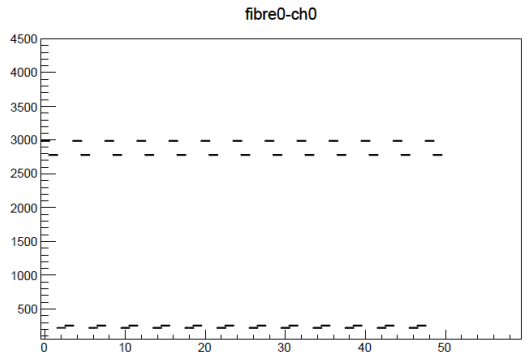


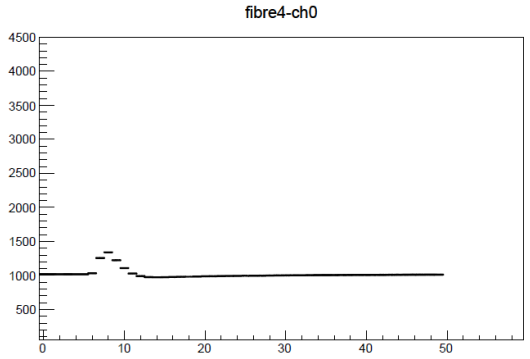


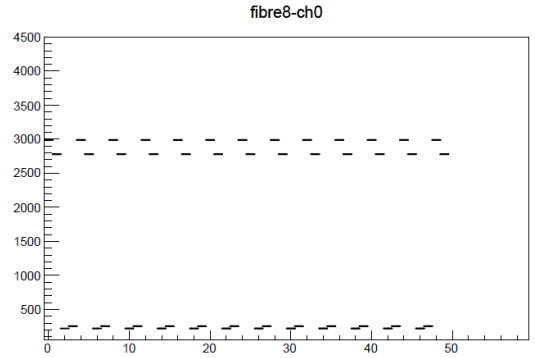


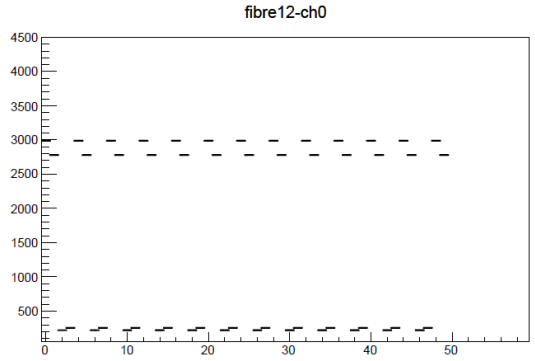


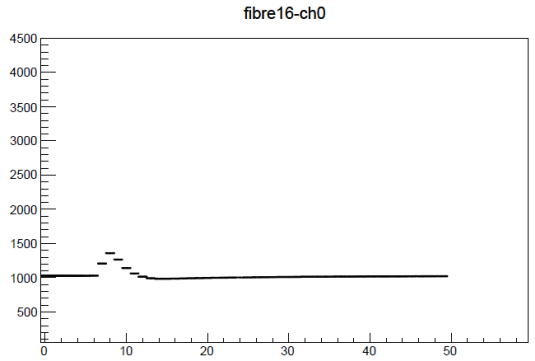
Run 323511 (16th of May) – FPGA 19:1 (French LTDB)

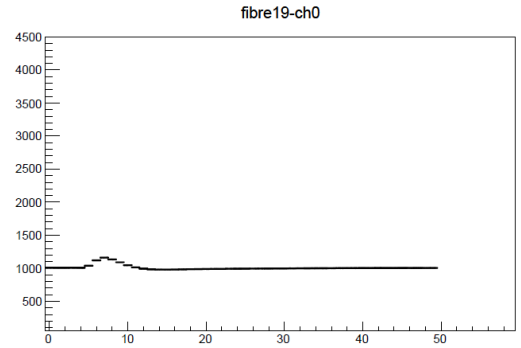




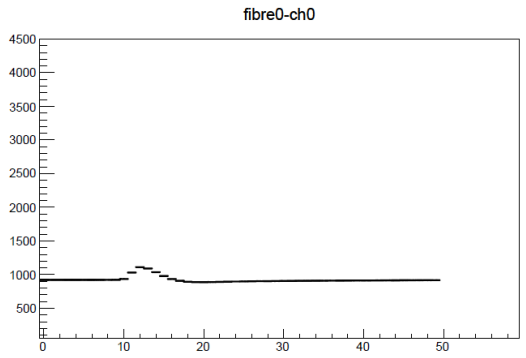


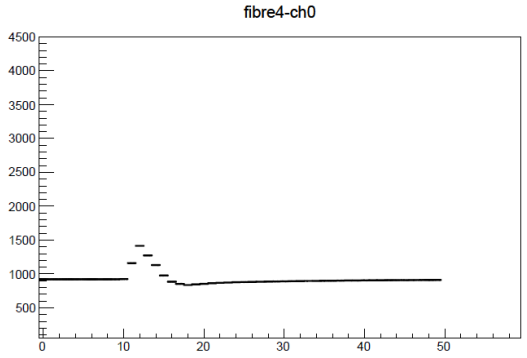


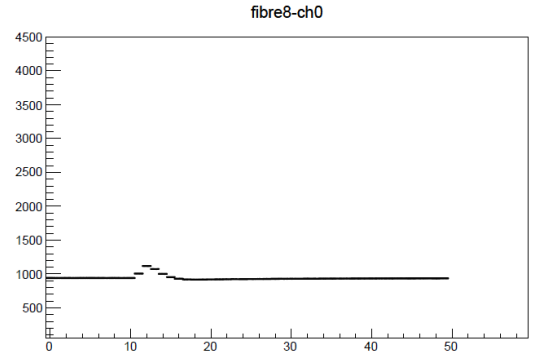


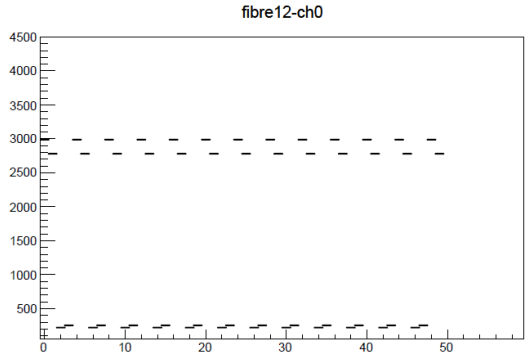


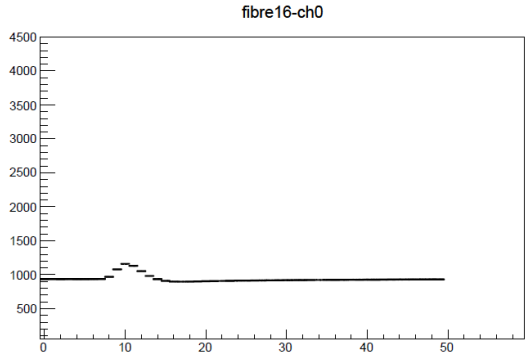
Run 321355 (28th of April) – FPGA 19:2 (BNL LTDB)

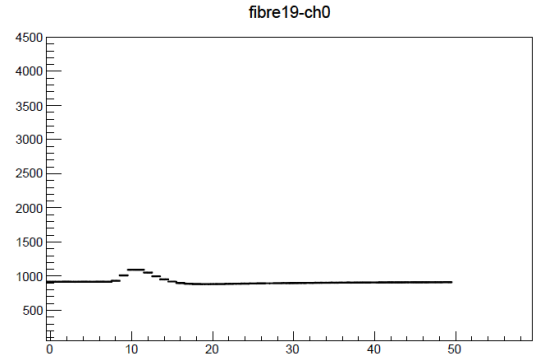




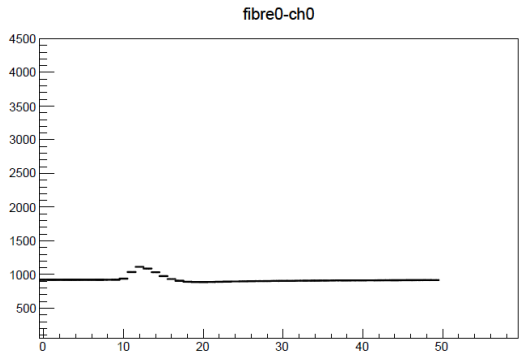


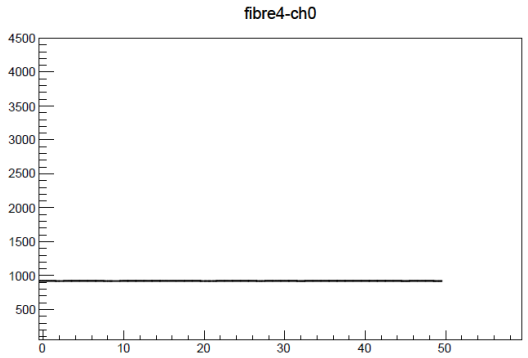


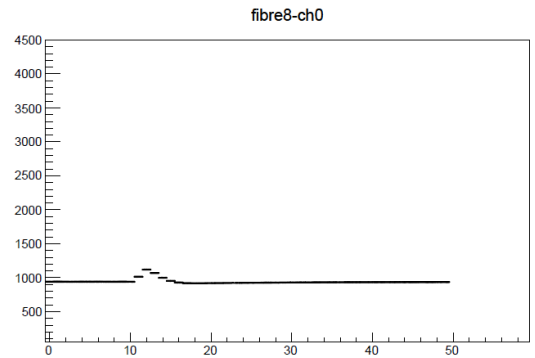


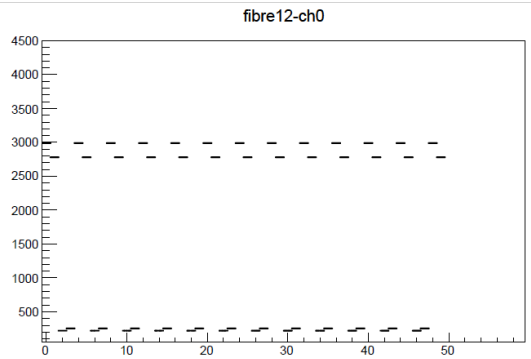


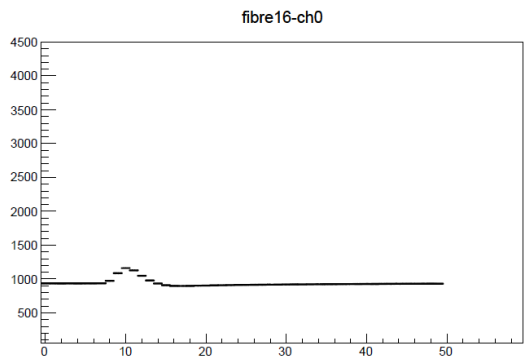
Run 323511 (16th of May) – FPGA 19:2 (BNL LTDB)

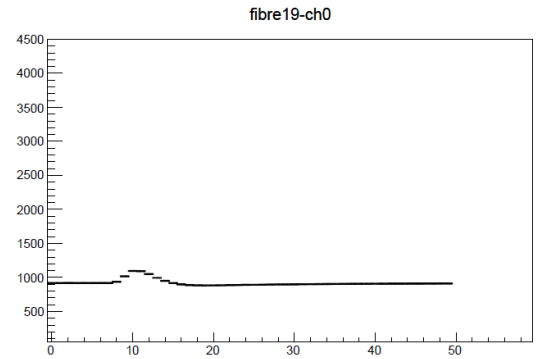




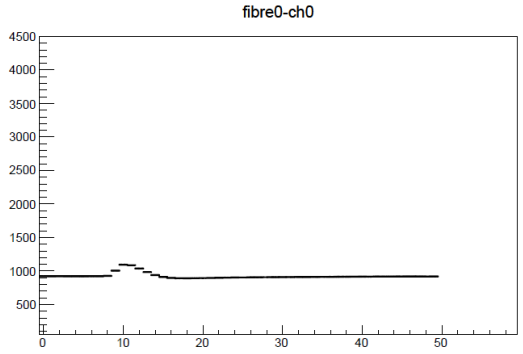


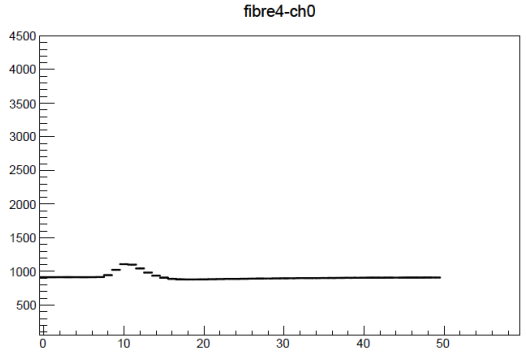


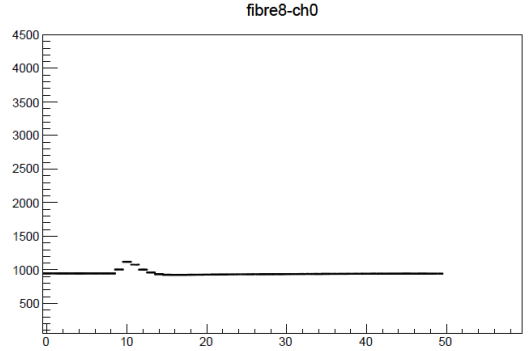


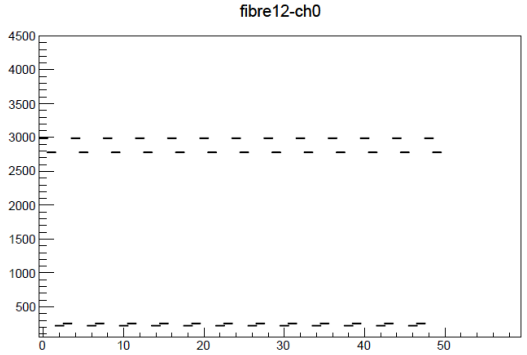


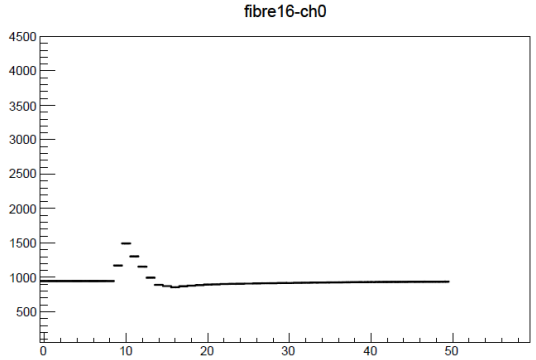
Run 321355 (28th of April) – FPGA 20:2 (BNL LTDB)

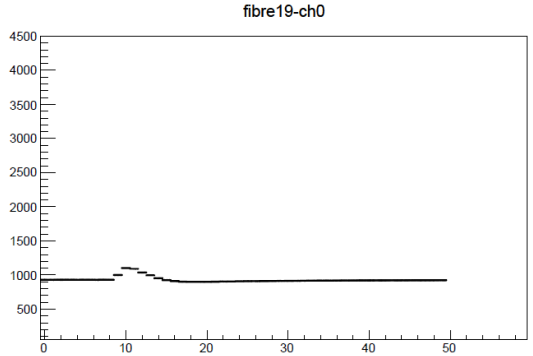




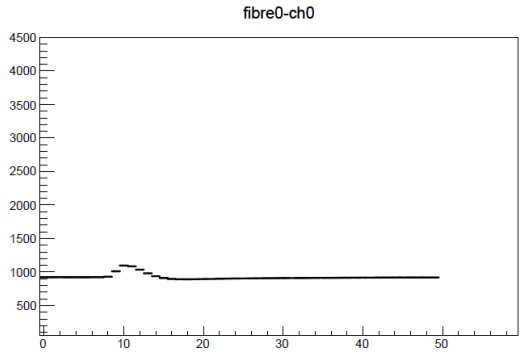


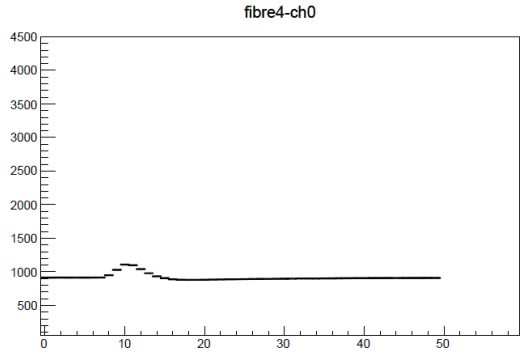


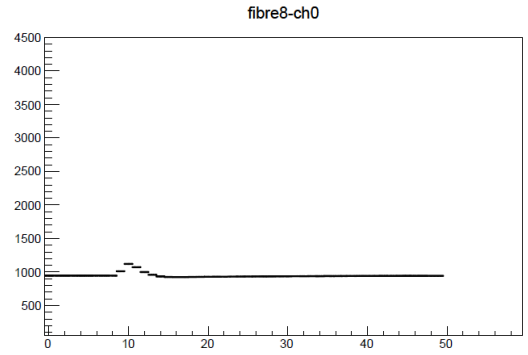


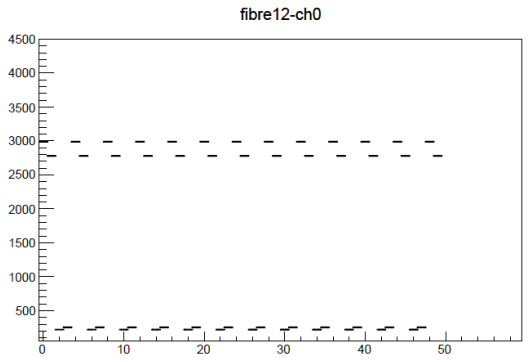


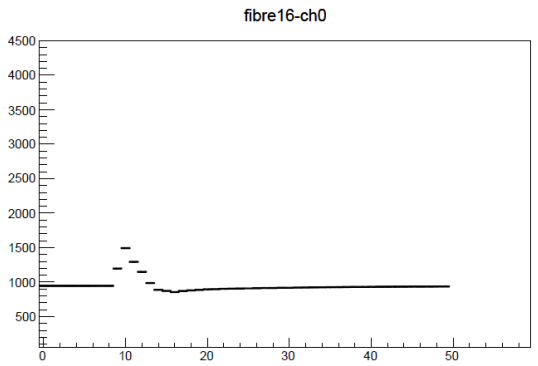
Run 323511 (16th of May) – FPGA 20:2 (BNL LTDB)

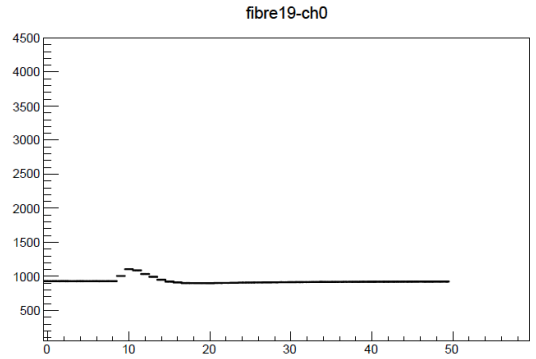








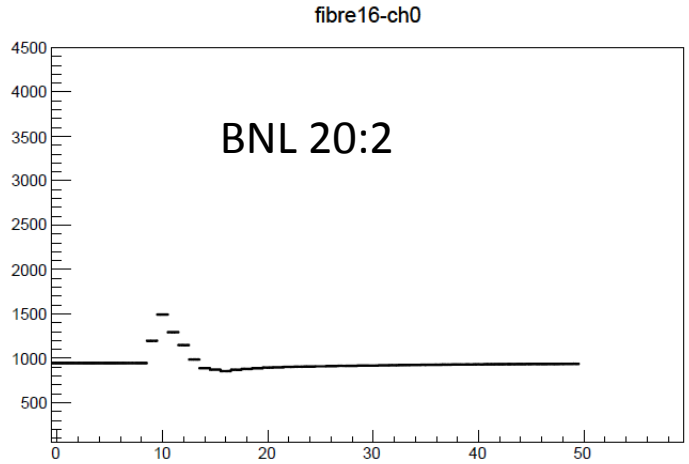


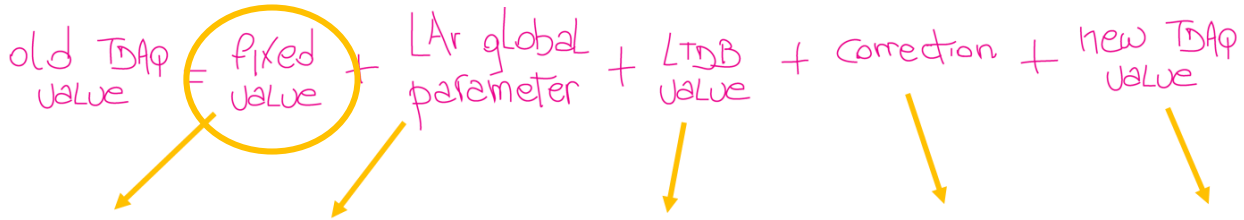


Conclusion

- BNL pulses are stable

- The latency setting inside the panel was set to 8 while the calibrations were taken
  - From the picture: the pulse peak is at 10
  - Before the official restart of the data taking the firmware will have to be recompiled
    - Fixed value has to be corrected: it is off by 2 BC





Set in the firmware and calculated to comply the LAr global and the new TDAQ value: it will be -46

For example, 104 for LAr Physics, to be set through TDAQ

Set in the firmware, it will be 8 for BNL LTDB and 0 for LAL LTDB, according to the latency between the two boards

Set in the firmware, it is the value explained previously

To have the pulse at position 20 in the readout window, this value will be set directly to 20 in the panel