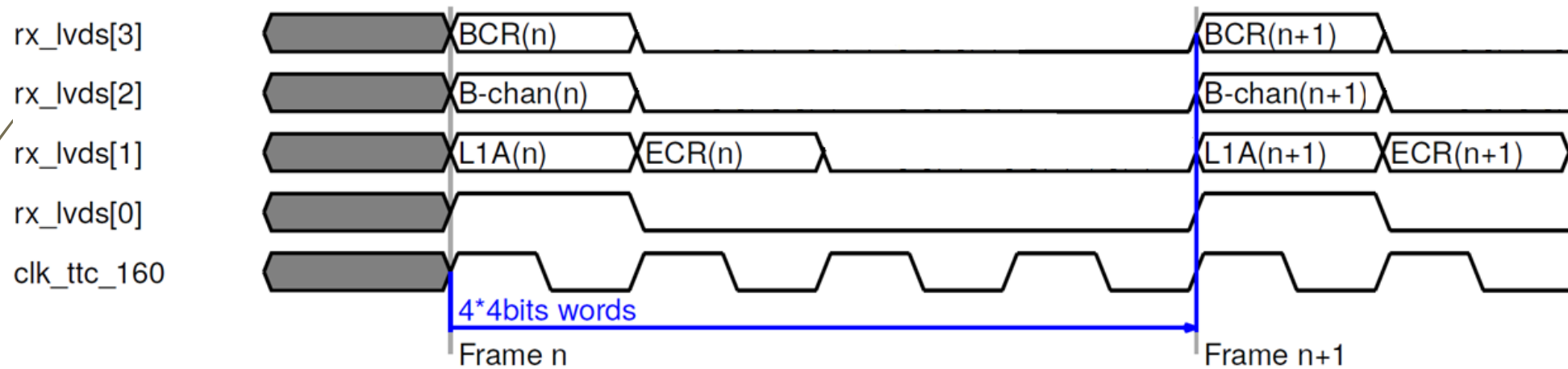# TTC decoding tests in EMF

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Expected protocol

Expected protocol between Carrier and Latome on the LVDS links:

Carrier and Latome onstraints

Carrier constraints

From an email from Kade:

«Keep in mind that this project, only extracts the TTC information, and forwards it to the AMC LVDS pairs. The Stony Brook ATCA Clock project is still required to setup the clock, as this isn't built in.»
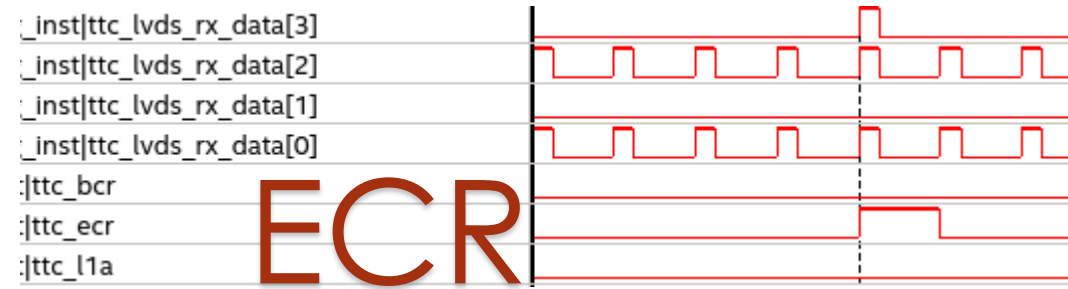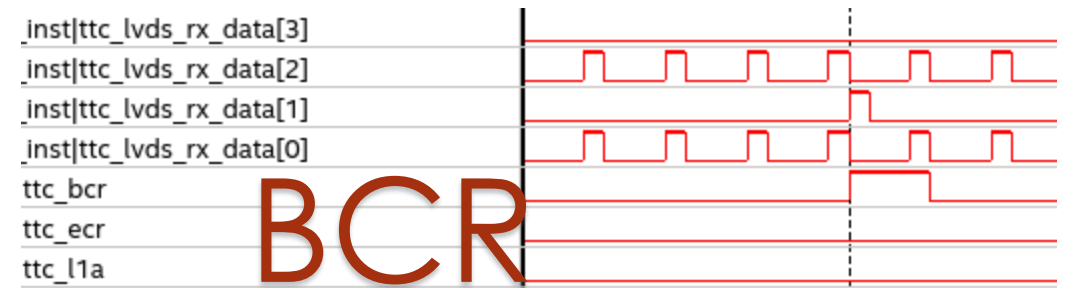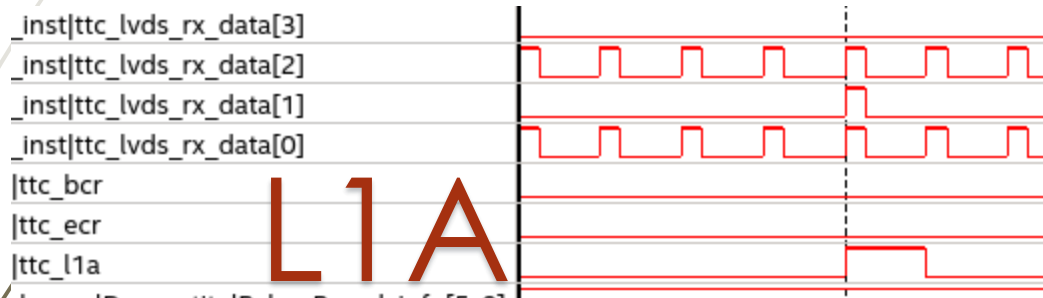
Latome constraints
- Added constraints between the input pin and the first register on the LVDS lines
- Falling edge in lli processes to be improved

From Nico DD email:

The "preserve" synthesis directive works to disable registers merging only for the LVDS registers. We will use it for the LVDS synchronization in the LLI/daq/lli_modules/lvds_interface (Nico DD email)

TTC signals decoding

- Constraints on the Carrier and Latome
- With a swap on pins for LVDS2 and LVDS3
- With lli processes working on falling edge
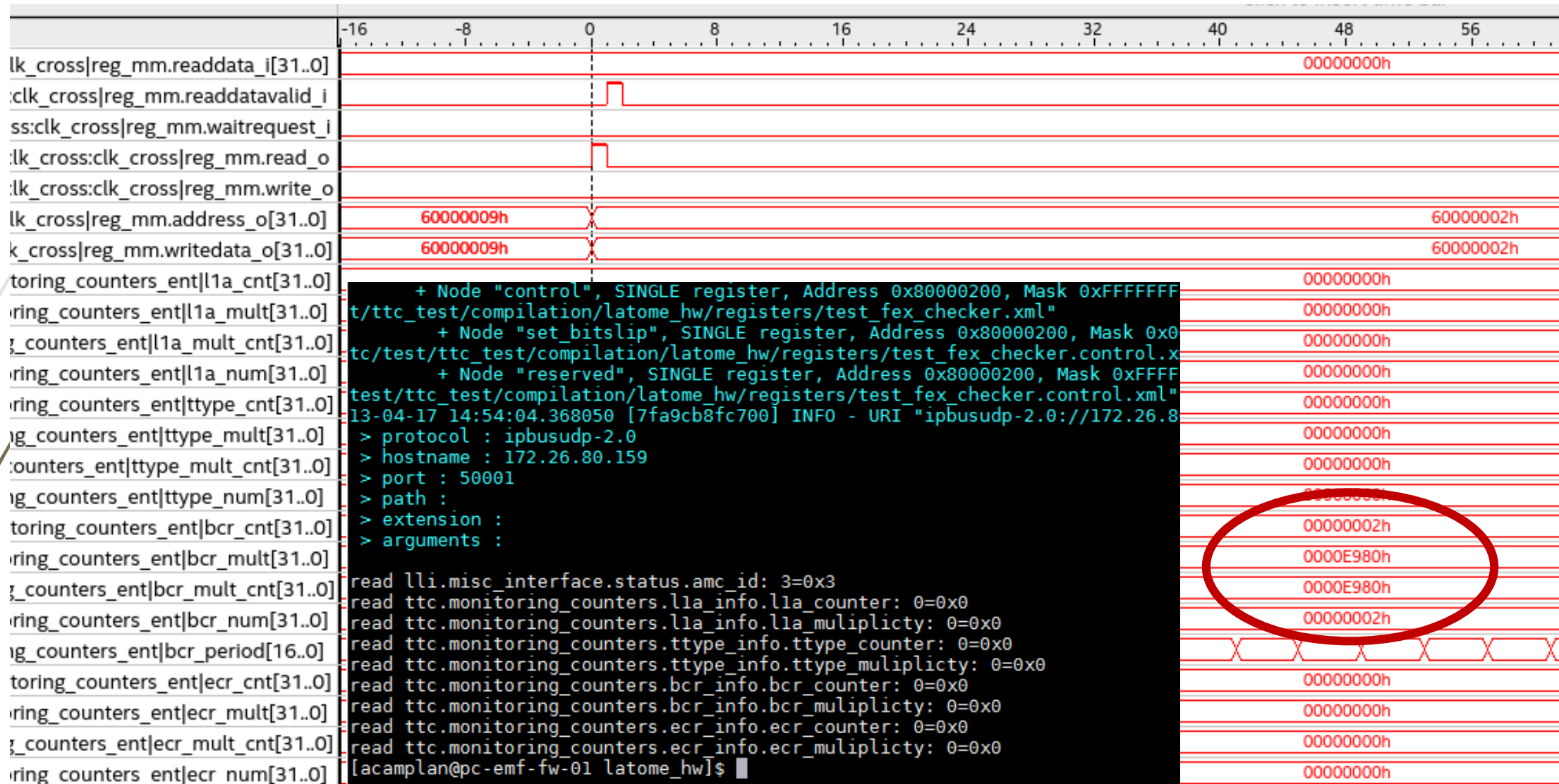- With a swap on ECR and BCR on firmware side

TTC signals decoding (2)

- Constraints on the Carrier and Latome
- With a swap on pins for LVDS2 and LVDS3
- With lli processes working on falling edge
- With a swap on ECR and BCR on firmware side
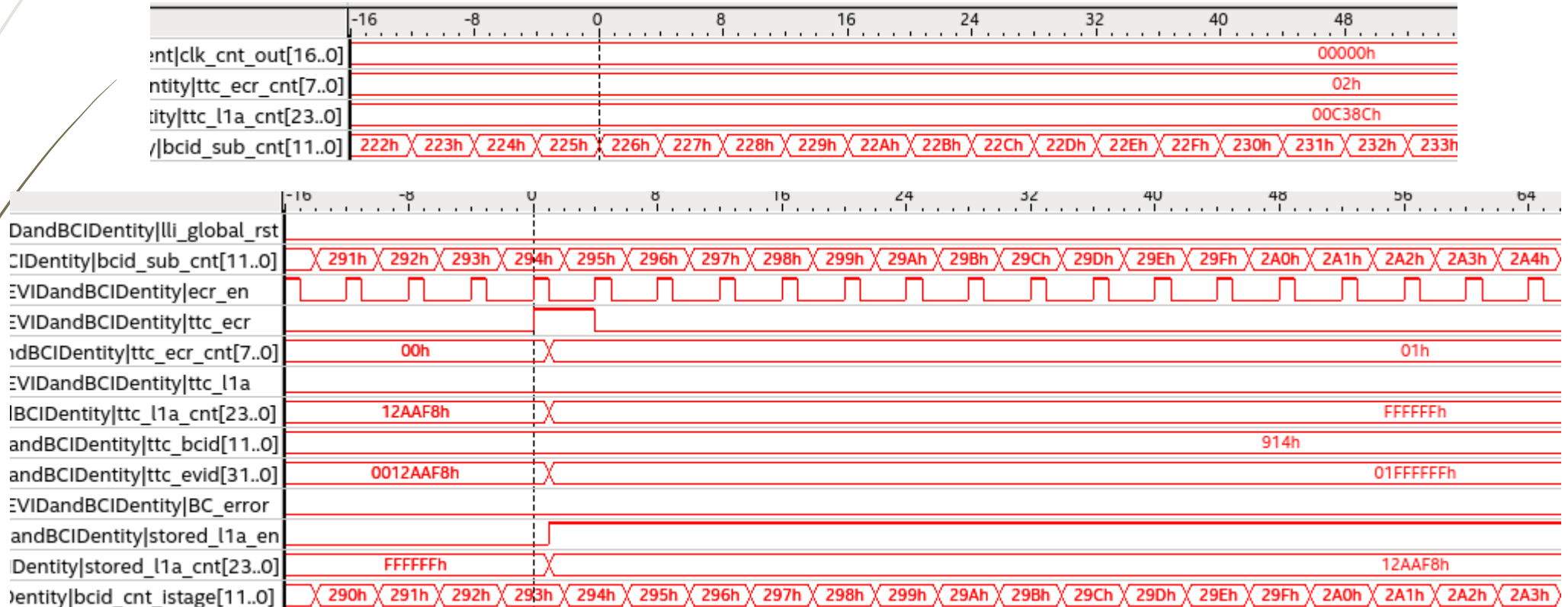
TTC registers

Conclusions

➢ **We are improving! Thanks to everybody!**

➢ **L1A, ECR, BCR** received properly and decoded
   ➢ Ttype still to be checked but bchannel broadcast and long address are visible
➢ Improving with the TTC **registers**
   ➢ Implemented and readable
   ➢ Still some troubles: reading zero instead of the correct value
➢ **Falling edge** is going to be addressed
➢ **Constraints** on both sides seems ok
➢ What about the **swap**?
   ➢ For the moment using a file provided by Nico C. with the swap

➢ **More tests**: run for some time and compare the counters value (for L1A, BCR, ECR and TType) in the partition and in the registers

   ➢ Latome not respoding after few minutes