ABBA firmware status

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Firmware version

Last firmware versions presented **during the Upgrade Week** in April 2016:

- front FPGA: **v0.95b**
- back FPGA: **v0.68a**

For more details
Upgrade Week: ABBA firmware status

Current versions used to take data:

- front FPGA: **v0.96**
- back FPGA: **v0.69a**

Improvements in front FPGA

- **Test firmware version: v0.95b1**
  Solved "critical warnings" for timing constraints and improved reset structure in front fpga firmware

- **Test firmware version: v0.95b2**
  Changed reset from asynchronous to synchronous in front FPGA top level processes

- **Test firmware version: v0.95b3**
  Reorganisation of writing procedure for front FPGA registers (to simplify the code)

- **Test firmware version: v0.95b4**
  Combination of writing and reading procedure for registers: new entity defined (to simplify the code)

- **Test firmware version: v0.95b5**
  Changed reset from asynchronous to synchronous in IPBUS front FPGA files

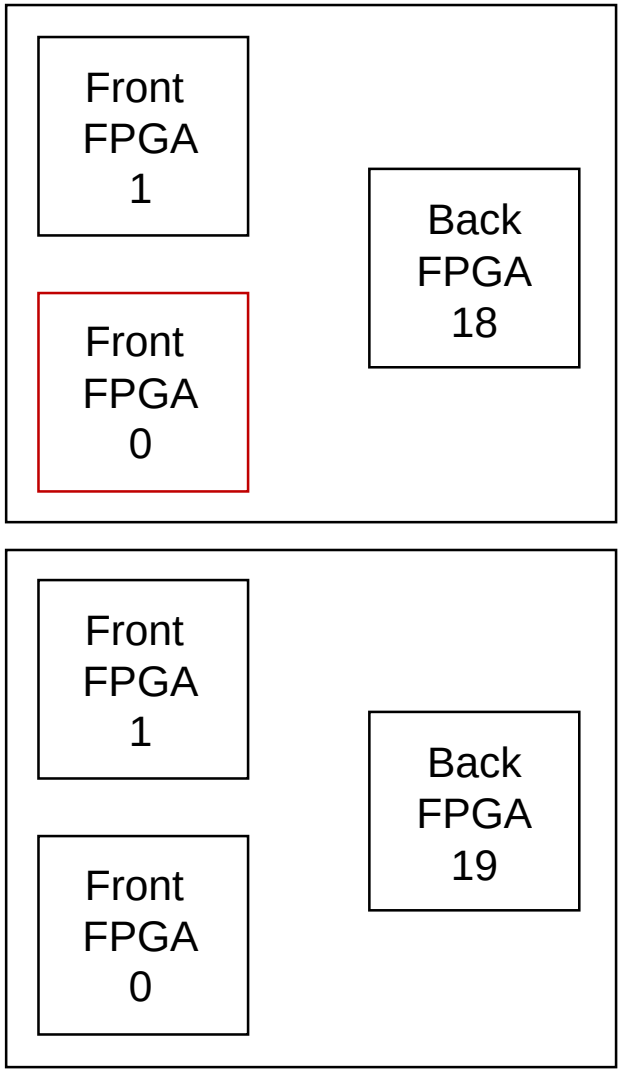
➢ After some tests, **v0.95b5 (test)** upgraded to production version **v0.96**

Known issue with FPGA 18:0 in USA15 (part 1)

In USA15:
- two “identical” ABBAs
- 3 “identical” FPGAs per board (all Stratix IV from ALTERA)
  - 2 front FPGAs
  - 1 back FPGA

All **4 front FPGAs** using the **SAME firmware** version:
➢ **only one not responding** (FPGA 18:0)

Reminder from ATLAS Upgrade Week:
- FPGA 0 from ABBA 91.18 was sending some random data that affect FPGA 1 on the same board, but also the other board
  ➢ v0.68a: length check in UDP and IP module now avoids transmission of garbage!
    ➢ Stabilized readout with 3 remaining FPGAs



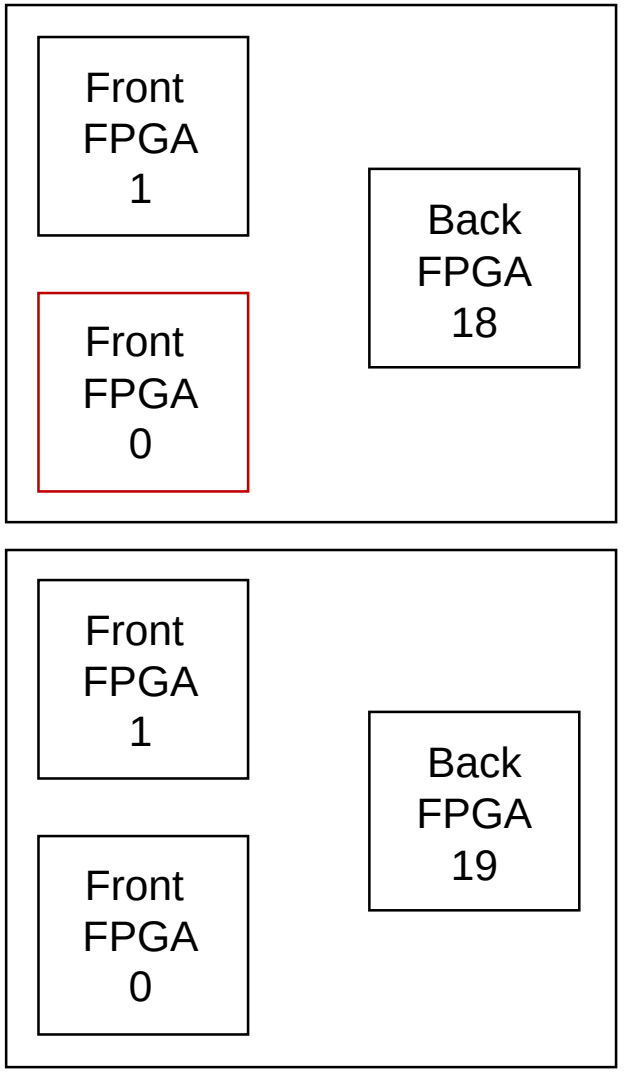
Known issue with FPGA 18:0 in USA15 (part 2)

Issue hidden but not solved …

Looking with **Signal Tap** Altera tool in front FPGA:

- the signal which is blocking if the FPGA is *aligned_status:*
  - coming from the ALTERA XAUI CORE
  - connected to *channelaligned* signal in the back FPGA interface

The issue is coming from the **communication between front and back** FPGA.



Known issue with FPGA 18:0 in USA15 (part 3)

To solved this issue **different strategies** have been adopted:

- Solved timing critical warnings
- Used a different (better) clock source: oscillator
- Improved reset structure
- Changing reset in most important processes from asynchronous to synchronous

➢ **All these attempts didn't solve the issue.**

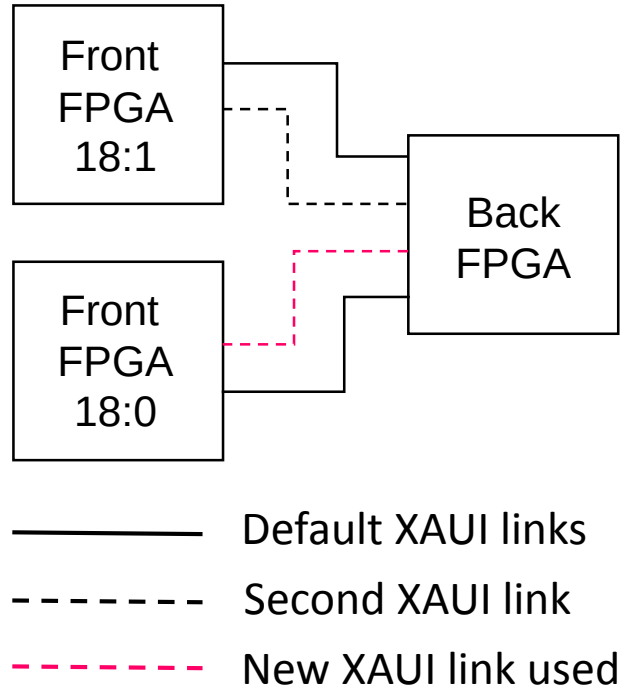
Last chance was:
Two pairs of XAUI transceivers interconnecting front and back FPGAs on ABBA

➢ Tried the second XAUI transceiver

Neither this solution recovered the FPGA.

➢ **Conclusion**: hardware issue (also the TTC is behaving differently here!)

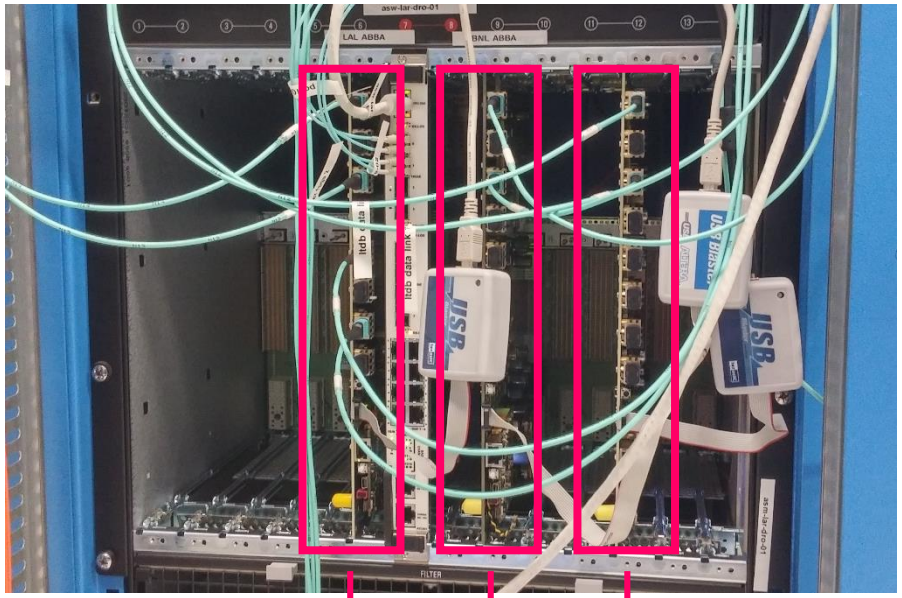
➢ **Finally (27/05/2016)**: added a new ABBA in USA15 to substitute FPGA 18:0



Improvements in back FPGA

Firmware version v0.69:

- Back FPGA **STP file and constraint files reworked**:
  - no more timing warnings
  - no more unconstrained paths
  - no complaints of unconnected signals in Signal Tap
- Minor update in **interface merger process** (sensitivity list) for ready signal



Firmware version v0.69a:
As said before, **another board** has been installed in USA15.
New IP and MAC addresses added in the firmware.

Added a **new item to the MAC_IP_selector** generic:

- selects the pair of MAC and IP address of the Back FPGA

Actually back FPGAs with IP -.18 and -.19 are using (and can remain with) version v0.69.

Only FPGA with IP -.20 is using version v0.69a.

Conclusion and outlook

- **v0.69a** for the back FPGA and **v0.96** for the front FPGA: **STABLE!**
  - No needs to reprogram the FPGAs during the data taking

- Issue with FPGA 0 on ABBA 91.18 in USA15
  - After many trials **new (Oregon) board installed**
    - Previously installed in EMF
  - No firmware (or hardware) issues on the new board

- **Collecting data with all 4 FPGAs**

- **Next step:**
  - Some data already analysed: found bad readings
    - ➢ To be investigated …