ABBA firmware (and partition) status

Alessandra Camplani – Università degli Studi di Milano

05/07/2016

Improvements in front FPGA

- **Version v0.96b**
  - Solved all the remaining timing constraints (thanks to Kenta!)
- **Version v0.96b1 (test version)**
  - Improved reset structure: several soft_resets are now available to reset different interfaces, registers and counters (more details in the next slides).
  - New registers implemented.
- **Version v0.96c**
  - Released version for v0.96b1

New reset structure in front FPGA

A **new reset structure** has been implemented and is now available in front FPGA firmware.

The **soft_resets signal is a 32 bit vector** and each bit is able to reset a specific register/counter/memory in front FPGA firmware (more detailed table in the next slide).

These resets can be used from the **standalone tool**, selecting the command **“fpga_reset”** and the FPGA:

- ./fpga_resets 10.145.91.19 1

A **hexadecimal parameter** will be required for the reset, for example:

- *1f* to reset LTDB interface
- *7f00* to reset ABBA configuration
- *1000000* to reset the TTC decoder
- *60000000* to reset the interface to the back FPGA

These resets are now also implemented in the **ABBA partition** at CONFIG and START level.

Available soft_resets bits

byte	bit	reset name	dedicated to
0	0	rst_int_ltdb	LTDB interface
	1	rst_mem_ltdb	
	2	rst_reg_ltdb_ctrl	
	3	rst_reg_ltdb_dec	
	4	rst_cnt_ltdb_err	
	5		
	6		
	7		
1	8	rst_reg_l1a_latency	ABBA configuration
	9	rst_mem_abba	
	10	rst_reg_header	
	11	rst_cnt_l1a	
	12	rst_cnt_pkg_write	
	13	rst_cnt_pkg_diff	
	14	rst_cnt_pkg_sent	
	15		

byte	bit	reset name	dedicated to
2	16		
	17		
	18		
	19		
	20		
	21		
	22		
	23		
3	24	rst_int_ttc	TTC interface
	25	rst_int_AV	avalon interface
	26	rst_int_XAUI	XAUI interface
	27	rst_int_osc01	(not yet implemented)
	28	rst_int_osc23	oscillator interface
	29		
	30		
	31		

New registers implemented

Two new registers have been implemented in the front FPGA firmware to monitor the packets:

Register name	Register address	Internal variable name	Read_counters interface name
L1A_TTYPE_CNT_REG_ADD*	16011	l1a_ttype_cnt	l1a received counter
L1A_ADC_PACKET_WR_CNT_REG_ADD	16013	l1a_adc_packet_wr_cnt	l1a packet built counter
L1A_ADC_PACKET_RD_CNT_REG_ADD	16014	l1a_adc_packet_rd_cnt	l1a packet trasmitted counter

* was called L1A_TTC_CNT_STATUS_REG_ADD and was used for both l1a received counter and l1a packet built counter.

Also in this case, the counters can be displayed from the **standalone tool**, with the command "**read_counters",** selecting the FPGA:

- ./read_counters 10.145.91.19 1

They are also available now on the **ABBA partition panel** per each FPGA that is recording data.

Latency and n°samples changes

Two major changes in the default settings for **ABBA partition** have been done on 28 June:

- **Number of samples** read out changed to 50 (instead of 60)
  - Changed done to because we were losing 50% of data
  - After this change data lost were only 1…5 (after 200 ... 300 events)

- **Latency settings** changed to 0x42 (instead of 56, for all fibers):
  - Changed done because the pulse tail is partially cut
  - Moving the pulse into the new readout window
  - Result of this change presented in the next slides

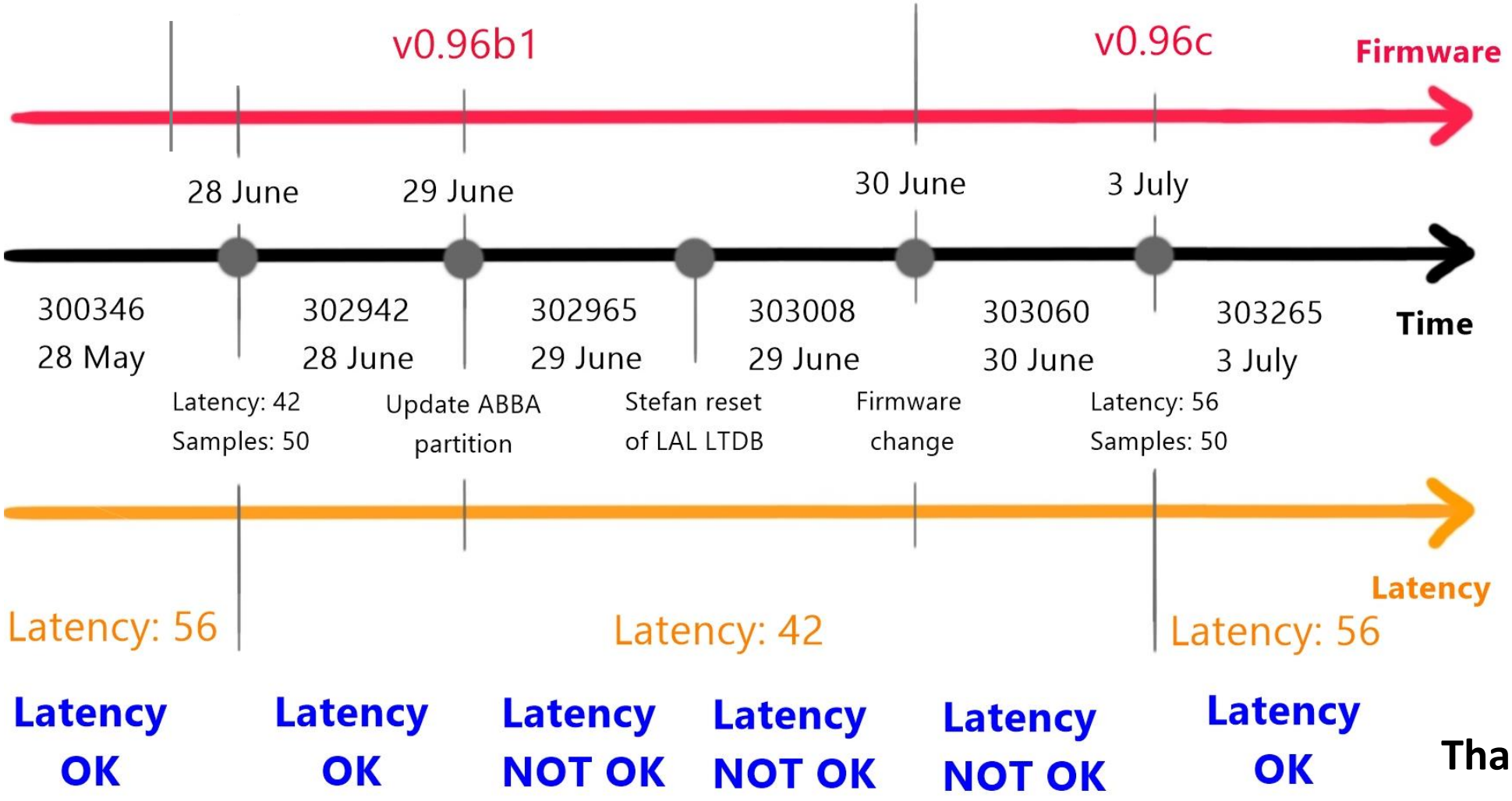
Latency settings issue (1)

After the latency change **some issues have been found**.
More details about the starting sample for the pulses are shown in the table:

	Pulse starting at sample....			
	28 May **run 300346** **latency = 56**	**28 June** **run 302942** **latency = 42** **before partition update**	**30 June** **run 303060** **latency = 42** **after partition update**	**3 July** **run 303265** **latency = 56** **after partition update**
LAL LTDB	28	33	sample 6	28
BNL LTDB	20	25	sample 0 or before	19

More tests to be done (in EMF) to find the reason of this behaviour!

Latency settings issue (2)



Thanks to Adriana!

Conclusion and outlook

- **Stable data taking**: no need to send reset or reconfigure the FPGAs.

- **New firmware versions** for front FPGA**:**
  - Timing constraint solved
  - New reset structure
  - New registers for packet monitoring

- **Solved**: bad readings in the first sample
  - Thanks to the new reset structure in front FPGA firmware

- **Ongoing**
  - Latency check and pulse position to be understood
  - Still searching the reason of the HOP

BACKUP SLIDES

Updates in ABBA partition

Last updates in ABBA partition:

- **27 June**
  Loaded v0.96b1 on all our 4 Front FPGAs of the ABBA and applied a TDAQ patch for the ABBA package to use the new firmware features.

- **28 June**
  The transition Stop -> Start was not enough to bring back ABBA into normal data taking mode. Instead the transition Stop -> Unconfig -> Config -> Start is the way to go.

- **29 June**
  New patches have been added to:
  - restore the standart transition Stop -> Start for data taking (more details in next slides)
  - read the l1a received counter
  - read the l1a packet built counter
  - read the l1a packet trasmitted counter

Reset in ABBA partition

1. **at pressing CONFIG**
   - Issue reset 0x01_FF_FF_FF
   - Read back the "configuration fully done" register: Expect 0.
   - Configure all settings (TType, # samples etc.)

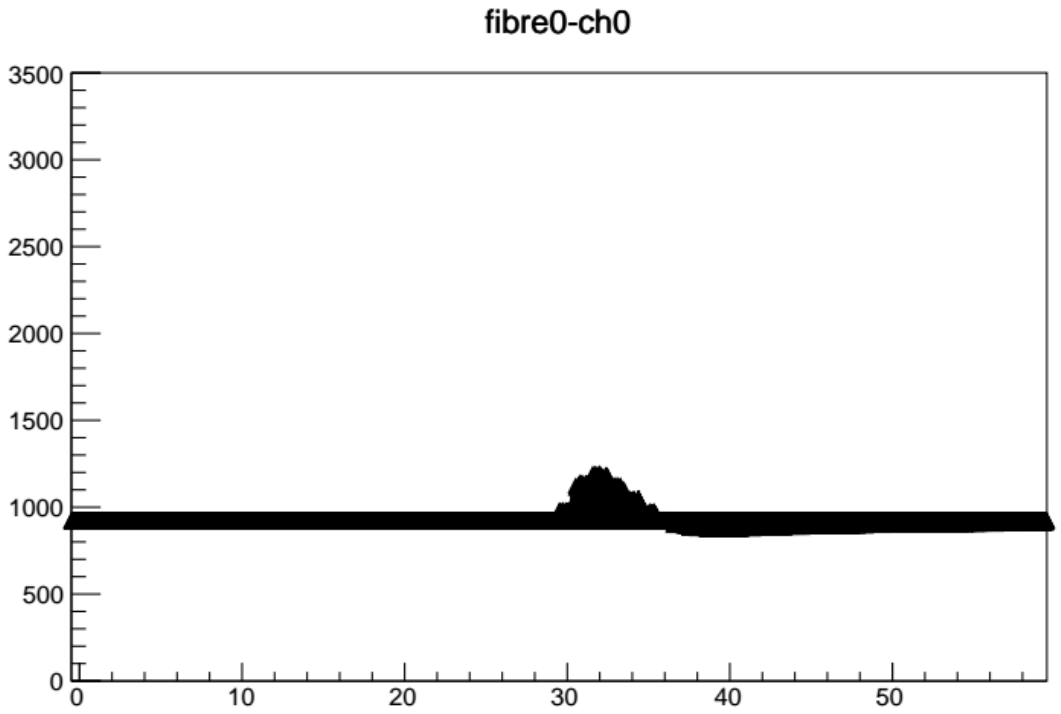
2. **at pressing START:**
   - At prepare for run reset value 0x7**A** 00
   - Set "configuration fully done"; read back, expect 1

3. **at pressing STOP:**
   - Nothing, should remain how it is now

4. **at pressing UNCONFIG:**
   - Unset "configuration fully done"; read back, expect 0

Pulses position

Run 302611 (22 june)



Run 303060 (30 june)