TTC decoding tests in EMF

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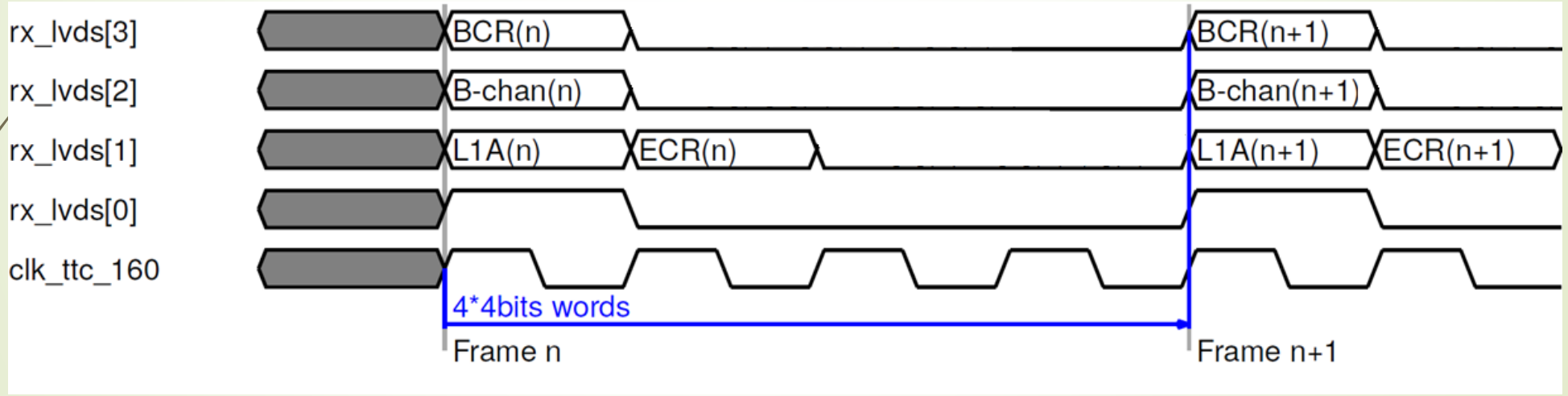
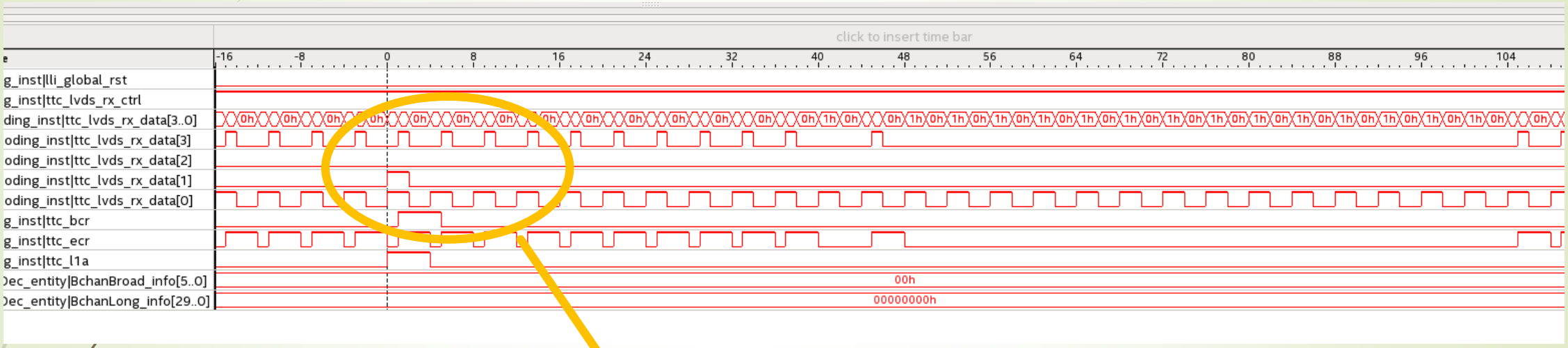
Expected protocol

Expected protocol between Carrier and Latome on the LVDS links:



Signals on Latome (test during LAr week)



Input signals of ttc_decoding module

Constraints and code updates

- Changed clk edge in lvds interface processes
- Added constraints between the input pin and the first register on the LVDS lines

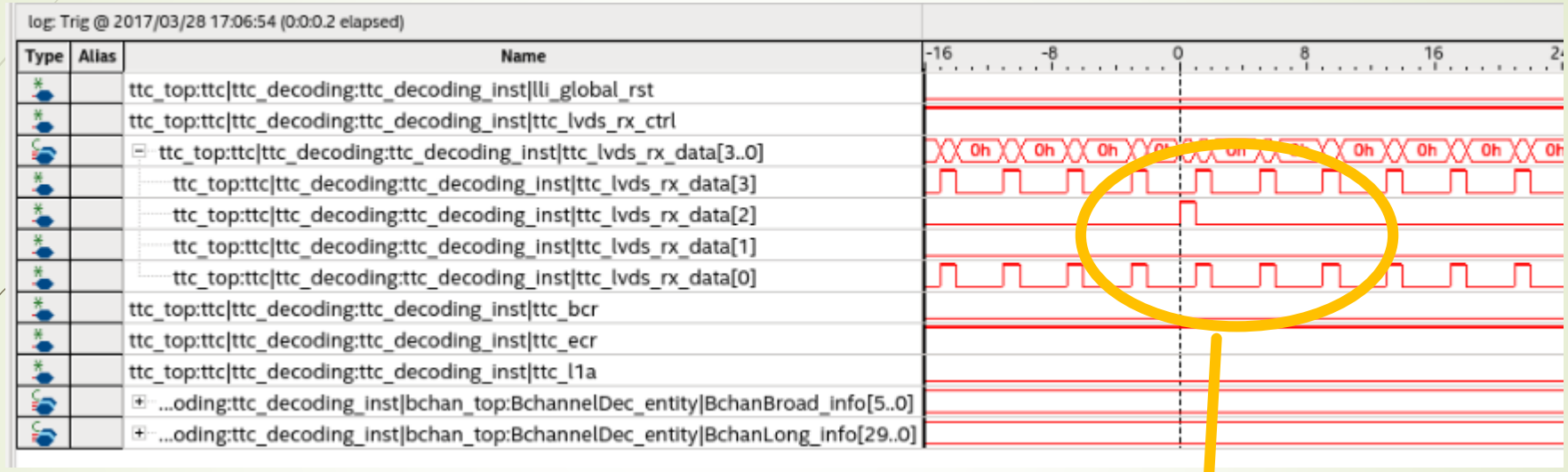
LATOME/src/lli/daq/lli_modules/lvds_interface/top/lvds_interface.vhd

```
...  ...  @@ -117,7 +117,7 @@ begin
117  117      begin
118  118          if async_rst = '1' then
119  119              lvds_rx_data_reg <= (others => (others => '0'));
120       -      elsif rising_edge(ttc_160_clk) then
     120  +      elsif falling_edge(ttc_160_clk) then
121  121              lvds_rx_data_reg <= lvds_rx_data_reg(0) & rx_lvds;
122  122          end if;
123  123      end process;
...  ...  @@ -126,7 +126,7 @@ begin
126  126      --! @details Pipeline LVDS valid for 2 clocks cycles
127  127      lvds_rx_valid_proc : process(ttc_160_clk)
128  128      begin
129       -      if rising_edge(ttc_160_clk) then
     129  +      if falling_edge(ttc_160_clk) then
130  130              lvds_rx_valid_reg <= lvds_rx_valid_reg(0) & not (async_rst);
131  131          end if;
132  132      end process;
```

LATOME/src/fpga/targets/latome_hw/io_logic_options_assignments.tcl

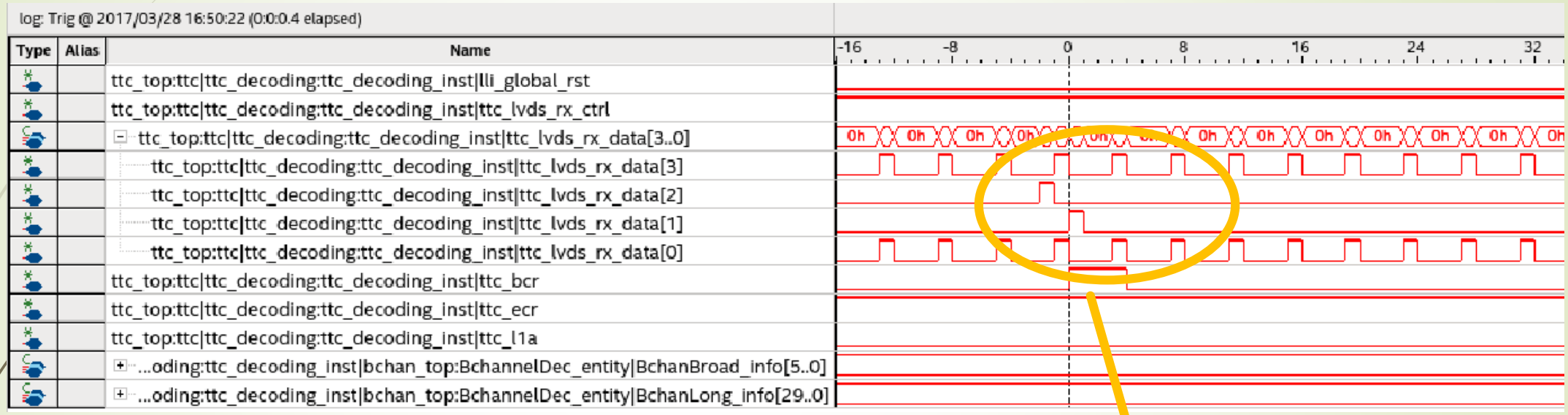
```
...  ...  @@ -14,6 +14,13 @@ while {$i<$LVDS_TTC_BUS_WIDTH} {
14   14       incr i
15   15   }
16   16
     17  + set_global_assignment -name ALLOW_REGISTER_MERGING OFF
     18  + set_instance_assignment -name FAST_INPUT_REGISTER ON -to lli_top:lli|lli_lvds_interface_top:lli_lvds_interface|lvds_rx_data_reg[0][0]
     19  + set_instance_assignment -name FAST_INPUT_REGISTER ON -to lli_top:lli|lli_lvds_interface_top:lli_lvds_interface|lvds_rx_data_reg[0][1]
     20  + set_instance_assignment -name FAST_INPUT_REGISTER ON -to lli_top:lli|lli_lvds_interface_top:lli_lvds_interface|lvds_rx_data_reg[0][2]
     21  + set_instance_assignment -name FAST_INPUT_REGISTER ON -to lli_top:lli|lli_lvds_interface_top:lli_lvds_interface|lvds_rx_data_reg[0][3]
     22  +
     23  +
```

Signals on Latome (test this week)

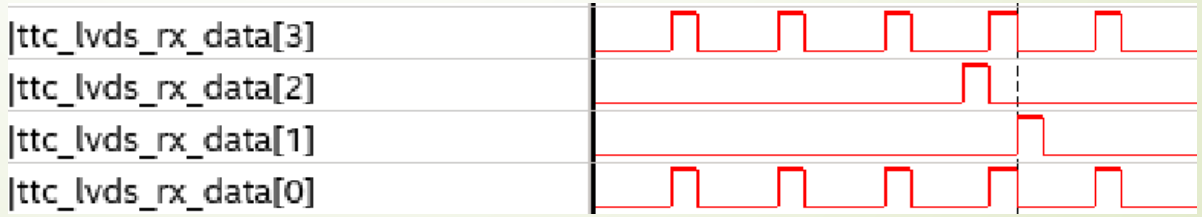


Input signals of ttc_decoding module
This is obtained requesting a BCR signal on TTCvi..

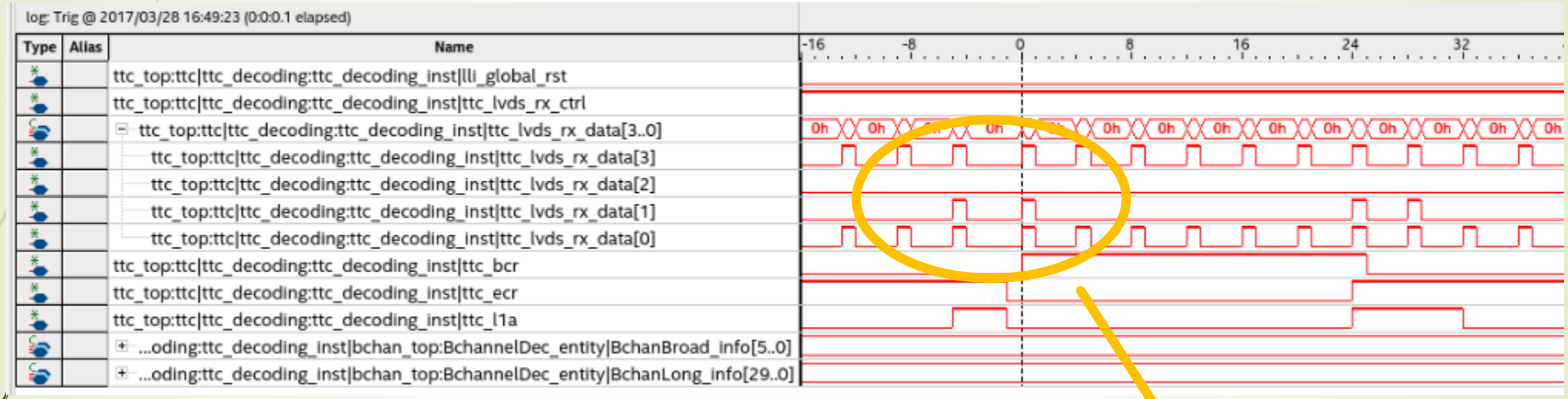
Signals on Latome (test this week)(2)



Input signals of ttc_decoding module
This is obtained requesting both ECR and BCR signals on TTCvi..



Signals on Latome (test this week)(3)



Input signals of ttc_decoding module
Immediately after requesting ECR and BCR signals on TTCvi..

Conclusions

- We are improving!
- Thanks to Nico&Nico and Ken
  - Pins check
  - Constraints check on the Carrier as well
  - Implementation of registers to monitor the counters (for M4)
- More debug on my side with the simulation
  - Locked state to be better checked (to avoid issues if the sync period is longer)
- Some more test will be done in the next weeks