Using polygons in EAGLE

POLYGONS are needed for a number of different tasks in a PCB design:

1. As a ground plane under RF lines like microstripe or coplanar lines.
2. As a power plane (for example Vcc) and/or groundplane, to create a low resistance connections.
3. Generally to make a low resistance connection for tracks that carry a high current.

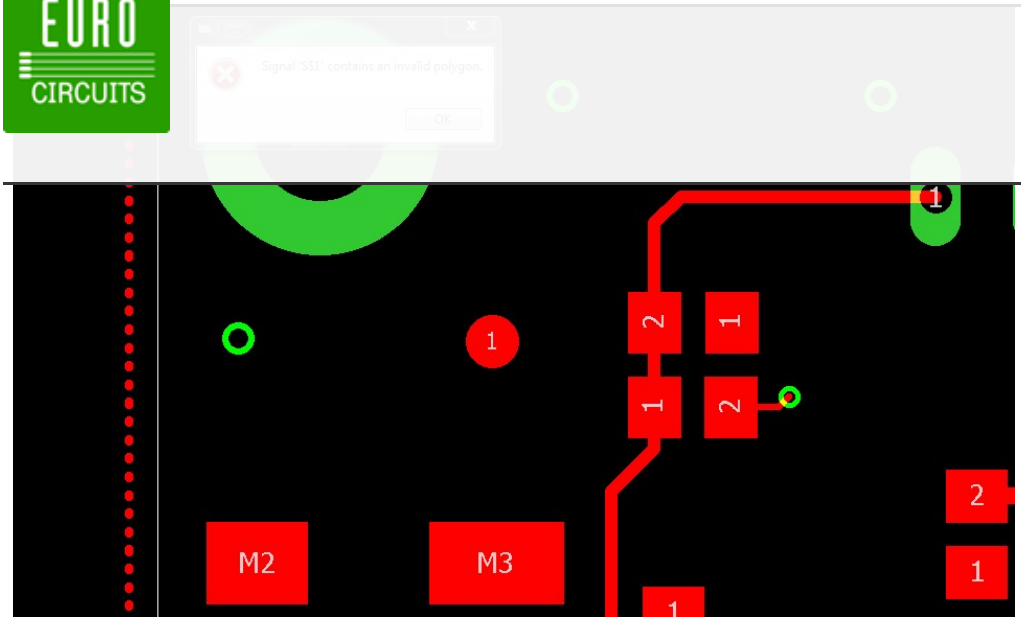
To define a valid POLYGON in EAGLE you must follow some rules:

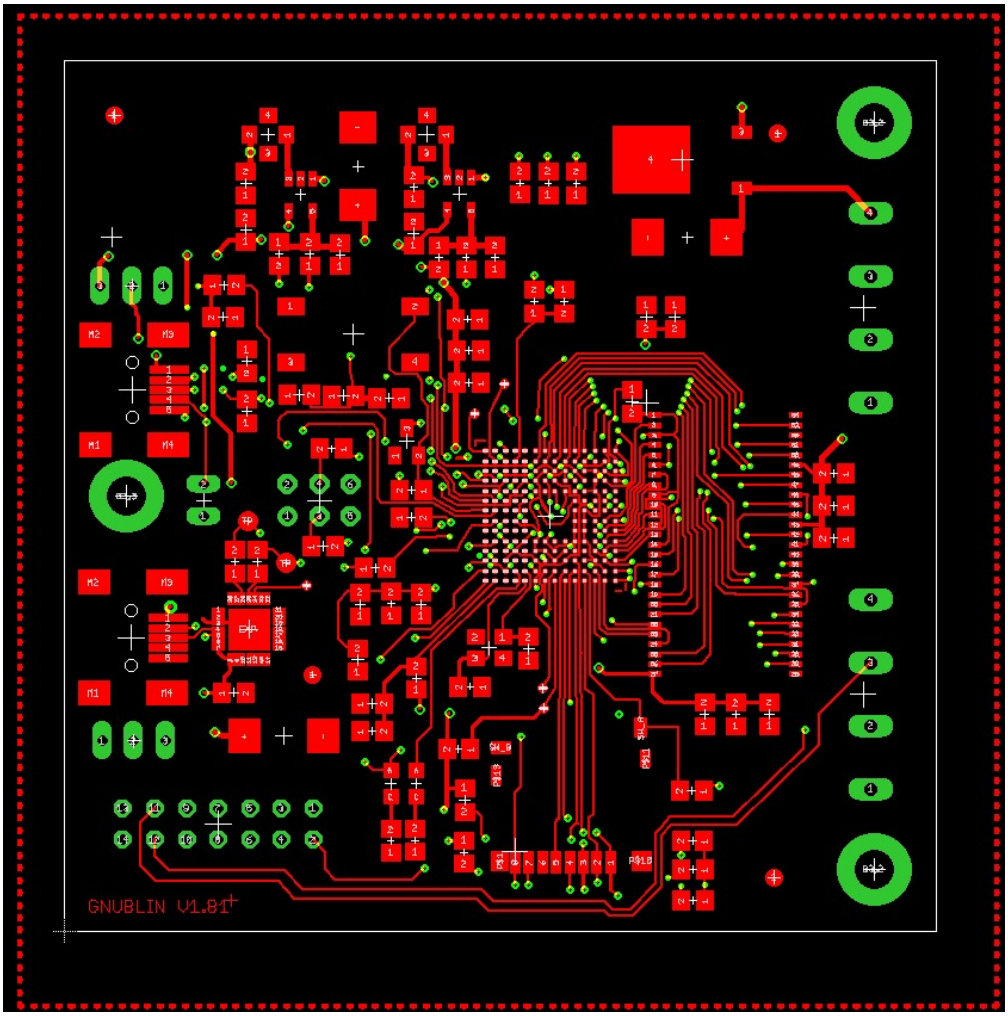
1. The POLYGON outline must be a closed contour. The contour must be drawn in the correct sequence and with one line. It cannot be built up in sections. When you have drawn the complete closed contour, the outline changes from a solid to a dotted line.
2. A valid POLYGON should not overlap itself.

Use the RATSNEST command to calculate and display the surface of the Polygon. Type in the command Line “Ratsnest” or use the Command button.

A Polygon which overlaps itself cannot be calculated. An Error Message will appear: “Signal contains an invalid Polygon”.

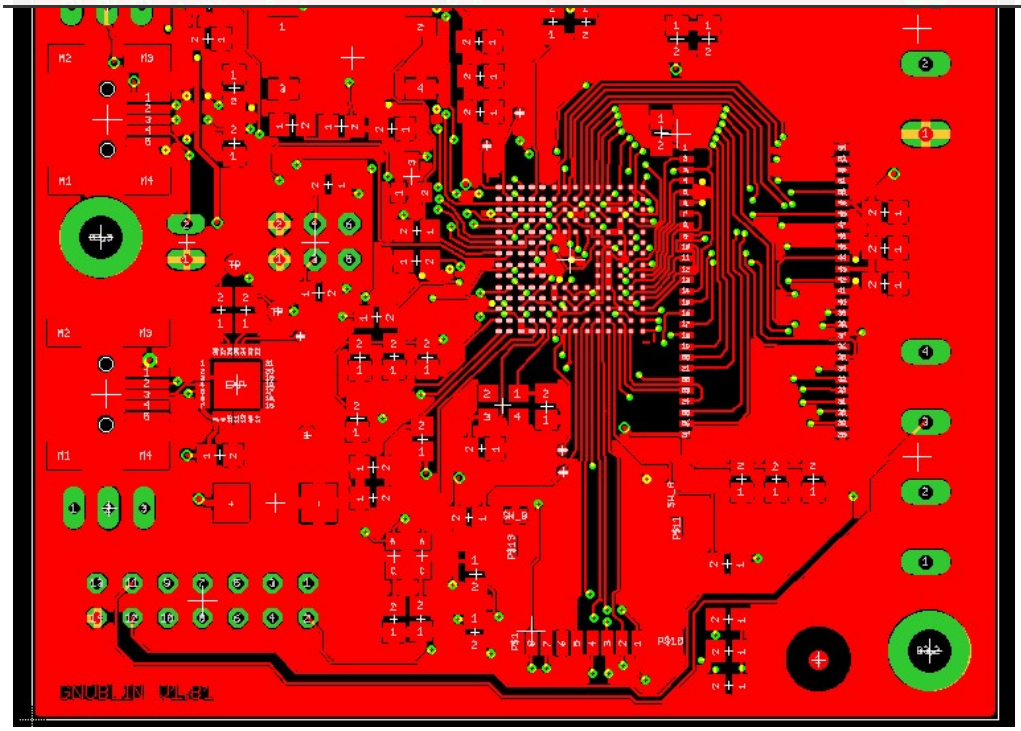
Contact support



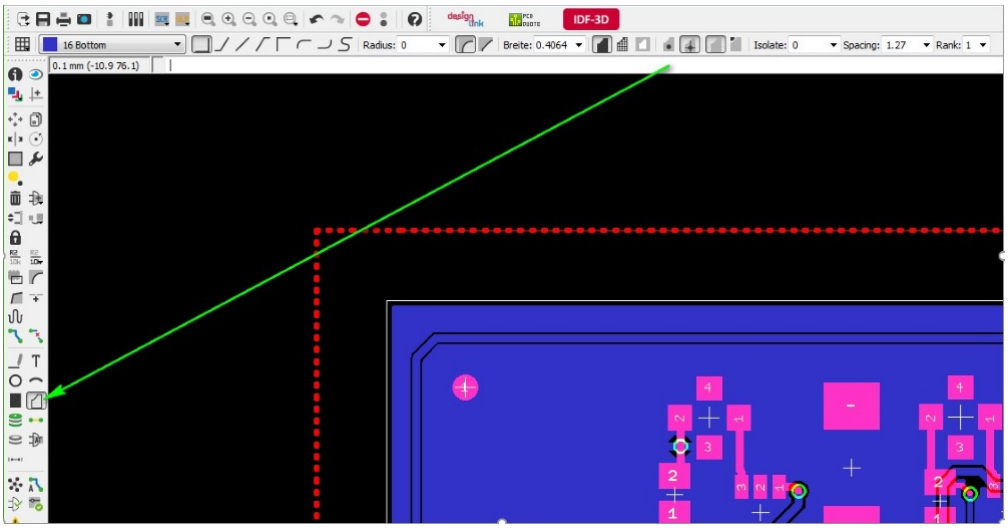


When you have solved the error use the RATSNEST command again, to calculate and display the surface of the POLYGON. Use RIPUP @ ; to switch back to outline mode.

Contact support

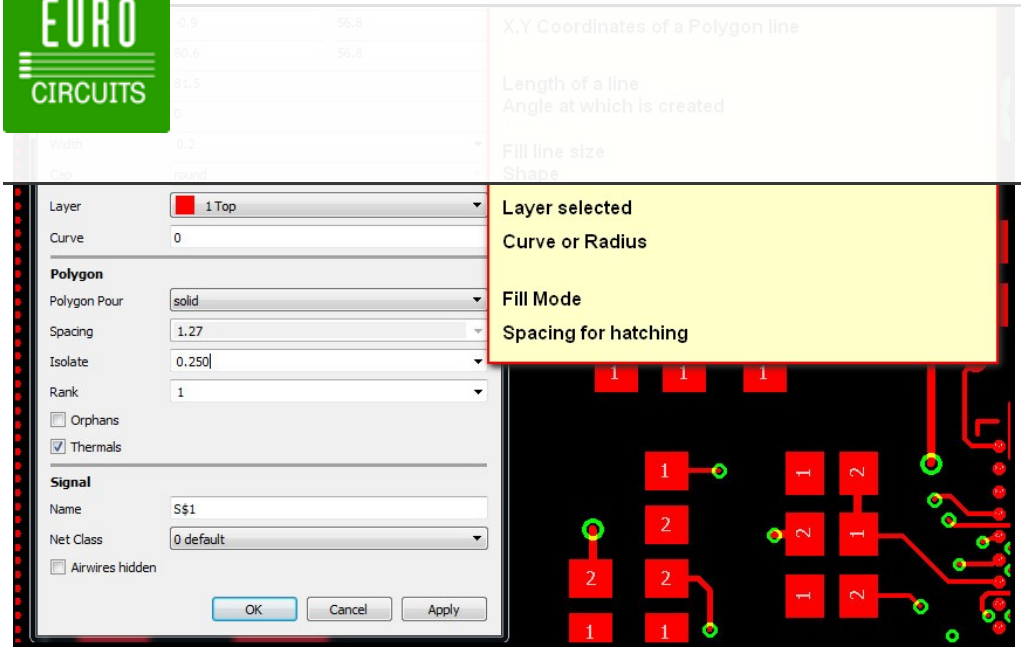


Polygon options can be changed via the parameter toolbar



Or, under Properties, right click on the POLYGON outline.

Contact support

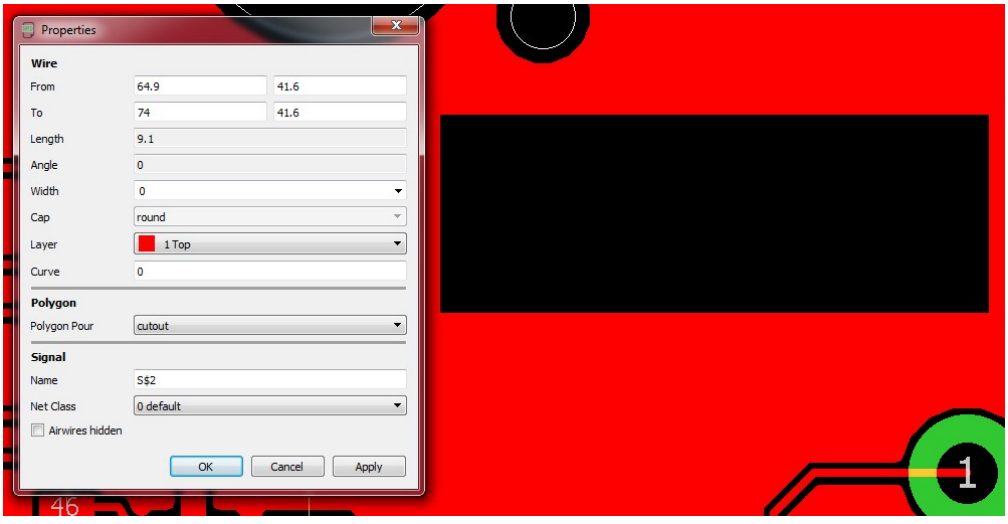


Width – specifies the thickness of the line used to fill the POLYGON.

> **TIP:** Select the largest possible line width. Too fine lines create unnecessarily large files when you output the data for manufacture. In any case the line used to fill the polygon should never be less than the minimum line width in the layout.

Polygon pour – specifies the fill type. The preferred fill is a whole area (Solid) fill, but you can also select a grid (Hatch) fill. If you choose Hatch fill, make sure that you set a suitable value under Spacing. The combination of line width and spacing must leave openings large enough for production. You can find more information in our PCB Design Guidelines

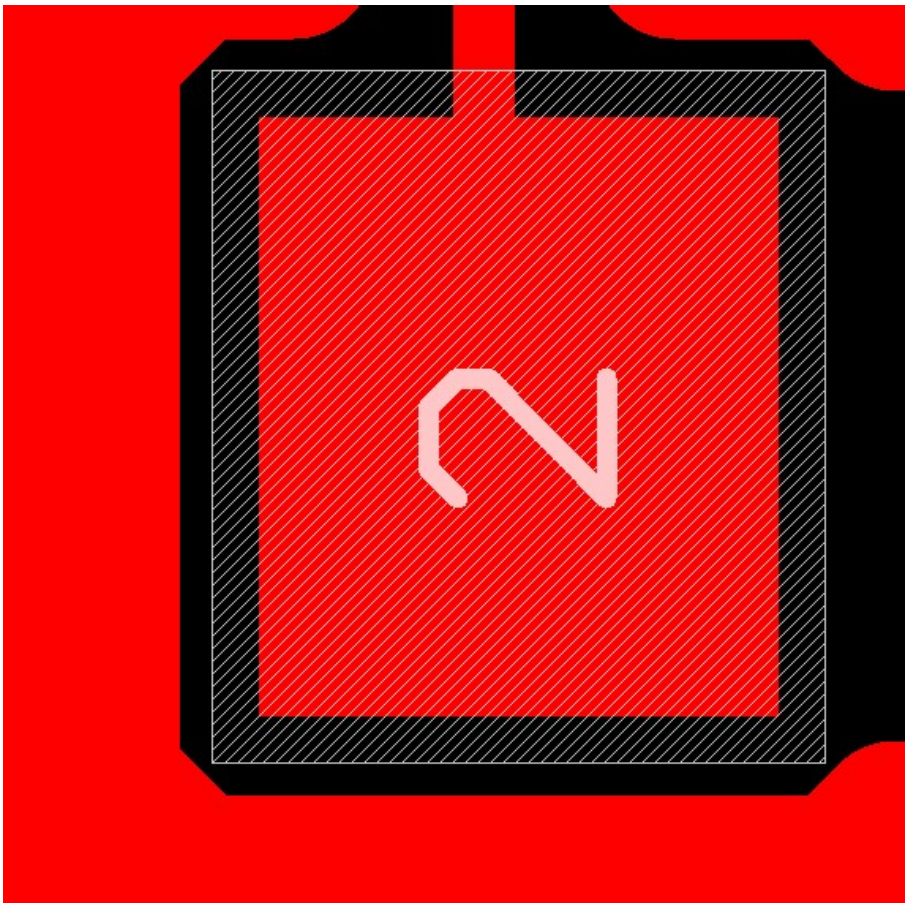
The special type CUTOUT is used to define POLYGONS that are cut out (subtracted) from all other signal POLYGONS within the same layer. **Cutouts are typically used to define restricted areas in polygons on inner signal layers. It is the only case where a POLYGON can be drawn with a line of width "0". The CUTOUT option is only used to define the open space and therefore it does not generate additional data.** Draw a Polygon and set the option in Properties to Cutout. Run again the command Ratsnest and the Polygon with open space is displayed.



Contact support

al signal or objects in the Dimension, tRestrict or bRestrict layer. Set the value to 0 if you want to use value defined in the DRC Rules. If there is enough space in the layout, we recommend a minimum ween plane and copper of 0.25mm. The soldermask window around a pad is typically 0.1 mm on all sides. An isolation distance of 0.25 mm compensates for any manufacturing tolerance when the soldermask is applied and ensures that there are no exposed areas on the copper plane which could short to an adjacent pad. For tight complex designs, we can accept smaller values. Check our PCB Design Guidelines for Soldermask to choose a tolerance.

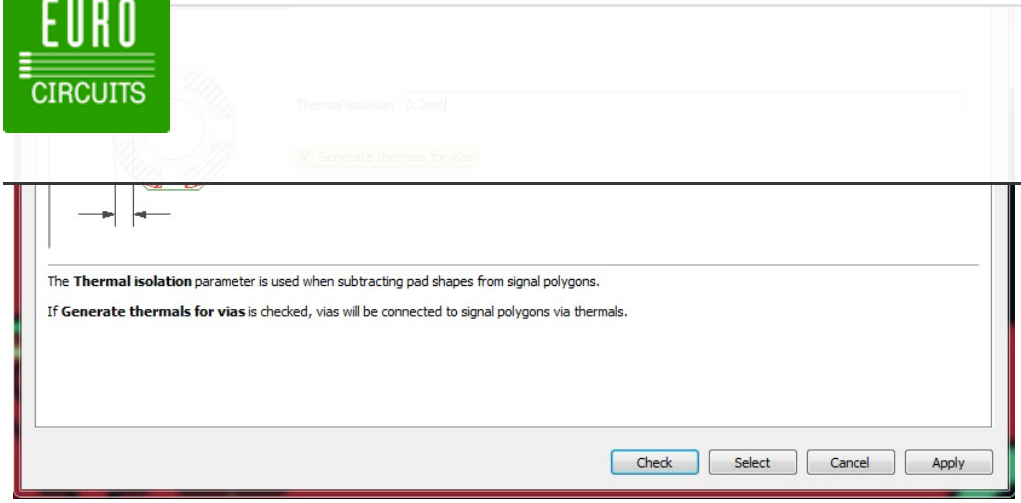
Picture below shows the standard soldermask window around a pad – 0.1 mm on all sides.



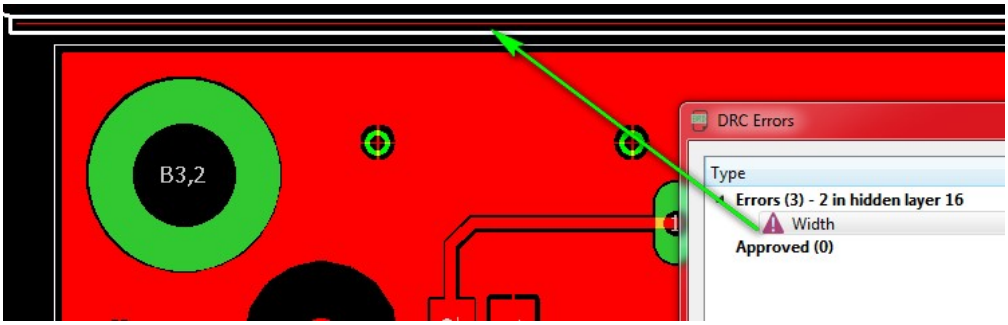
Rank – set values in this box to prevent overlapping POLYGONS from creating shorts. The Rank value determines which POLYGONS are to be subtracted from others. A POLYGON with rank = 1 has the highest priority in the Layout, so no other POLYGON drawn in the layout is ever subtracted from it. A POLYGON with rank = 6 has the lowest priority. If it is overlapped by a higher rank polygon the overlap area is cut out from the lower ranked POLYGON. POLYGONS with the same rank are checked by the DRC to ensure that there are no shorts. The rank property works only for POLYGONS with different signals. Overlapping POLYGONS with the same signal names are simply drawn one over the other.

Thermal – determines whether pads and drill holes in the POLYGON are connected using Thermal relief pads, or if they are connected directly to the copper plane. This applies to vias as well if the via option has been activated in the design rules.

Contact support



The width of the thermal connectors should normally be set as half of the pad"s drill diameter, with a minimum value of the wire width of the POLYGON and a maximum of twice the wire width. The length of the thermal connectors is defined by the Thermal isolation value in the Design Rules" Supply tab.



> **TIPS:**
> 1. Don"t set too fine a wire width for the POLYGON, or the thermal connectors won"t be able to handle the current load. The DRC will warn if this is the case (see illustration).
> 2. This also applies to necked POLYGONS. The minimum width of the copper area (neck) is determined by POLYGON'S wire width.

Orphans – Determines if a POLYGON may contain areas (islands) which are not electrically connected to the POLYGON"S signal. If **Orphans** is set to Off, such un-connected areas won"t be drawn.